A Novel 15-Level Inverter Topology With Reduced Count of Switches

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Abstract- *This paper introduces a new multilevel converter topology, which can synthesize all possible additive and subtractive combinations of input DC levels in the output voltage waveform with fewer power electronic switches. An appropriate modulation scheme has also been proposed for high switching frequency operation of the proposed topology. As compared with the classic multilevel topologies, the proposed topology results in reduction of the number of switches and conduction losses. The operation and performance of the proposed multilevel converter has been ascertained through simulation. A 15-level inverter with asymmetric source configuration has been presented or using the proposed modulation scheme. The results are verified using MATLAB/SIMULATION environment.*

Keywords- Multilevel inverter(MLI),APOD, POD, Total harmonic distortion(THD).

I. INTRODUCTION

A multilevel inverter produces a staircase waveform with the help of proper connection of switches and input DC voltages i.e. battery. Regulated switching of semiconductor devices plays an important role to achieve a multilevel waveform with controlled amplitude of waveform, and frequency[1-4]. This approach of DC to AC conversion offers a number of advantages over conventional inverters, such as: capability to operate at higher voltages using traditional semiconductors, reduced common mode voltages, and reduced dv/dt stresses, staircase waveform with better harmonic profile, smaller filter requirements, flexibility to operate on low- and high switching frequencies. As a result, multilevel inverters nowadays attract attention in high-power and high-voltage/medium-power applications. Although classical multilevel topologies such as Diode clamped clamped (DCMLI) converters [5], flying capacitors (FCMLI) converters [6] and cascaded H-bridge (CHBMLI) converters [7] have been commercialized, but device count becomes significantly high when they are to be designed for higher number of voltage levels. This introduces complexity in design and increase of cost. Therefore new topologies are being proposed and reduce the overall count of active and passive devices for power conversion [8-10]. However, reducing the number of devices involves one or more of following compromises: increased power rating of semiconductor devices, increased number of power sources, and complex modulation schemes. In spite of these compromises, there is still a possibility of exploring topological structures which can maximize the number of levels with given input DC sources.

In this paper, a multilevel inverter topology is proposed, which is capable of synthesizing all possible additive and subtractive combinations of the input DC levels. The proposed topology bears functional similarity to the CHB topology in two ways: first, it needs multiple isolated input DC voltages; and secondly, it offers the possibility of combining the input DC voltage levels into all additive and subtractive values. An important advantage of the proposed topology over the conventional topologies topology is in terms of ON state losses which are reduced considerably. The topology can be explored for various industrial i.e. grid interfacing of renewable energy sources (e.g. photovoltaic energy) [11], static synchronous compensators (STATCOMs) speed control of drives etc.

II. PROPOSED 15-LEVEL MULTILEVEL INVERTER TOPOLOGY

The proposed topology aims at synthesizing all possible combinations that can be attained through additions and subtractions of input DC voltage levels as described below in Fig.1.This topology is have reduced number of switch count and produces output voltage of 15-level output. Possible output voltage levels for V_1=13, V2=39 and V_3=39 are 13V,26V, 39V,52V,65V,78V,91V,0V,-13V,-26V,-39V,-52V,-65V,-78Vand -91V.

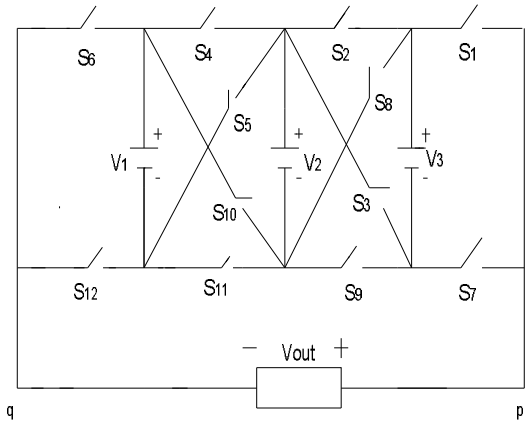

Fig.1 Proposed 15-Level MLI

Table I: Look Up table for 15-Level Inverter topology

Output Level	Corresponding Voltage value	Switches in ON state
0	0	S_1,S_2,S_4,S_6
1	V_3 =13	S_1,S_2,S_4,S_{12}
2	V_1-V_3=26	S_1,S_9,S_6,S_{11}
3	V_1=39	S_1,S_9,S_{12},S_{11}
4	V_1+V_3=52	S_1,S_3,S_4,S_{11}
5	V_1+V_2-V_3=65	S_1,S_3,S_{11},S_6
6	V_1+V_2=78	S_1,S_3,S_{11},S_{12}
7	V_1+V_2+V_3	S_1,S_3,S_5,S_{12}
-1	-V_1	S_7,S_9,S_{11},S_6
-2	V_3-V_1	S_7,S_2,S_4,S_{12}
-3	-V_1	S_7, S_2, S_4, S_6
-4	-V_1-V_3	S_7, S_8, S_{11}, S_6
-5	-V_1-V_2-V_3	S_7,S_8,S_4,S_{12}
-6	-V_1-V_2	S_7,S_8,S_4,S_6
-7	-V_1-V_2-V_3	S_7,S_8,S_{10},S_6

With such combinations of switches applications 15 level of output voltage is produced. Relevant look up table is shown with switching combinations for 15-level of output voltage production. For one level of output four switches are turned ON can be seen through table I.

III. WORKING OF PROPOSED TOPOLOGY

In this section operating modes of propose topology is introduced. From Fig.2 all operating modes are explained through relevant diagrams.

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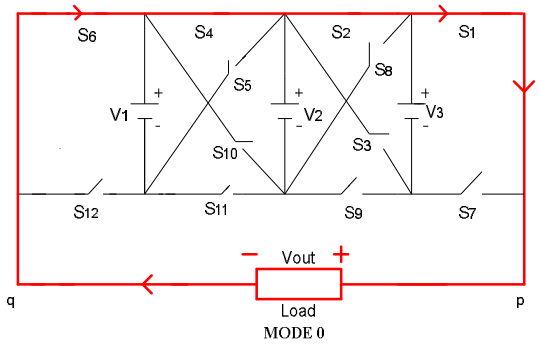

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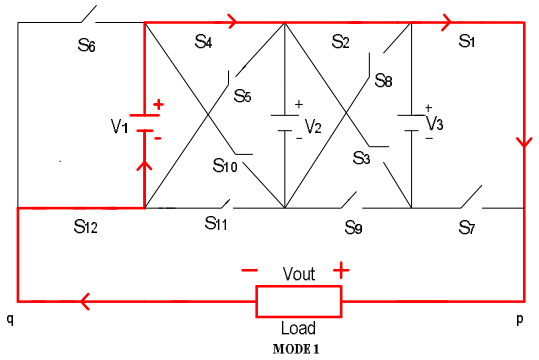

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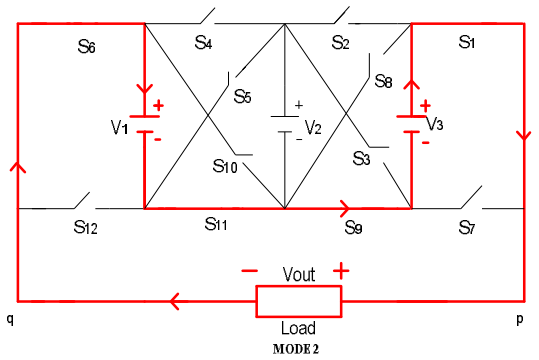

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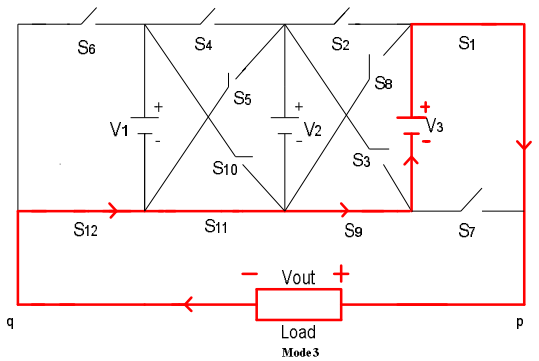

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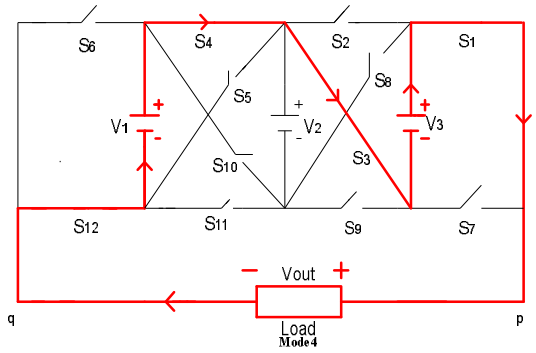
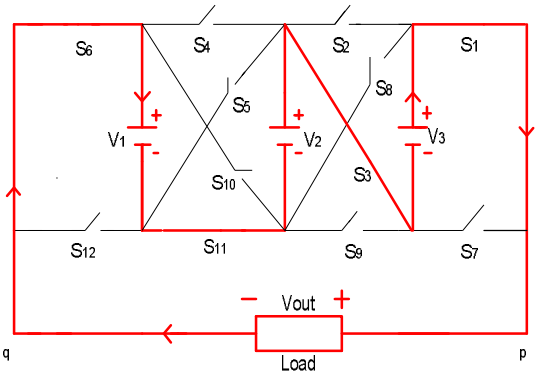


Mode 4

Mode 5:



Mode5

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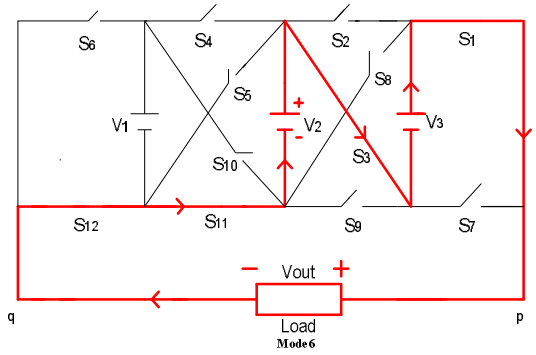

Mode6

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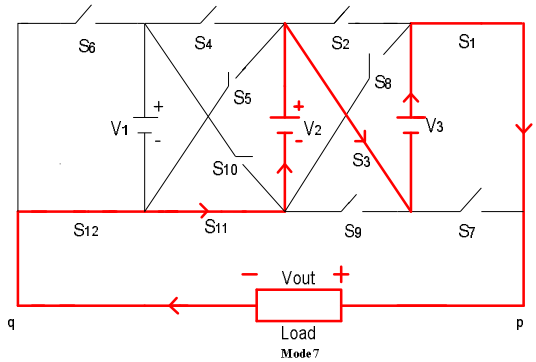
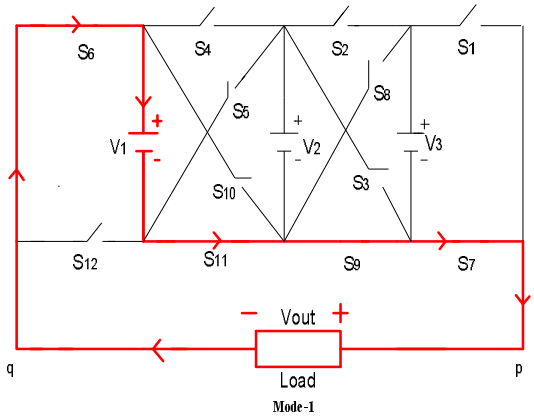


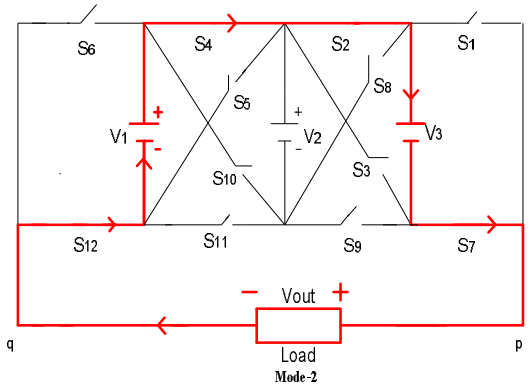
Mode7

Mode-1:



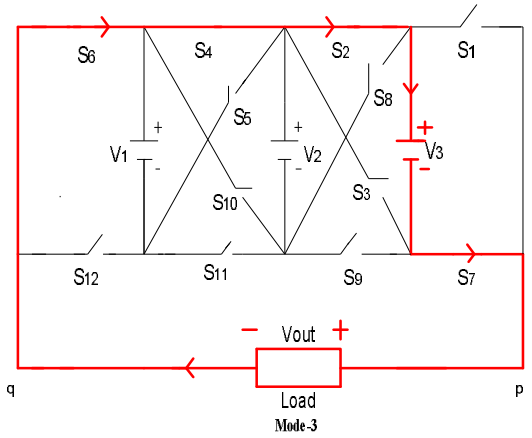
Mode-1

Mode -2:



Mode-2

Mode -3:



Mode-3

Mode-4:

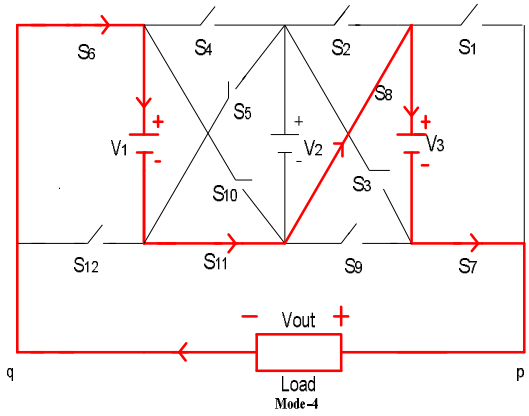
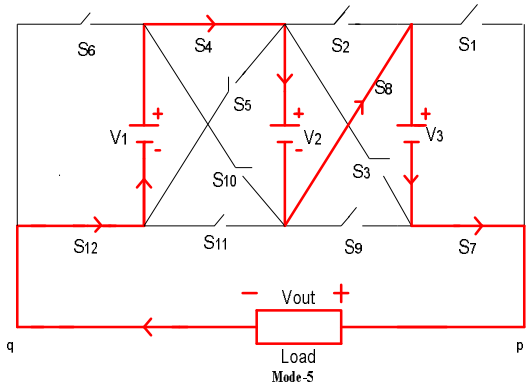


Fig.2 Operating modes of 15-level inverter

Mode -5:



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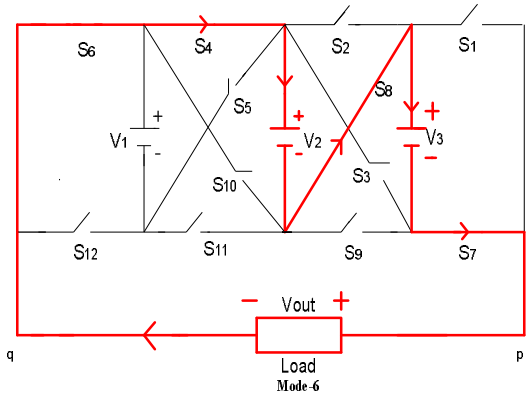
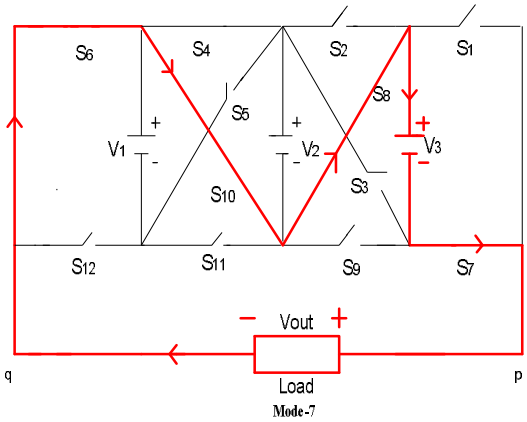


Mode -7



IV. MULTICARRIER PWM SCHEMES

Carrier shifting techniques:

a) Phase Disposition (PD)[12]
b) Phase Opposition Disposition (POD)[13]
c) Alternate Phase opposition Disposition (APOD)

All these techniques employed in proposed topology and these are high carrier frequency triangular wave with reference is sinusoidal wave.

4.1Phase Disposition (PD):

In this technique alternate waves are shifted from one other by magnitude of '1'. All the triangular carriers are in phase and compared with sinusoidal reference wave. Sine reference is compared with carrier wave and output pulse is obtained at reference wave magnitude is more than carrier wave.

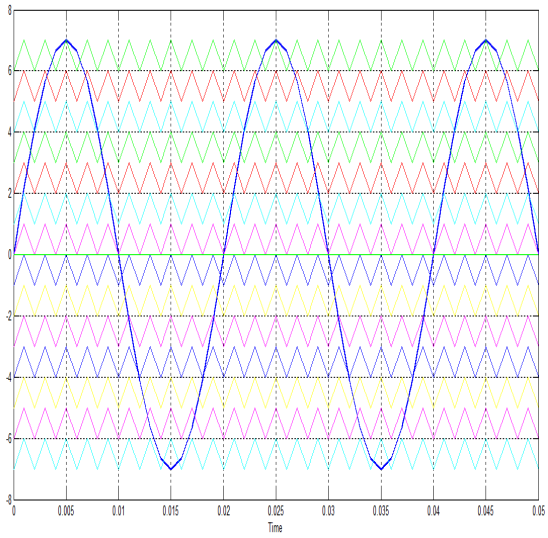


Fig.3 PD technique waveform

4.2. Alternate Phase opposition disposition technique (APOD)[14]

In this technique alternate waves phase shifted by 180 degrees and disposed from each other by '1'.Sine wave is reference and triangular wave is high frequency wave which is to be compared. Output is obtained at instant where reference wave magnitude is more than carrier wave.

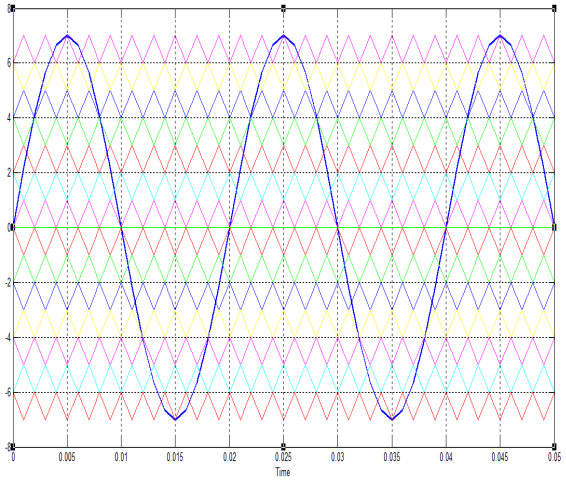


Fig.4 APOD technique waveform

4.3 Phase Opposition Disposition Technique (POD)

In this technique positive and negative side of reference line is phase shifted by 180 degrees. Sine reference is compared with carrier wave of high frequency .Output pulse is obtained when sine reference is more than carrier wave.

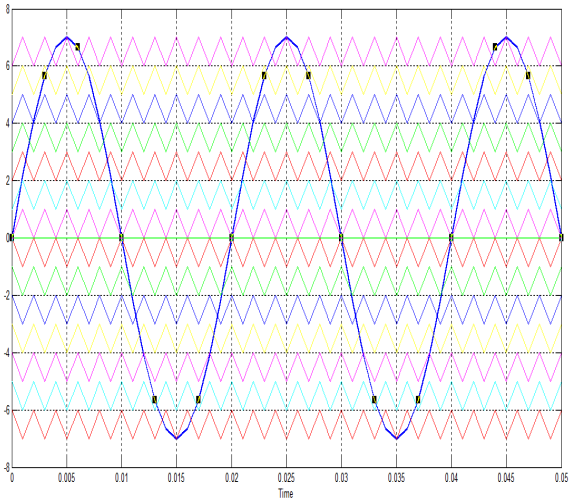


Fig.5 POD technique waveform

V. RESULTS

THD i.e. total harmonic distortion is parameter used to ascertain quality of inverter if THD is less then efficiency will be high, insulation losses are less and harmonic components i.e. third harmonic is less and can be filtered easily with small filter. It can be easily ascertained that PD techniques offers least THD OF 5.89% hence it is best suited for proposed topology. Whereas APOD and Pod offers high THD hence reduced efficiency is achieved by these modulation schemes .FFT analysis are shown from Fig.7 to Fig.9 of PD,POD and APOD respectively. Output voltage waveform is shown in Fig.6 having staircase waveform of 15 levels. Table II shows respective THD values for various modulation schemes at different modulation indices. Further Table III shows comparison of propose topology with conventional schemes of same level of output.

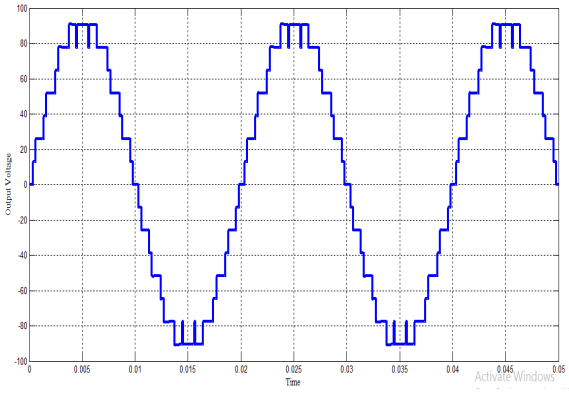


Fig.6 Output voltage waveform

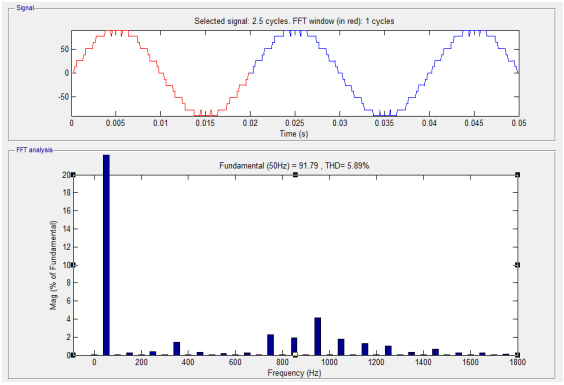


Fig.7 FFT analysis of PD Technique at ma==1

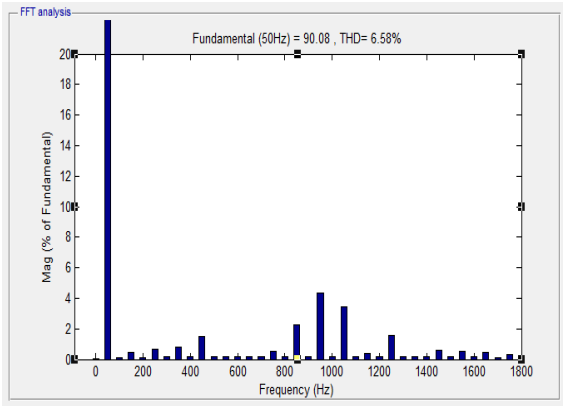


Fig.8 FFT analysis of POD technique at $m_{a=}1$

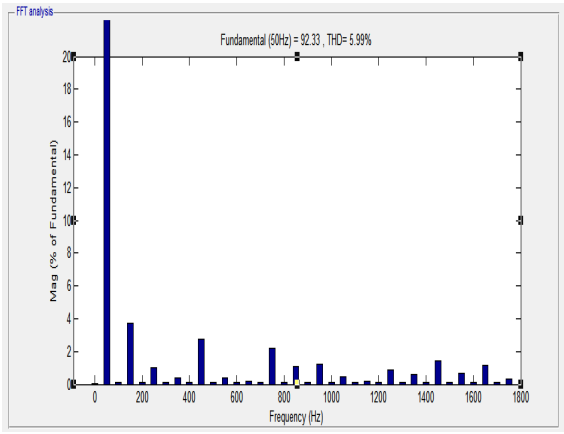


Fig.9 FFT analysis of APOD technique at ma=1

Table II:THD for various techniques at various modulation indices

Modulation technique	Modulation index(m_a)			
	1	0.95	0.9	0.87
PD	5.89%	8.15%	8.34%	8.27%
POD	6.58%	7.44%	8.02%	8.89%
APOD	5.99%	8.71%	8.78%	9.31%

Table III: Comparison of device requirement of conventional to proposed topology

Inverter topology	DCMLI	Flying capacitors	CHB	Proposed topology
Main switches	28	28	28	12
Clamping diodes	182	0	0	0
DC bus capacitors	14	14	0	0
Total components	224	42	28	12

VI. CONCLUSION

It can be well conclude that by increasing no of levels of inverter better wave shape near to sinusoidal is produced having low distortion.THD is considerably reduced by applying multicarrier PWM schemes. More efficient inverter with reduced count of switches than conventional topologies is synthesized. With less count of switches switching losses are reduced and gate driver requirement is reduced.

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