A Switch Ladder Topology For 31-Level Multilevel Inverter With Different PWM Techniques

Deepak Singh[1], Praveen Bansal[2]
[1, 2] Dept of Electrical Engineering
[1, 2] Madhav Institute of Technology & science Gwalior, India

Abstract- *The demand of multi-level inverter has been expanded due to their high power practical application and the capability for getting just about a sinusoidal output voltage liken to conventional two level inverter. This paper orient to develop a new variety of switch ladder multilevel inverter configuration for generations of thirty one levels of output voltage.*

This proposed multilevel inverter topology here is implemented with different pulse width modulation (PWM) techniques, which involve less count of power switches and voltage sources to bring down the complexness of a circuit as compare to other multilevel inverter configurations. A multicarrier PWM technique is used to generate 31-level output voltage. MATLAB/simulation is used to simulate the results of a 7-level multilevel inverter topology.

Keywords- multilevel inverter (MLI), thirty one level inverter, asymmetric topology, total harmonic distortion (THD), multicarrier pulse width modulation.

I. INTRODUCTION

In recent decades with the improvement of power semiconductor engineering, multilevel inverter (MLI) have obtained enormous popularity in researches as well as in industries owing to role in high power and high voltage practicle applications [7]. The commencement of the word " multilevel inverter " was recorded in year 1970s and 1980s. The introductory unit of a multilevel inverter is called three level. It is similar to a square wave form [3]. The some major applications areas of multilevel invertor are : high power medium voltage drives, HVDC transmission, distributed generations, electrical vehicular technology, static VAR compensator, induction heating, stand by air – craft power supplies, UPS (uninterruptable power supplies) for computer[2]. The advantages to use a multilevel inverter than a two level inverters configurations are decrease total harmonic distortion (THD), decrease dv/dt stress across devices, less electromagnetic interference (EMI), less common mode voltage and improve use of rail voltage etc [4].

Several multilevel topologies have been classified as the diode clamped multilevel inverter (DCMLI), the flying capacitor multilevel inverter (FCMLI), the cascaded H-bridge multilevel inverter (CHBMLI) [6]. The diode clamped and flying capacitor converter configurations function with the single DC source but the number of device increase parabolically with the number of output levels raises production cost and complicated control.

This paper present a new 31-level topology of switch ladder multilevel inverter configuration in section II, using fixed frequency level shifted carrier based pulse width modulation techniques which require for decrease deformation of sinusoidal voltage and less number of power switches.

II. PROPOSED MULTILEVEL INVERTER

The proposed switch ladder 31 level multilevel inverter (SLMI) is shown in figure 2.1. In this circuit there are six unidirectional switches (S3, S4, S7, S8, S9, S10) , four bidirectional switches (S1, S2,S5,S6), and six DC sources in which two have same magnitude V1 and other two have V2 . The values of dc sources are V1= 25V and V2 = 100V. The values of output voltages frequency is 50 Hz. The R-L load with the values of R= 108 Ω and L = 45mH is used for this topology. It is clear that the maximum output voltage is 375V. Fig. 5.1 shows the output voltage of 31level inverter. The levels are:0v,±25v,±50v,±75v,±100v,±125v,±150v,±175v,±200v,±225v,±250v,±275v,±300v,±325v,±350v,±375v.

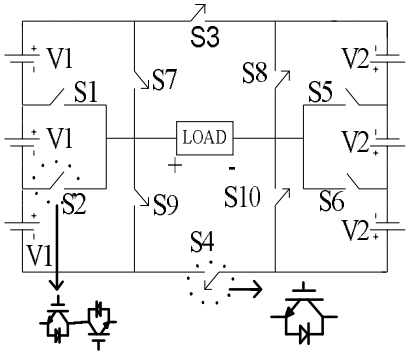


Fig. 2.1 SWITCH LADDER MULTILEVEL INVETER

TABLE 1 shows the value of output voltages (Vo) for the different states of S1, S2, S3, S4, S5, S6,S7,S8,S9 and S10 Switches.

No.	Switches States (1 – ON, 0 – Off)										Vo
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	
1	0	0	1	0	0	0	1	1	0	0	0
2	0	1	0	1	0	0	0	0	0	1	25
3	1	0	1	0	0	0	0	1	0	0	-25
4	1	0	0	1	0	0	0	0	0	1	50
5	0	1	1	0	0	0	0	1	0	0	-50
6	0	0	0	1	0	0	1	0	0	1	75
7	0	0	1	0	0	0	0	1	1	0	-75
8	0	0	0	1	0	1	0	0	1	0	100
9	0	0	1	0	1	0	1	0	0	0	-100
10	0	1	0	1	0	1	0	0	0	0	125
11	1	0	1	0	1	0	0	0	0	0	-125
12	1	0	0	0	1	0	1	0	0	0	150
13	0	1	1	0	1	0	0	0	0	0	-150
14	0	0	0	1	0	1	1	0	0	0	175
15	0	0	1	0	1	0	0	0	1	0	-175
16	0	0	0	1	1	0	0	0	1	0	200
17	0	0	1	0	0	1	1	0	0	0	-200
18	0	1	0	1	1	0	0	0	0	0	225
19	1	0	1	0	0	1	0	0	0	0	-225
20	1	0	0	1	1	0	0	0	0	0	250
21	0	1	1	0	0	1	0	0	0	0	-250
22	0	0	0	1	1	0	1	0	0	0	275
23	0	0	1	0	0	1	0	0	1	0	-275
24	0	0	0	1	0	0	0	1	1	0	300
25	0	0	1	0	0	0	1	0	0	1	-300
26	0	1	0	1	0	0	0	1	0	0	325
27	1	0	1	0	0	0	0	0	0	1	-325
28	1	0	0	1	0	0	0	1	0	0	350
29	0	1	1	0	0	0	0	0	0	1	-350
30	0	0	0	1	0	0	1	1	0	0	375
31	0	0	0	1	0	0	0	0	1	1	-375

The number of output voltage levels and the
Number of bidirectional switch and value of DC sources V1 and V2 are obtained as follows,

V1 = Vdc (1)

V2 = (n) Vdc (2)

Vo = (n-1)(V1 + V2) (3)

Where n represent the no. of bidirectional switch in SLMI.

III. OPERATING MODES

Various operating modes to obtain different voltage levels are shown in the following figures.

Figure 3.1 shows the different operating modes of switch Ladder 31- level Multilevel Inverter.

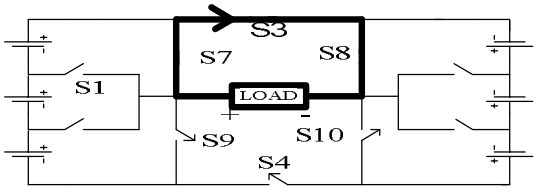


Fig 1 ; V0 = 0v

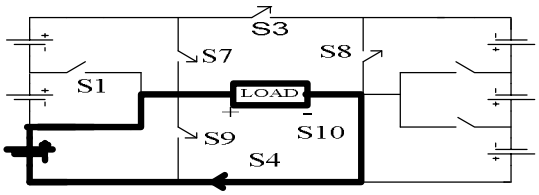


Fig 2 ; V0 = 25v

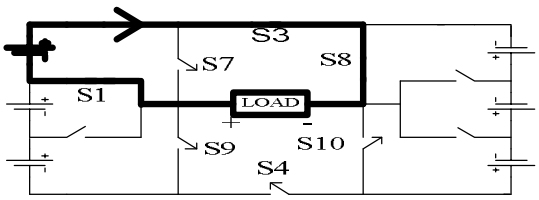


Fig 3 ; V0 = -25v

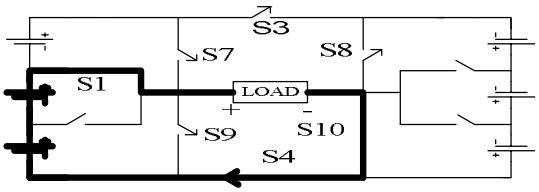


Fig ; 4 V0 = 50v

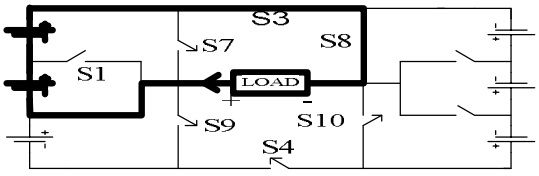


Fig 5 ; V0 = -50v

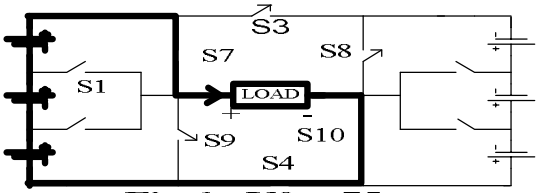


Fig 6 ; V0 = 75v

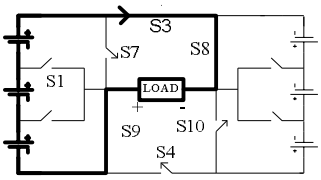


Fig 7 ; V0 = -75v

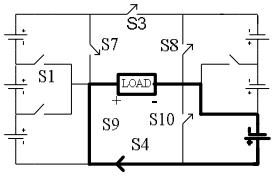


Fig 8 ; V0 = 100v

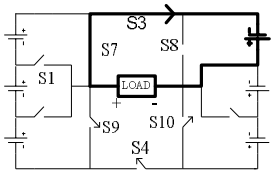


Fig 9 ; V0 = -100v

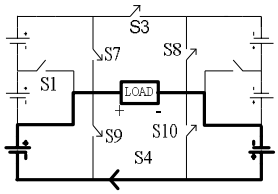


Fig 10 ; V0 = 125v

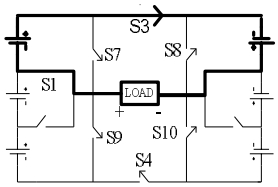


Fig 11 ; V0 = -125v

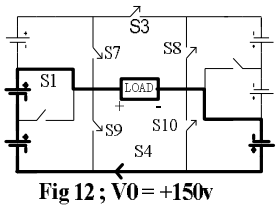


Fig 12 ; V0 = +150v

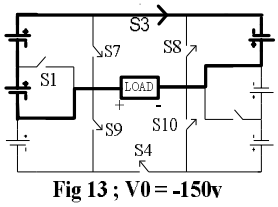


Fig 13 ; V0 = -150v

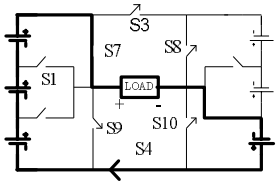


Fig 14 ; V0 = 175v

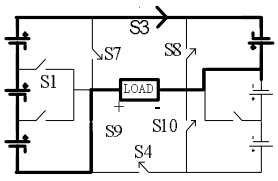


Fig 15 ; V0 = -175v

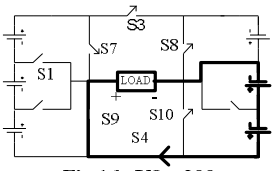


Fig 16 ; V0 = 200v

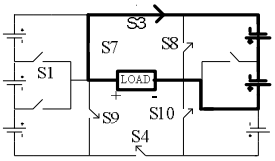


Fig 17 ; V0 = -200v

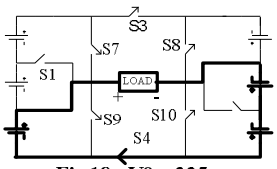


Fig 18 ; V0 = 225v

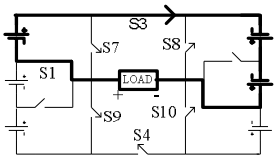


Fig 19 ; V0 = -225v

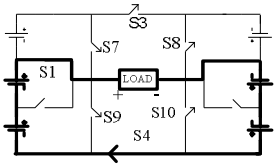


Fig 20 ; V0 = 250v

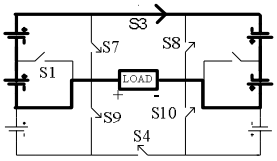


Fig 21 ; V0 = -250v

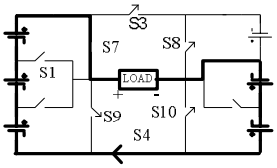


Fig 22 ; V0 = 275v

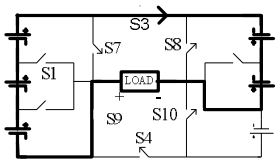


Fig 23 ; V0 = -275v

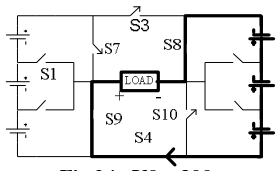


Fig 24 ; V0 = 300v

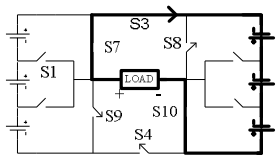


Fig 25 ; V0 = -300v

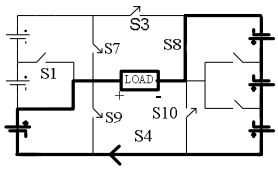


Fig 26 ; V0 = 325v

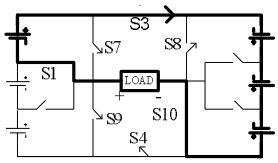


Fig 27 ; V0 = -325v

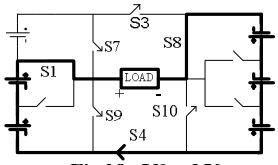


Fig 28 ; V0 = 350v

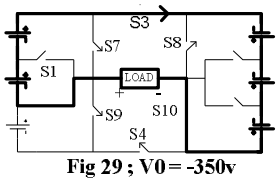


Fig 29 ; V0 = -350v

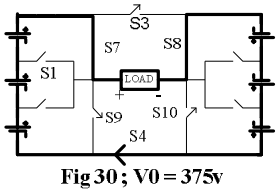


Fig 30 ; V0 = 375v

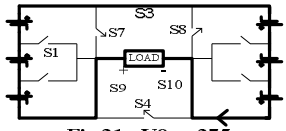
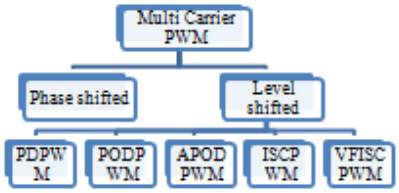


Fig 31 ; V0 = -375v

Fig 3.1(Fig 1 – fig 31) shows Different operating modes of proposed MLI

IV. MULTICARRIER PWM

Different types of MCPWM modulation techniques are



The entire above multicarrier pulse width modulation techniques are use in high frequency switching.

- **PHASE DISPOSITION (PD) TECHNIQUE** In PD technique all carrier waveform are superimposed over one another like layer with same phase, amplitude and frequency as shown in figure 4.1

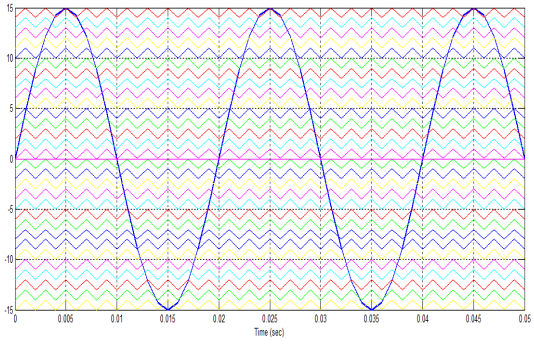


Fig. 4.1

- **PHASE OPPOSITION DISPOSITION (POD)TECHNIQUE**
  In POD technique the carrier waveforms above or below the zero reference are phase shifted by 180 degree as shown in figure 4.2

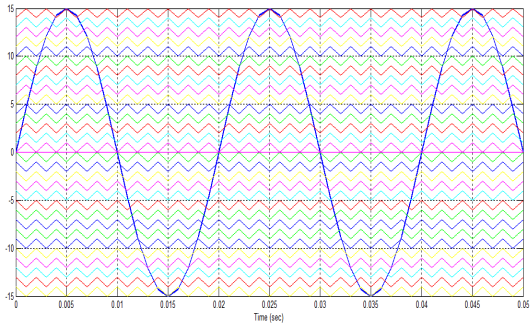


Fig. 4.2

- **ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD -PWM) TECHNIQUE** In APOD technique all the adjacent carriers are 180 degree out of phase from each other on either side of zero reference level as shown in figure 4.3

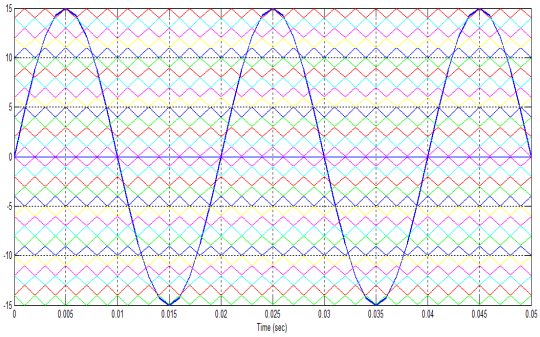


Fig. 4.3

- **INVERTED SINE CARRIER PWM TECHNIOUE** In ISCPWM technique inverted sine wave of certain constant frequency acts as a carrier signal as shown in figure 4.4

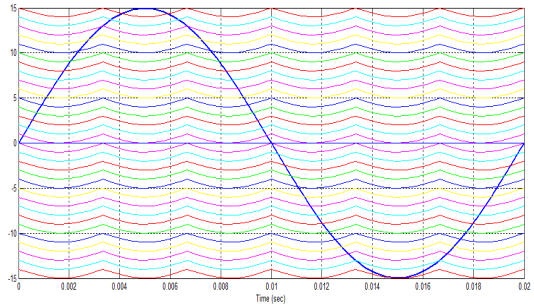


Fig. 4.4

V. SIMULATION RESULT

Multiple Modulation techniques is presented for proposed inverter topology and it has found out that by increasing the output voltage level THD can be considerably reduced. THD depicts the harmonic contents in the output voltage wave and by increasing the levels of output voltage, we can reduce THD and associate losses, thereby increasing efficiency. FFT analysis is shown for various modulation schemes from Fig. 5.3 to Fig. 5.6. On application of POD technique at m_a=1 THD is 3.48%, and for PD, APOD and ISCPWM technique at m_a=1 THD is 3.52% 3.75%, 6.38% respectively. Thus POD technique minimize the THD to 3.48% is as per IEEE standard 519 and it is best suited for proposed topology.

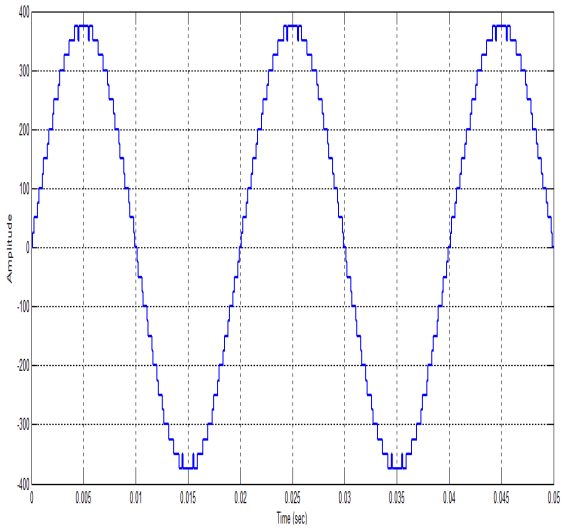


Fig.5.1 Output Voltage waveform for a 31 level MLI

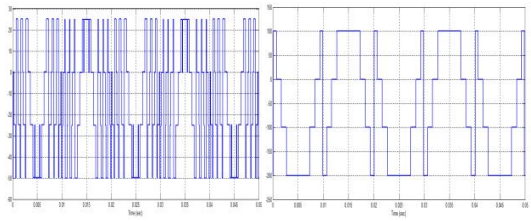


Fig. 5.2 Voltage waveform of bidirectional switches S1 and S5

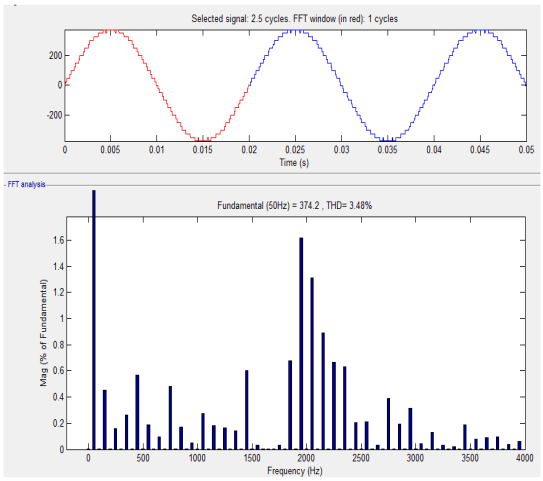


Fig. 5.3 FFT analysis by PODPWM for RL load (Ma= 1, Mf= 80)

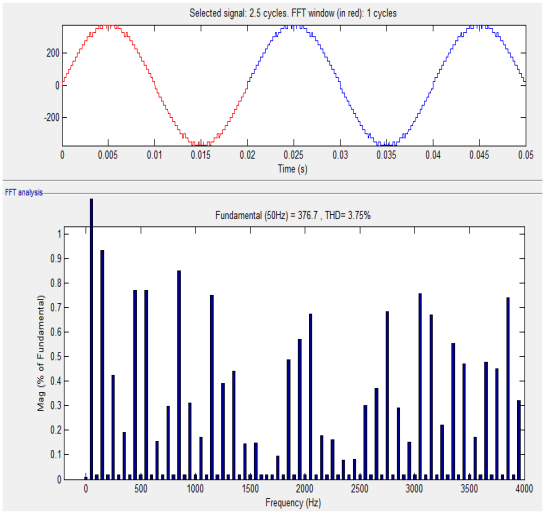


Fig. 5.4 FFT analysis by APODPWM for R-L Load (Ma = 1, Mf = 80)

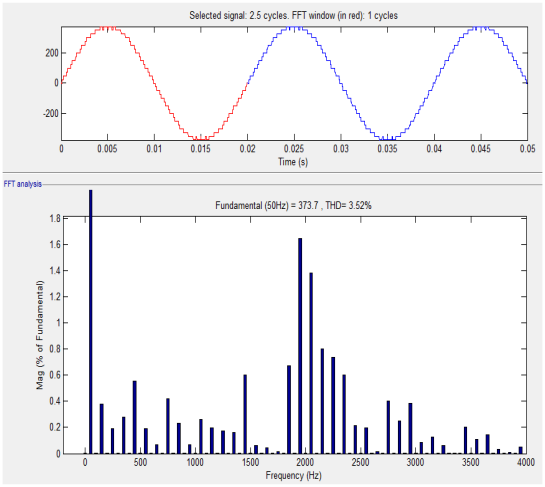


Fig. 5.5 FFT analysis by PDPWM for R-L Load (Ma = 1 , Mf = 80)

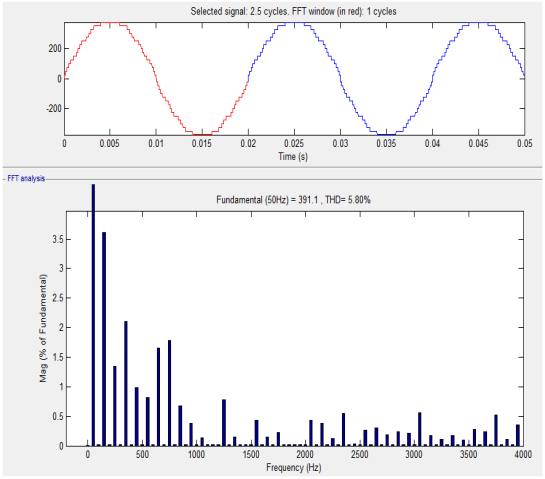


Fig 5.6 FFT analysis by ISCPWM for R-L load (Ma =0.95 , Mf = 80)

TABLE-III THD analysis between different PWM techniques for 31-level MLI topology

SCHEMES	% THD				
MODULATION INDICIES (MI)	1	0.95	0.9	0.85	0.8
PD	3.52	3.99	4.69	4.53	4.91
POD	3.48	4.05	4.64	4.44	4.84
APOD	3.75	4.28	4.88	5.12	4.80
ISCPWM	6.38	5.80	6.23	6.61	6.54

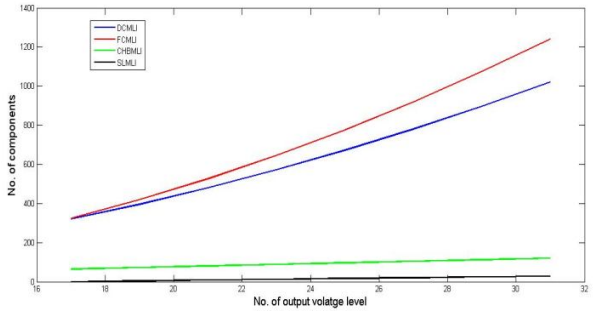


Fig. 5.7 Comparison between different multilevel inverter topologies

VI. CONCLUSION

In this paper 31-level Switch Ladder multi-level inverter topology is proposed with different PWM techniques and it is being found that the SLMLI is the too encouraging choice for industry application. The switching operation of this topology requires less number of switches, less gate drive circuits and higher reliability as compared to conventional MLI topologies. It can be seen that the different PWM techniques reduce the harmonics. Phase opposition disposition (POD) technique to reduce THD of 3.48% and obtain nearer sine wave.

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Deepak Singh was born in Mathura, India. He Received B.Tech Degree in Electrical Engineering from UPTU, Lucknow, India , currently he is doing M.E. at the Department of electrical engineering, M.I.T.S. Gwalior, India since 2016. His area of interest in the power electronics, Multilevel Inverter.

Praveen Bansal born in Gwalior, India. He Received B.E. Degree in Electrical Engineering from M.I.T.S Gwalior, India in 2009 with Honours. He is received M.Tech degree in electrical drives From M.N.I.T. Bhopal, India in 2012.Currently he is Assistant Professor in M.I.T.S Gwalior, India .His area of interest in power electronics and drives.