The Design of Phase Locked Loop Using 180nm VLSI Technology

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Abstract- *Phase locked loops (PLLs) can be found in many different types of circuits nowadays. Their applications range from a variety of uses. From synchronization of clock signals, demodulation, clock recovery, jitter and noise reduction, and de-skewing, the list of different fields to which PLL operation can be applied is extensive. A PLL operates by comparing a certain operating frequency with the circuit clock frequency and subsequently adjusting its output to match the input. It is analogous to a car's cruise control system. As the car exceeds the speed specified by the user, the system slows it down. If the car's speed drops below the specified level, the car speeds up.*

Keywords- PLL, CMOS, 180 nm

I. INTRODUCTION

A PLL is a feedback system that compares the output frequency/phase with the input frequency/phase. Phase-locked loops can be making used for frequency synthesizing, carrier synchronization, Carrier recovery, Frequency division, frequency multiplication and frequency Demodulation. A VCO is the compassion of the PLL and shall be designed either by LC or RC. A LC VCOs have higher phase noise performance compared with ring VCO's. Nevertheless, the LC VCO has a small tuning range for large layout area and probably has higher power. The ring oscillators do not have the problem of the on-chip inductors vital for the LC oscillators.

- **Existing system**

Most of the existing systems are physical systems. The physical systems needs high power, more area and operating frequencies are also less. Considering this the cost of physical system is also more. In today's world VLSI is more advanced and much needed field to improve overall performance of any device. The one device which is developed in VLSI will have high operating frequency, uses less power, more accurate outputs, uses less area etc. Majority of PLL designs uses inverter based phase frequency detector (PFD) it has many design issues with it a few are listed below.

- **Proposed system**

To improve the performance of design in low power digital circuit we used the pass transistor logic (PTL).Pass transistor it is like electronic switch with properties like non-mechanical relay, uses CMOS technology. Some of merits of PTL over standard CMOS design are: a) Low power dissipation, as it uses less number of transistor b) It requires less area hence low inter connection .c) High speed because of small node capacitances. However most of PLL implementations incur with two main basic problems.

In this design, the biasing circuit can operate at voltages even lesser than 0.8V and eventually save a significant amount of power.

II. BLOCK DIAGRAM OF PROPOSED SYSTEM

As shown in block diagram the PLL is mainly consists of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO), and a frequency divider (FD) blocks.

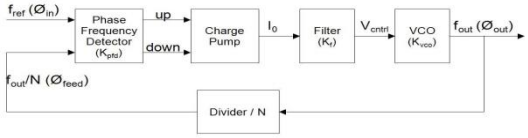

Fig .1 Block Diagram of Phase Locked Loop

Whenever an input (fref) or reference signal is applied to the phase detector block a VCO is produce an output which matches the input signals phase and frequency.To maintain a well-defined phase and hence frequency relation between two independent signal sources, PLL can be used.

Table 1: The various parameters used

VARIABLES	DESCRIPTION
fref	The input reference signal and its corresponding phase
fout/N	The feedback signal and its corresponding phase
Kpfd	The gain of the PFD block
up, down	The output signals of the PFD block
Io	The current fed into the filter by the charge pump
Kf	The gain of the filter/impedance of the filter
Vcntrl	The control voltage applied to the VCO
Kvco	The gain of the VCO
Fout	The output signal and its corresponding Phase
N	The factor of frequency division

PROPOSED DESIGN WORKING

As shown in block diagram the PLL is mainly consists of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO), and a frequency divider (FD) blocks. Which are connected as shown in fig1. Whenever an input (fref) or reference signal is applied to the phase detector block a VCO is produce an output which matches the input signals phase and frequency.To maintain a well-defined phase and hence frequency relation between two independent signal sources, PLL can be used[4].

III. IMPLEMENTATION

The main components to design and verify the simulation result

1. PHASE FREQUENCY DETECTOR
2. CHARGE PUMP
3. LOW PASS FILTER
4. VOLTAGECONTROLLED OSCILLATOR
5. FREQUENCY DIVIDER

- **PHASE FREQUENCY DETECTOR**

A phase frequency detector (PFD) is a device, which compares the phase of two input signals and provides a signal in the form of phase error. It has two inputs which match up to two different input signals, generally one from a voltage controlled oscillator and other is a reference source. The Schematic Circuit of Phase Frequency Detector. Compares the primary edges of data and data1 (data is the input signal and data1 is the feedback signal).

Design the above showed schematic of PFD in virtuoso cell view by taking the following transistors values,

NMOS : length-180 nm , width- 240nm
PMOS : length- 180nm , width- 240nm

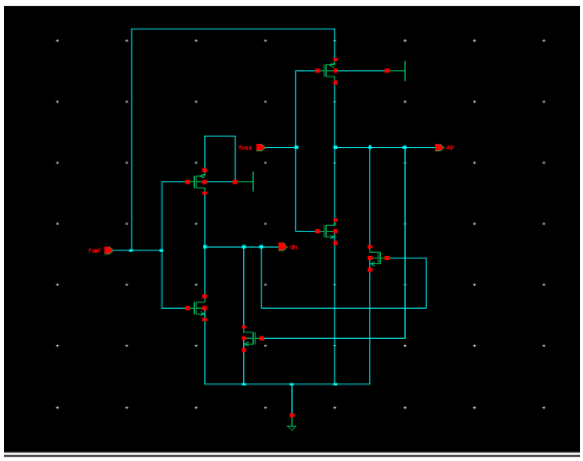

Fig 2: schematic of phase frequency detector (PFD)

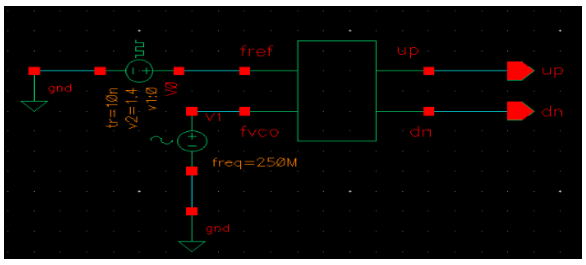

Fig 3. PFD test circuit

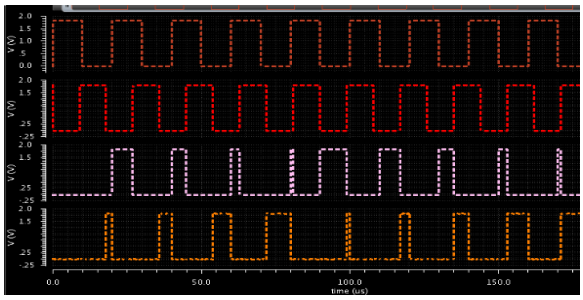

Fig 4. PFD block output with both (fref and fout) square waves

- **CHARGE PUMP**

A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. A charge pump circuit takes in the UP and DOWN output pulses from the PFD and changes it to a single DC voltage. At the start of the design process a simple schematic was used for the Charge Pump to see if the basic operation of the block could be verified[1].

Design a schematic with the transistor values as given below

PMOS: Length- 180nm, width- 1.2um
NMOS: Length-180nm, width- 600nm

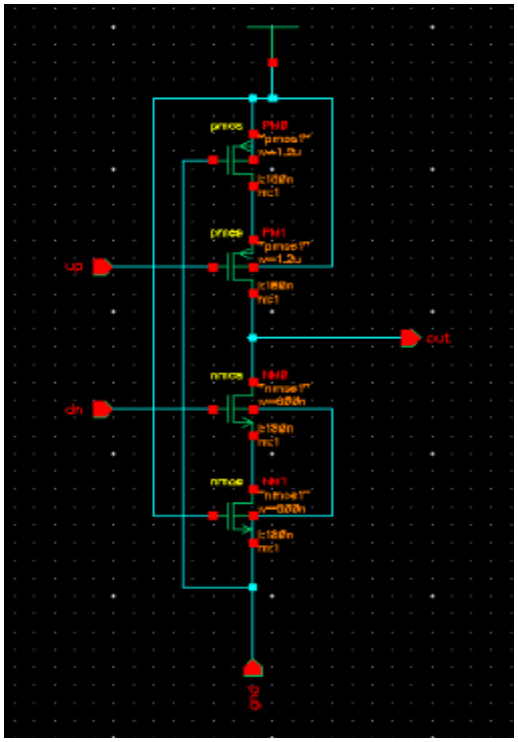

Fig 5: schematic of charge pump

- **VOLTAGE CONTROLLED OSCILLATOR**

The VCO is the one of the key components of the PLL. It is also one of the highest power consuming block in the PLL[4]. To reduce the overall power consumption of the PLL the supply voltage can be reduced. But in a conventional VCO with a current biasing circuit the VCO operating range usually starts from around 0.8V.

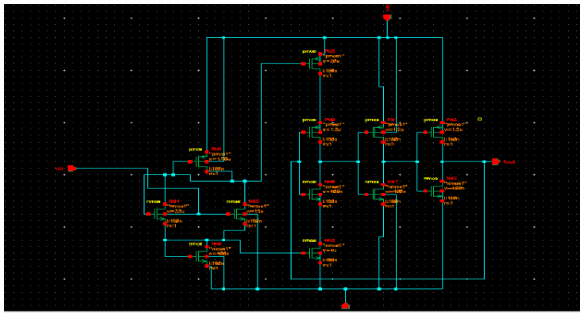

Fig 6. schematic of VCO

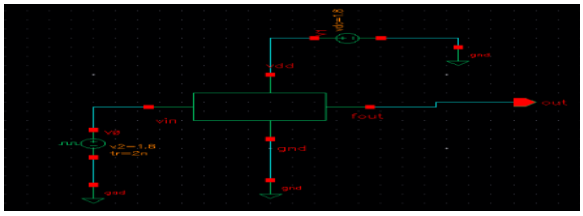

Fig 7. Test circuit of VCO

In this design, the biasing circuit can operate at voltages even lesser than 0.8 v and eventually save a significant amount of power. Design a schematic of voltage controlled oscillator as shown in the fig 5. make the connection as per the schematic use the same length and width of transistor to maintain low power and to get high operating frequency[3].

- **FREQUENCY DIVIDER**

Frequency divider divides the VCO frequency to generate a frequency, which is comparable with reference frequency. It divides the clock signal of VCO and then applied to phase frequency detector that compare it with input data. It divides the clock signal of VCO.

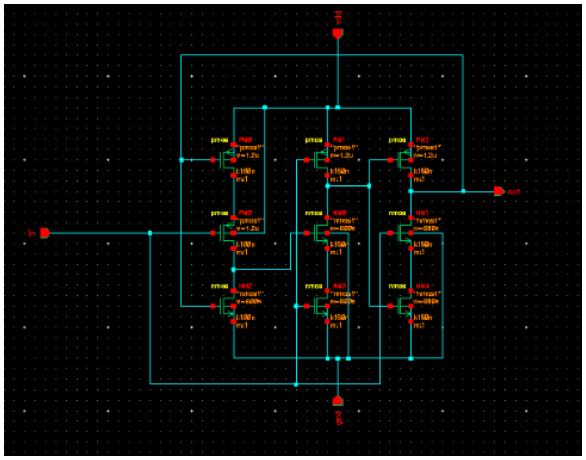

Fig 8. schematic of frequency divider

A frequency divider is needed to produce a clock signal that runs many times faster than the reference clock.

The PFD input clock and reference clock have to be synchronized for PLL to be in locked condition. In order to perform this task we use a fractional-N divider circuit, which divides the VCO clock by the highest power of 2 factor to synchronize reference clock signal and the divider output clock[6].

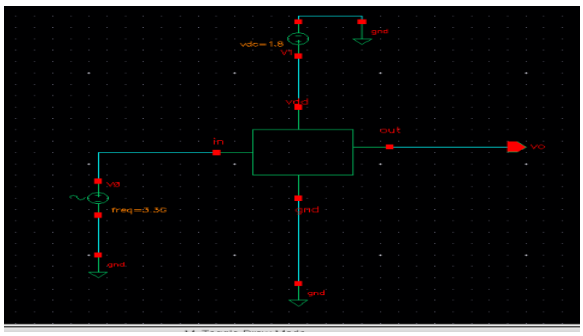

Fig 9. test circuit of frequency divider

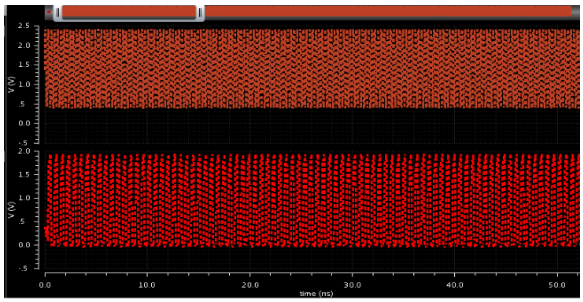

Fig 4.20 output of frequency divider

This is the output of FD where we can observe that a high frequency of VCO is divided by N to obtain fout/N frequency.

IV. EXPERIMENTAL SETUP OF PLL

The overall system arrangement is as shown in fig 10, where all 5 blocks are integrated together to form an functional Phase Locked Loop (PLL).

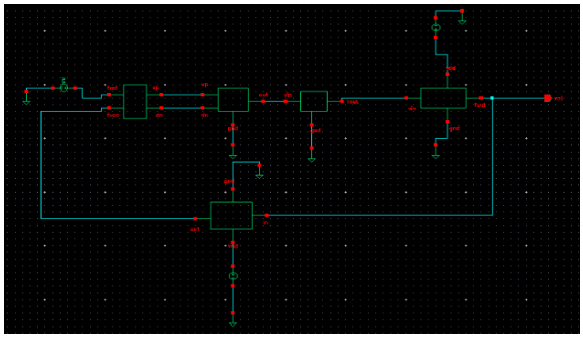

Fig 10. overall system view of PLL

Integrate all the blocks as shown in final PLL block and make the connections as per schematic. Apply the reference frequency (Vref) to the phase detector block, by selecting the terminals to be plotted in output obtain the final output of PLL and verify the output of PLL.

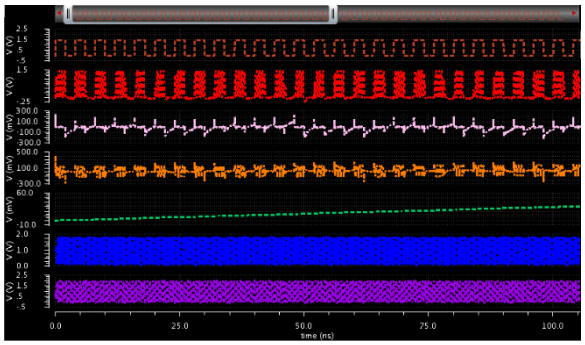

Fig 11. Final output waveforms of PLL

The fig 5.2 shows the final output of PLL here the signal 1 is reference (Fref) signal, signal 2 is phase detectors up signal, signal 3 is down signal, signal 4 is the output of charge pump , signal 5 is the input signal of VCO (output of LPF), and the signal 6 is the output of VCO i.e. the desired output of PLL, and the signal 7 is the output of frequency divider(FD) which is Fout/N feedback signal applied to the PFD block .

We have designed the VCO to obtain 3.2 GHz output signal, here in this PLL output we have successfully obtained 3.2 GHz output frequency by applying 250MHz input frequency signal[7].

V. CONCLUSION

Modern wireless communication system spend phase locked loop (PLL) mainly on synchronization clock synthesis, skew and jitter reduction. As to increase of speed of the circuit operation, there is required of a PLL circuit with faster locking capability. The PLL has been designed with low power, small chip size area, and high Frequency of oscillation and better phase noise using 180 nm CMOS technology for High performance PLL and simulated by CADENCE VIRTUOSO environment. While increasing the number of stages for getting the higher frequency the power dissipation and size of oscillator was going to increase. Therefore, instead of increasing the number of stages and time constant again control voltage and width of the CMOS can be adjusted for getting the higher frequency.

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