Low Power Pulse Triggered D-Flip Flops Using Mtcmos And Self-Controllable Voltage Level Circuit

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Abstract- *Reducing power consumption is a crucial task for any circuits. Increased demand for portable devices with reduced power dissipation has put necessary traction to design low power circuits. Both explicit and implicit pulse triggered flip flops are designed. Multiple Threshold CMOS (MTCMOS) technique and Self-controllable voltage level (SVL) circuit are employed to reduce power consumption. All the circuits are designed in 45nm technology for 1 GHz frequency.*

Keywords- Conditional Discharge Flip Flop (CDFF); Conditional Data Mapping Flip Flop (CDMFF); Clocked Pair Shared Flip Flop (CPSFF); MTCMOS; SVL

I. INTRODUCTION

In any integrated circuit, a tradeoff between power, area and delay are necessary. For certain applications, low power circuits will be needed and the design engineers have to compromise with more area and delay. Leakage power is another major concern. If the device dissipates more power in standby mode it calls for certain techniques to reduce them. Increased demand for mobile phones and other gadgets have steered for power efficient VLSI circuits

In digital circuits, we have mainly four major components of power dissipation.

$$\mathbf{Pt = {}^{\alpha}CLV^2ddfclk + Vdd(Isc + Ileakage + Istatic)} \quad (1)$$

P_t ⇨ Total power dissipation

C_L ⇨ Load capacitance

α ⇨ Node transition factor

First component in equation (1) denotes power dissipation during switching event. $\mathbf{I_{sc}}$ is the short circuit power which arises when both nMos and pMos transistors conduct simultaneously and hence forming a direct current path from power supply to the ground. Reverse diode leakage current and sub-threshold current contributes for $\mathbf{I_{leakage}}$.[1]

Flip-flop is widely used to store data in response to a clock pulse. Major portion of on chip power is consumed by clocked systems. More the number of clocked transistors more will be the power consumption. Clock systems have redundant transitions and hence reducing power consumption by flip flops will certainly have a profound impact on the total power consumed. Pulse Triggered flip flops can be explicit or implicit pulse triggered. Conditional Discharge Flip Flop (CDFF) is an explicit pulse triggered flip flop where we use an external pulse generator to generate the pulses. Conditional Data Mapping Flip Flop (CDMFF) and Clocked Pair Shared Flip Flop (CPSFF) are implicit pulse triggered flip flops. The output of implicit pulse triggered flip flop changes when there is an overlap between CLK and CLKB. During that particular instant both the CLK and CLKB will be HIGH for a very short duration. Multiple Threshold technique and SVL circuits can be successfully applied to get low power.

All the flip flops mentioned above are D- flip flops. The D flip flop is widely used. They are also called as “data” or “delay” flip flops. This flip flop captures value of the input at a definite portion of the clock (rising edge or level or pulse). The captured value gives the Q output. At other times, Q remains unchanged.

II. FLIP FLOP DESIGN

D flip flops are categorized as follows. Fig. 1 is Conditional Discharge Flip Flop (CDFF) which is an explicit type of pulse triggered circuit. It has a pulse generator circuit which generates the pulses and these pulses are fed to circuit as shown. Output switches the state during the high level of the pulses. The power dissipation is more. It has mainly two stages. The first stage does the LOW to HIGH transitions while the second stage is mainly for HIGH to LOW transitions. Fig. 2 is Conditional Data Mapping Flip Flop (CDMFF). It is a pulse triggered flip flop which samples the

input during the instant when CLK and CLKB overlap. The circuit has a feedback network as shown. When D=1, Q=0, the pass transistor turns ON. During that overlap period, there is a discharge path to ground through which precharge transistors discharges and hence output goes LOW.

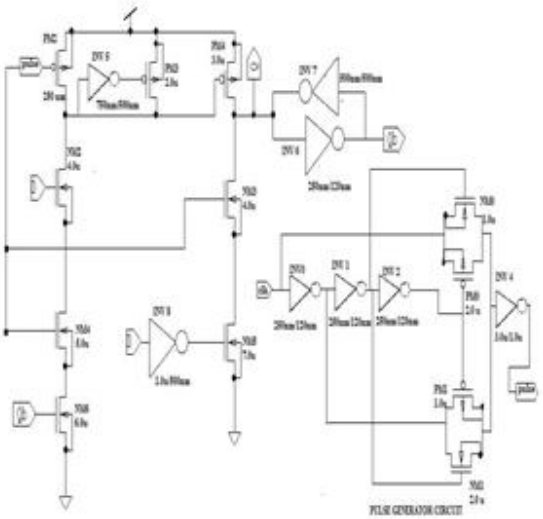


Fig. 1.Conditional Discharge Flip Flop

CDMFF has 7 clocked transistors. It exploits the property of flip flop with a stage that maps its input to (0, 0) if a redundant event is predicted. Here output act as the control signal. Though CDMFF provides low power consumption, it is more

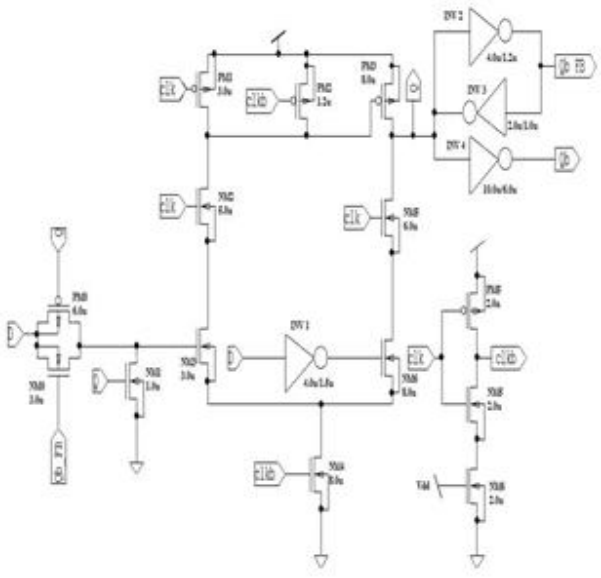


Fig. 2 Conditional Data Mapping Flip Flop

susceptible to redundant clocking in addition to floating node. As shown in Fig. 3 there is a pMos transistor which is always ON (PM1). This transistor is always connected to V_{dd}. It uses only 4 clocked transistors. Clocked Pair Shared Flip Flop has less power consumption than CDMFF. Both CDMFF and CPSFF have implicit pulse generation during which output switches its state.

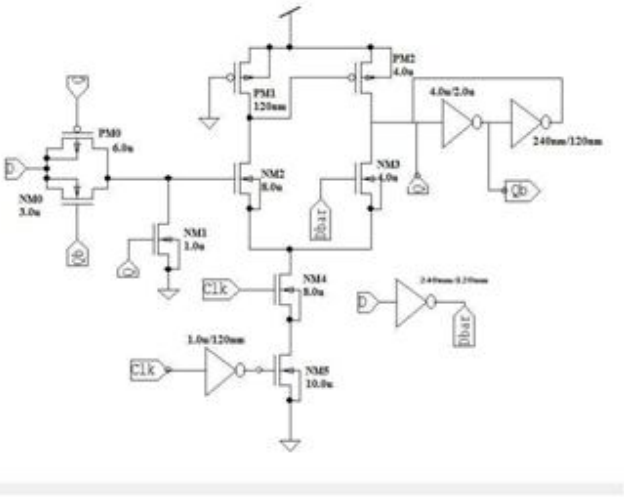


Fig. 3.Clocked Pair Shared Flip Flop

III. MTCMOS TECHNIQUE

Multiple Threshold CMOS technique is the most widely used technique to reduce the leakage current. As show in the fig. 4, there are two sleep transistors (PM0 & NM0) as the header and footer transistors. Typically nMos sleep transistors are effective. It is because they have got low ON resistance than that of pMos sleep transistors.

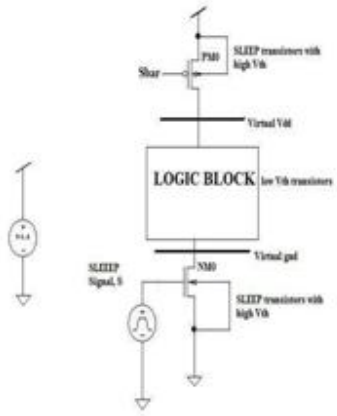


Fig. 4.MTCMOS Technique

MTCMOS technique uses two types of transistors with both high threshold voltage (V_t) and low threshold

voltage (V_t). Low V_t transistors are used where fast switching is required

High V_t transistors reduce leakage current. Another important feature of this technique is that it operates in two modes: ACTIVE and SLEEP. High V_t transistor is connected to V_{dd} and Gnd which gets turned ON during ACTIVE mode and OFF during SLEEP mode. During ACTIVE mode, transistors in the logic block are connected to V_{dd} and Gnd and while in SLEEP mode they are in floating state and hence there is no path to discharge thereby reducing the leakage current. However using both the header and footer transistors is the slowest solution. The circuit using only a gating nMos is the fastest. High V_t nMos transistors have the lowest area overhead and is the fastest but has a virtual ground which will bounce. Some designers prefer to have a noisy supply voltage maintaining a clean ground. This calls to use only a gated pMos even if it is a slowest solution.

MTCMOS technique is applied to CDFF, CDMFF and CPSFF.

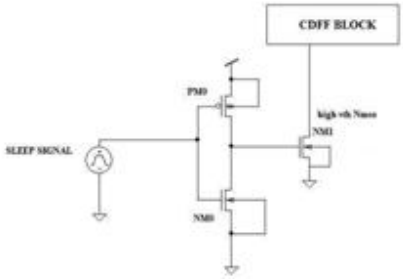


Fig. 5.CDFF-MT

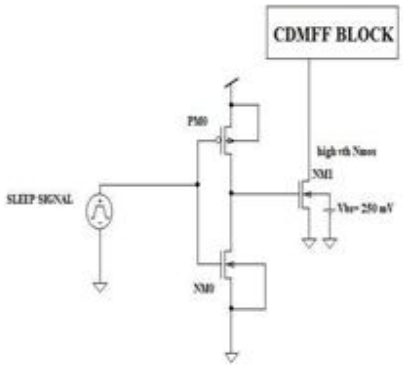


Fig. 6.CDMFF-MT

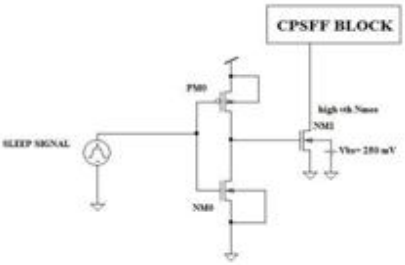


Fig. 7.CPSFF-MT

IV. SELF CONTROLLABLE VOLTAGE LEVEL (SVL) CIRCUIT

A self-controllable voltage level (SVL) circuit can supply a maximum dc voltage to an active load circuit or will decrease the dc voltage supplied to a load circuit in standby mode. There are three types of SVL circuit (Type1, Type2 and Type3) [9]. Type2 SVL has been applied to CDFF, CPSFF, and CDMFF and the power consumption has been reduced. Type2 SVL has a single nMos switch (n-SW) and *m* pMos switches (p-SW) connected in series. The lower SVL circuit supplies V_{ss} to active load through the ON n-SW and standby load circuit through weakly ON p-SWs. Load circuit is an inverter. When V_g is '0', NM0 is turned OFF and the drain-to-source voltage of this transistor is the function of voltage drop of *m* ON pMos switches in the lower SVL circuit. By increasing the voltage drop (V_p) by increasing the value of *m* will result in less drain-to-source voltage. Hence threshold voltage will rise which reduces the subthreshold current I_{stn} of the nMos at a gate- to- source voltage of 0V.

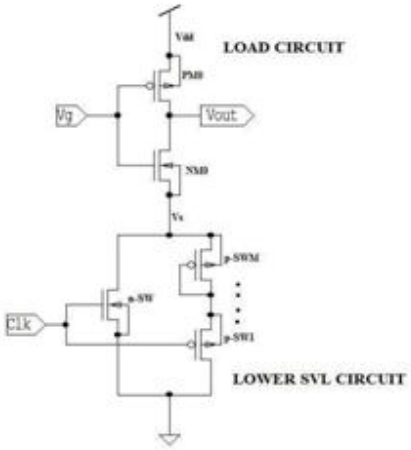
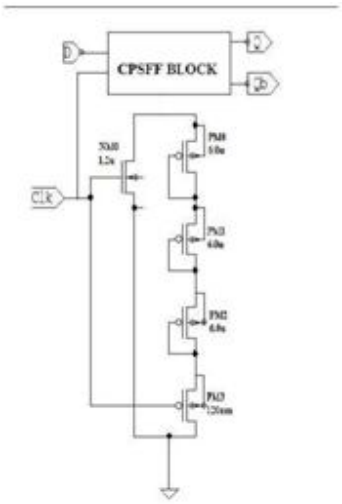


Fig. 8.Type2-SVL



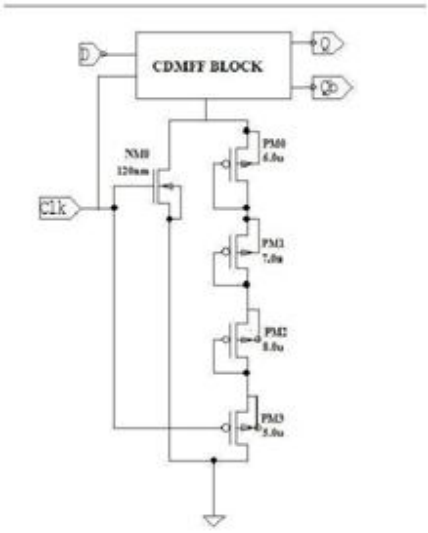


Fig. 9.CPSFF-SVL
Fig. 10.CDMFF-SVL

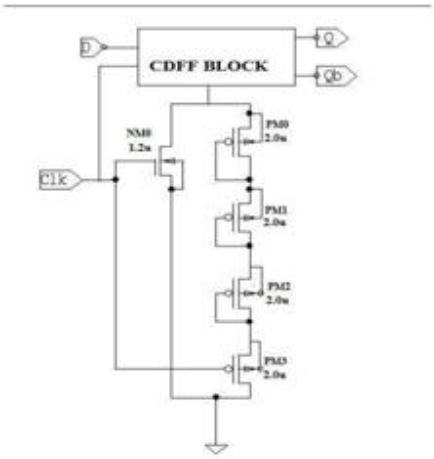


Fig. 11.CDFF-SVL

TABLE I: POWER CONSUMPTION COMPARISON FOR VARIOUS FLIP FLOPS AFTER APPLYING MTCMOS TECHNIQUE

LOGIC NAME	POWER WITHOUT MTCMOS TECHNIQUE (µW)	POWER WITH MTCMOS TECHNIQUE (µW)	LEAKGE POWER WITHOUT MT (nW)	LEAKGE POWER WITH MT (nW)
CPSFF	16.14	15.82	1.12	0.86
CDMFF	21.5	13.06	1.3	1.104
CDFF	59.33	56.22	30	29

TABLE II: POWER CONSUMPTION COMPARISON AFTER EMPLOYING SVL CIRCUIT

LOGIC NAME	POWER CONSUMPTION WITHOUT SVL (µW)	POWER CONSUMPTION WITH SVL LOGIC (µW)
CPSFF	16.14	13.6
CDMFF	21.5	20.3
CDFF	59.73	41.49

V. RESULTS

MTCMOS technique and SVL circuits have been applied successfully to flip flops and a greater reduction in the total power consumption is observed. All the circuits are

operating at 1 GHz and supply voltage is 1 V. Technology used is 45 nm. Circuits are designed and simulated using Cadence Virtuoso 6.1.5. MTCMOS technique can be successfully applied to any type of flip flops. CDMFF gives 39% power reduction after applying the technique. MTCMOS technique has cut down the power consumption to a greater extent. Major drawback of this technique is that there is data loss during SLEEP mode. A self-controllable voltage level (SVL) circuit can supply a maximum dc voltage to an active load circuit or will decrease the dc voltage supplied to a load circuit in standby mode. Self-controllable logic drastically reduces power without losing data in SLEEP mode. SVL circuits of type2 with m= 4 has given a tangible reduction in power. CPSFF gives 15.7% reduction in power with SVL circuit whereas CDMFF showed 3.33% reduction in power consumption. MTCMOS technique requires additional fabrication for High V_t transistors which is another disadvantage.

VI. ACKNOWLEDGMENT

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