Low Power 8-Bit Segmented Current Steering Digital-To-Analog Converter

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Abstract- *Data converters are important component of any electronic system. This paper presents the design of an 8-bit low power current steering. The lower 4 bits are decoded using binary decoder while upper 4 bits are decoded in parallel with lower 4 bits using thermometer decoding. Both are implemented using current cells. The op amp based I to V converter converts the total output current into analog voltage. Current cell is designed using current mirrors in cascode configuration. The final I to V converter is designed using op amp based difference amplifier. All the components of DAC are implemented in 90 nm TSMC CMOS technology using Cadence environment. The simulation results indicates DNL and INL less than ± 0.5 and power less than 5 mW.*

Keywords- Current steering, Low power, Segmentation, Current cell design.

I. INTRODUCTION

With advancement in Very Large Scale Integration (VLSI) technology has been made, many mixed-signal circuits have been implemented on a single chip (IC's). Data conversion circuits such as analog-to-digital converters (ADC's) and digital-to-analog converters (DAC's) are important component of any electronic system. ADC converts analog signal into digital signal while DAC converts digital data into analog signal. DACs are used in wide range of applications like Display Electronics, Data Acquisition Systems, Calibration Systems, Data Distribution Systems, Software radio, audio applications, communication and information systems etc.

This paper presents a novel architecture for 4 to n bit DAC, where n is an integer.The various architectures used for converting digital data into analog signal are resistor string DAC, R-2R resistor ladder DAC, Binary weighted resister DAC and capacitor DAC etc. These architectures converts digital input directly to analog output voltage. The architecture presented in this paper is based on current steering mode which generates a current proportional to digital input which is finally converted into analog voltage using op amp. This approach has found to be area, speed and power efficient with performance parameters INL and DNL to be half LSB.

The design presented here is an 8-bit segmented current steering DAC using 90 nm CMOS technology. The main features of the DAC design are discussed in the next sections. In Section II an overview of the DAC architecture is presented. In Section III,sub-circuits and its operations are described. Implementation details, integration, testing and results are given in Section V.

II. 8-BIT CURRENT STEERING DAC OVERVIEW

For the DAC presented, segmentation was used to obtain 4 thermometer encoded MSBs, and 4 binary weighted LSBs. The unit current cells are arranged in a matrix pattern as given in Figure 2.1. To control the current cells, two thermometer encoders are used. One decoder addresses the column and the other addresses the appropriate row in the current cell matrix. Since the segmentation for the MSBs is 4, the first three most significant bits (B6, B7) of the inputs are sent to the row encoder, the next three most significant inputs (B5, B4) are sent to the column encoder. With two digital inputs going to the encoder, 3 thermometer outputs are produced. By using this segmentation scheme the DAC has a 4×4 unit current cell matrix.

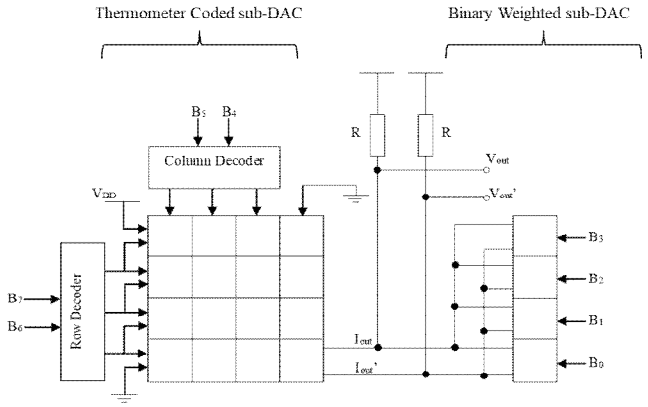

Figure 2.1: Internal Architecture of Proposed Current Steering DAC.

The four least significant bits (B3-B0) digital inputs are sent to the binary weighted sub-DAC. The binary weighted section contains four current cells producing the currents I, 2I, 4I, 8I. The output from the binary weighted sub-DAC is connected to the output from the thermometer encoded cells to produce the analog output. Two load resistors are connected to the positive and negative output terminals to convert the output current to voltage. The supply voltage is connected to one end of the load resistor while the current cells are connected with the other end of the resistor. As the current is drawn through the load resistor to the current cells a voltage is created. The final DAC output is found by subtracting the differential voltages Vout and Vout' using op amp.

The value of current cell is designed as follows: For this design of 8-bit DAC, the current value is specified as 5 µA as the Cadence Virtuoso tool with 90 nm technology gives minimum desirable W/L value for MOS. Total binary digital levels for 8-bit DAC = 28-1 = 255.So total output current through DAC = 255 × 5 µA = 1.275 µA. The total binary digital levels for lower 4 bit of binary coded DAC is 15 (23 + 22 + 21 + 20). So current through binary coded DAC is 75 µA (15 x 5 µA). And four current cells of Binary Weighted sub-DAC will have value 5 µA, 10 µA, 20 µA, 40 µA. The total binary digital levels for upper 4 bit of thermometer coded sub-DAC is 240 (24 + 25 + 26 + 27). So current through thermometer coded sub-DAC is 1.2 mA (240 x 5µA). As there are 15 current sources for a 4-bit DAC, the value for each cell will be 80 µA.

III. SUB-CIRCUIT DESIGN

The current steering architecture has several sub-components that need to be carefully designed. The key component is the current cell, which includes a differential pair of switches, and a current mirror to produce the reference current. The next set of components is the thermometer decoder, local decoders, register.

A.Binary to Thermometer Decoder

The decoder converts binary codes to thermometer ones. Thermometer code, so named because it is similar to a mercury thermometer, where the mercury column always rises to the appropriate temperature and no mercury is present above that temperature.

Table 3.1: Binary to Thermometer Truth Table.

Binary	Thermometer
A B	T_3 T_2 T_1
0 0	0 0 0
0 1	0 0 1
1 0	0 1 1
1 1	1 1 1

The Binary Code with a length of 2 can represent 2^2 – 1=3 Thermometer code.Table 1 gives its truth table which shows thermometer code changes only one bit at a time and the Boolean equations can be written as:

$$T_3 = A.B \quad (3.1)$$
$$T_2 = A \quad (3.2)$$
$$T_1 = A+B \quad (3.3)$$

Here, A is the most significant bit (MSB) and B is the least significant bit (LSB) of binary codes while T1 is LSB and T3 is MSB of thermometer codes.

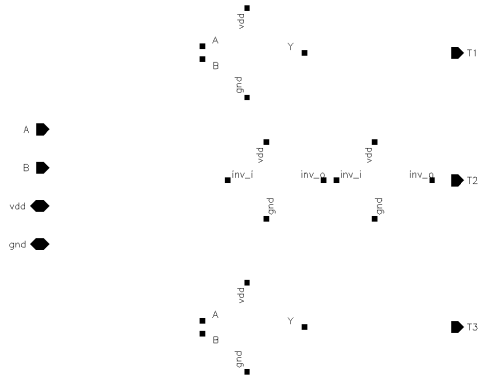

Figure 3.1: Schematic for Binary to Thermometer Decoder.

The schematic of this decoder is in Figure 3.1. Inverters are added to obtain similar delay time in T2 branch of the decoder's output while retain the same logic. In this design of DAC, two decoders are used one for row and another one for column.

B.Local Decoder

The local decoder receives outputs from the thermometer encoders. Each current cell is indexed by row i and column j. The local decoder consists of an OR and NAND gate with inputs rowi, rowi-1, and columnj. These are used to determine if the current cell should be turned on by checking, if the previous row is high and either the current column or the current row is high, current source should source current

through the positive output terminal (OUT = ROW_{N-1} AND (ROW_N OR COL_N)). Figure 3.2 shows schematic for Local Decoder.

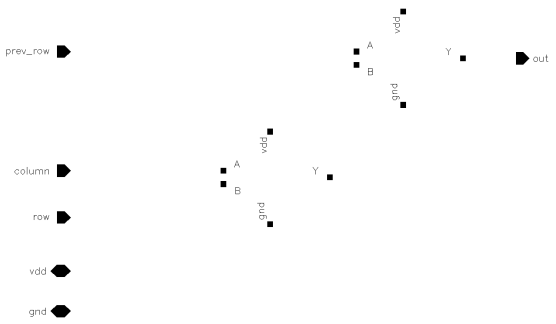

Figure 3.2: Schematic for Local Decoder.

The outputs from the local decoder are then sent to a master-slave latch to re-time all of the input signals.

C.Register

A master-slave latch is placed between the local decoder and the current cell switch transistors. This type of register consists of two cascaded D latches and an inverter placed in the clock path. The purpose of the register is to synchronize all the input signals so the current cell switches switch in unison. Since the current cell has differential outputs, the latch includes differential input and output. A simple latch can be created using cross coupled inverters. The latch used in this proposed system. Figure 3.3 shows schematic for register.

Figure 3.3: Schematic for Register for Switching Transistors.

The digital inputs are connected to a pair of pass gate transistors. These transistors are controlled by the clock. When the clock signal is high, the digital signals enter the latch. The cross coupled inverters form a feedback loop that holds the digital value. A set of inverters are placed at the end of each latch stage to boost the signal strength between the stages. The two latches are cascaded to create the master-slave flip flop. A rising edge flip flop design is used, which means the first stage is controlled when clock is “High” and the second stage is controlled when the clock is “Low”.

D.Current Source

Current cell is simply a current source implemented using MOS. The simplest design of the current source is a single MOS transistor biased with constant gate to source voltage that operates in saturation region. The architecture, shown in Figure 3.4, improves the performance by cascoding the current source transistor. This will greatly increase the output impedance and reduce the output capacitance of the current cell. The main disadvantage with the cascode current cell is that the area is increased, and the need for an additional bias voltage. The switching consists in two MOS transistors operating as switches with complementary gate signals.

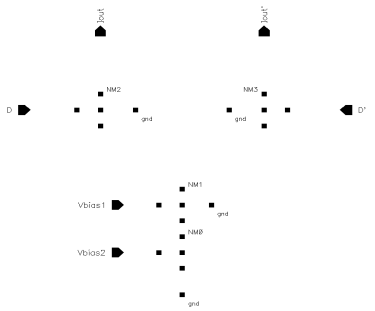

Figure 3.4: Schematic for Cascode Current Source.

Design procedure followed to design current source is as follows: Consider the current cell of 5 µA, as it is a value for LSB current cell. So the (W/L) found out by Equation (3.4) by neglecting □ effect.

$$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox} V_{OD}^2} \qquad (3.4)$$

As per the designed explained in Section II, the W/L for current cell of values 10 µA, 20 µA, 40 µA and 80 µA are calculated.

E.Current Source Bias

The simple method to bias current source is current mirror. The schematic for generating the current source bias voltage Vbias1 and Vbias2 is shown in Figure3.5. The width of transistors is designed for the minimum value of current cell which is done using Equation (3.4).

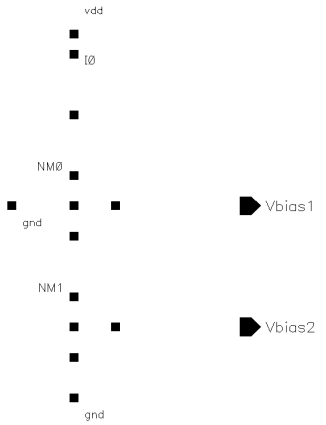

Figure 3.5: Schematic for Generating Current Source Bias Voltage.

F.Operational Amplifier as Difference Amplifier

The output of DAC is obtained by taking the difference between voltages which we get by passing the total current through resistors. To take this difference, Operational Amplifier is used. The Op-Amp is configured as difference amplifier as shown in Figure3.6.

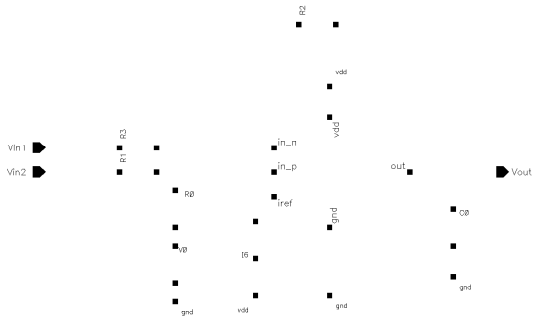

Figure 3.6: Difference Amplifier using Op-Amp.

The output voltages of current cells Vout and Vout' obtained by passing the current through resistor are applied as input to the difference amplifier. Then the voltage difference is amplified, whose gain is the ratio of two resistances. An Operational Amplifier is one of the important signal processing block in most of the electronics systems. It is characterized by very high open loop gain with high capacity to reject the common mode noise i.e. giving high CMRR. It can be configured in closed loop form for implementing many mathematical functions like addition, subtraction, etc. Besides it is used as comparator in open loop configuration. All active filters use op amp as one of the important building block. Figure 3.7 shows circuit for classical two stage op amp.

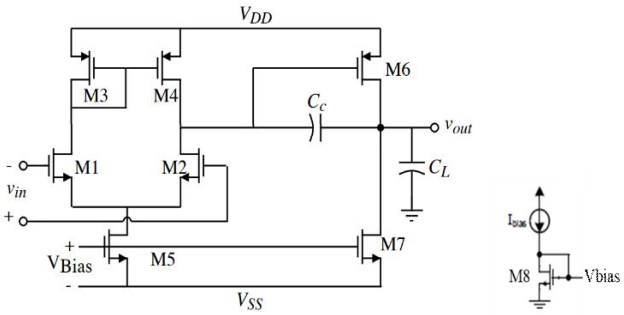

Figure 3.7 a) Circuit Configuration for Two Stage Operational Amplifier. b) Generation of Vbias Using Current Mirror.

The design procedure from Section 6.3 "CMOS Analog Circuit Design" by Phillip Allen is followed to achieve the required specifications.Table 3.3 gives comparison between required specification and simulated values. Which shows the op amp is well designed with the required specifications.

Table 3.3: Comparison between Required Specification and Simulated Value.

Specification	Actual required Value	Simulated Value
Open Loop Gain	> 70 dB	70.6 dB
Gain Bandwidth	> 30 MHz	30 MHz
Phase Margin	> 60°	74°
Cut-off Frequency	---	9.45 KHz
Slew Rate	20 V/µSec	32 V/µSec

IV. SYSTEM INTEGRATION, TESTING AND RESULTS

In this section a revision of the work developed and the results obtained in this project will be presented. Also the static performance, dynamic performance and power dissipation analysis will be presented. The simulation is done to test 4-bit Binary Weighted DAC, 4-bit Thermometer Coded DAC and 8-bit Segmented Current Steering DAC by giving all possible inputs. All the simulations are done using Cadence Virtuoso tool.

A. 4-bit Binary Weighted Current Steering DAC

Figure 4.1 shows schematic for 4 bit Binary Weighted Current Steering DAC. Input clock frequency is 10 MHz and the inputs are changing from 0000 to 1111. Here the values of current cells are 5 µA (I), 10 µA (2I), 20 µA (4I) and 40 µA (8I).

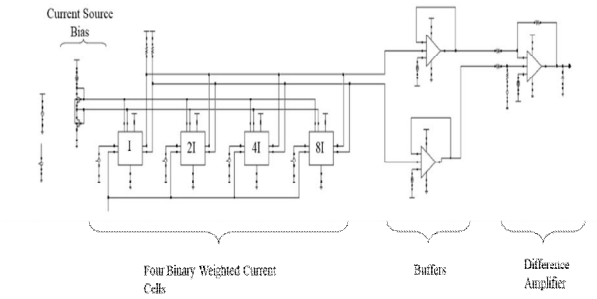

Figure 4.1: Schematic of 4-bit Binary Weighted Current Steering DAC.

Figure 4.2 shows enlarged output of DAC which shows 16 distinct voltage levels as input changing from 0000 to 1111.

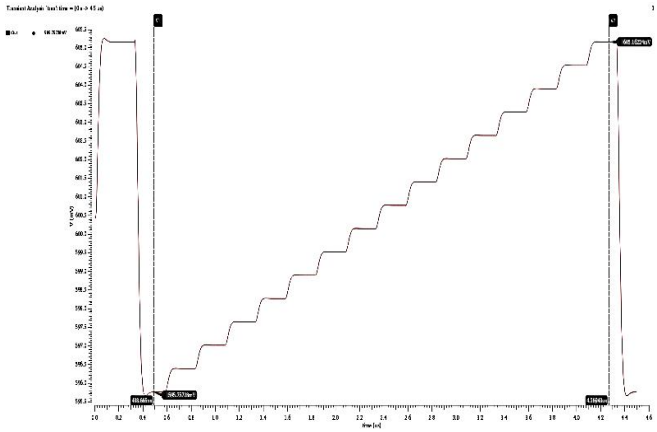

Figure 4.2: Enlarged Output of 4-bit Binary Weighted Current Steering DAC.

B. 4-bit Thermometer Coded Current Steering DAC

Figure 4.3 shows schematic for 4 bit Thermometer Coded Current Steering DAC. Input clock frequency is 10 MHz and the inputs are changing from 0000 to 1111. Here the current of each cell is 80 µA.

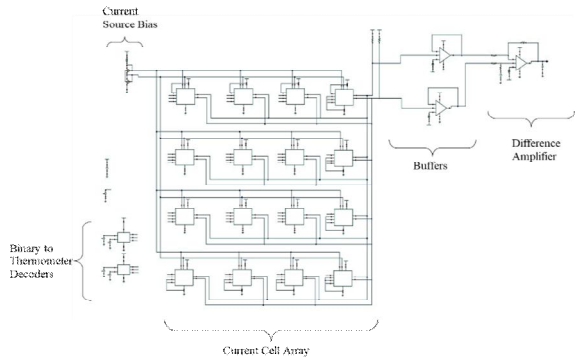

Figure 4.3: Schematic of 4-bit Thermometer Coded Current Steering DAC.

Figure 4.4 shows enlarged output of DAC which shows 16 distinct voltage levels as input changing from 0000 to 1111.

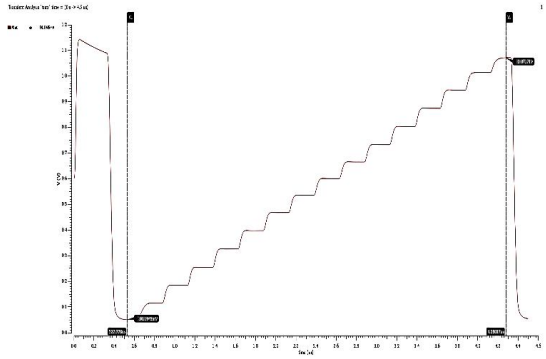

Figure 4.4: Enlarged Output of 4-bit Thermometer Coded Current Steering DAC.

C. 8-bit Segmented Current Steering DAC

Figure 4.5 shows schematic for 8-bit Segmented Current Steering DAC. Input clock frequency is 10 MHz and the inputs are changing from 00000000 to 11111111. This 8-bit segmented current steering DAC in build by using 4-bit Binary Weighted sub-DAC and 4-bit Thermometer Coded sub-DAC as explained in the Section 4A and 4B respectively.

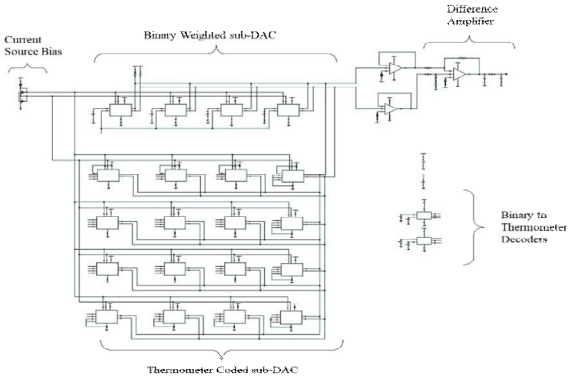

Figure 4.5: Schematic of 8-bit Segmented Current Steering DAC.

Figure 4.6 shows enlarged output of DAC which has 256 distinct voltage levels as input changing from 00000000 to 11111111.

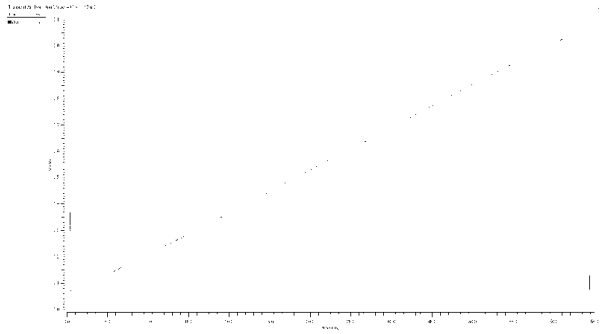

Figure 4.6: Enlarged Output of 8-bit Segmented Current Steering DAC.

D. Static Performance

The Table 4.1 shows the digital level and its corresponding analog voltage, INL and DNL. With the reference of Table 4.1, The DAC is seems to be monotonic.

Table 4.1: INL and DNL for Corresponding Voltage Level

Digital Level	Analog Voltage	DNL	INL
0	66.77	---	---
1	69.67	-0.271	-0.271
2	73.36	-0.0728	-0.3442
3	77.35	0.0025	-0.3417
4	81.31	0.00502	-0.3467
5	84.83	-0.1155	-0.4623
6	88.5	-0.1155	-0.54

E. Power Dissipation

The total power consumption of the DAC is measured to be 4.204 mW with an input frequency of 10 MHz.

F. Performance Comparison

The performance of this DAC is compared with some previous works by earlier researchers and is summarized in Table 4.2.

Table 4.2: Performance Comparison

	[6]	[7]	[13]	This Work
Technology	90 nm	130 nm	90 nm	90 nm
Resolution	10	8	12	8
Power Dissipation	43 mW	14.72 mW	128 mW	4.2 mW
DNL	0.02	---	0.5	-0.271
INL	0.29	---	1.2	-0.462

VI. CONCLUSION

The Current Steering mode saves the area, because if we look at conventional/ traditional DAC, it uses resistor which requires larger area than that of current source and also less power. Also the implementation of different current sources of different value is simple than implementing different valued resistance. And usage of active devices increases speed of DAC. The segmentation of bits between Binary Weighted and Thermometer current Steering DAC found helpful, because while implementing 8-bit DAC using the Binary Weighted current steering architecture requires large value current source and output gets affected by glitches. Whereas 8-bit DAC using Thermometer Coded current steering architecture reduces glitches at the output it requires more area. Also while taking difference of voltages at the load resistances directly by the op amp, it is observed that current flowing though the resistances is more than the expected values. This problem gets solved by putting the buffers between op amp and differential output. The proposed design of 8-bit Segmented Current Steering DAC operates at frequency of 10 MHz and low power of 4.202 mW. So the design is power efficient and it is suitable for industrial application.

REFERENCES

[1] ManthanSheth, Rushabh Mehta, "12-Bit, 1GHz Hybrid Current Steering DAC", *https://www.eeweb.com/project/rushabh_mehta/12-bit-digital-to-analog-converter*.

[2] Maruthi Chandrasekhar Bh, Dr. SudebDasgupta "A 1.2 Volt, 90nm, 16-bit Three Way Segmented Digital to Analog Converter (DAC) for Low Power Applications," *10th International Symposium on Quality Electronic Design, ISBN 978-1-4244-2953-0/09*, pp.447 - 450, 2009.

[3] Paolo Crippa, Claudio Turchetti, Massimo Conti, "A Statistical Methodology for the Design of High-Performance CMOS Current-Steering Digital-to-Analog Converters," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol.21, No.4, pp.377 - 394, April 2002.

[4] Maria Helena Casaca da Trindade, "A 7 bit 3.52 GHz Current Steering DAC for WiGig Applications", Instituto Superior Técnico, University of Lisbon, Portugal, June 2016.

[5] Benjamin Jankunas, "Design and Calibration of a 12-Bit Current-Steering DAC Using Data-Interleaving", Arizona State University, December 2014.

[6] Taylor J. Moody, "Design of a 10-bit 1.2 GS/s Digital-to-Analog Converter in 90 nm CMOS", B.S.E.E., Wright State University, 2015.

[7] Lijo Jose, A.M. Vijayaprakash, K.V. Kumaraswamy, "An 8-bit segmented current steering DAC for low power communication applications", *2016 International Conference on Emerging Technological Trends (ICETT) 978-1-5090-3751-3/16*, 2016.
[8] Philip E. Allen, Douglas R. Holberg, "CMOS Analog circuit design", Oxford, 2nd edition.
[9] https://www.youtube.com/watch?v=F2fCmRKGoCY&list =PLK2eyR1C9gjoBp61ZDvz6Zdd_6Hu7vZTz "Two Stage Op-amp Design in Cadence".
[10] Yang Lin, "Design of a 8-bit CMOS Unit-Element Current-Steering Digital-to-Analog Converter", University of Maine, 2008.
[11] Yannan Ren, Fule Li, Chun Zhang, Zhihua Wang, "A 400MS/s 10-bit Current-steering D/A Converter," *Institute of Microelectronics of Tsinghua University, Beijing, China, ISBN 978-4244-4888-3/09*,pp.533 – 536, 2009.
[12] Tan G.H., Surpajo B.S., Wagiran R., Sidek R., "The Design of 8-bit CMOS Digital To Analog Converter," ICSE2000 Proceedings,pp.231 - 234, Nov. 2000.
[13] Wei-Hsin Tseng, Chi-Wei Fan, and Jieh-Tsorng Wu. A 12-bit 1.25-gs/s dac in 90 nm cmos with 70 dbsfdr up to 500 mhz. Solid-State Circuits, IEEE Journal of, 46(12):2845–2856, 2011.