A Back Gated, Ultra Low Power, Better Phase Noise Voltage Control Oscillator For Multi-Standard Wireless Communication Protocol

Harshal Chauhan[1], Asst. Prof. Vinod Sonkar[2]
[1, 2] Dept of EC
[1, 2] SDBCT Indore

Abstract- *Since VCO is the important part for any receiver, it need to be design in such a way that it justify all the parameter such as low power consumption, low phase noise, tuning range, FOM. Low power consumption depends on low supply and current consumption by whole circuit. Low phase noise and FOM depend upon the transistor design, device size and tuning range depend on MOS varactor. It is very difficult to obtain low phase noise since it depends on quality factor and all the devices connected in the circuit and the value of inductor is chosen in such a way that it can generate require frequency range. So, in this thesis, VCO consist of eight transistor connected in compounded pair which in turn are connected in cross coupling. NMOS transistor is bulk bias to reduce the power consumption. This reduces the phase noise which is very important for any VCO. The whole circuit is working at 1.2 V supply which consume 3.9 mW of power. This VCO has frequency range of 5.0-7.35 GHz and is design for wireless standard communication protocol such as 802.11 a/g/n. This circuit achieve phase noise of -118.84 dBc/Hz and figure of merit of -197 dBc/Hz.*

Keywords- VCO, Phase Noise, FOM, Tuning Range, Low Power, Bulk Bias.

I. INTRODUCTION

VCO are widely used in instrumentation and communication systems. Technical evolution and market requirements demand for High frequency generation.vco are also used in pacemaker. A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by an input voltage.

In recent years, there has been a strong growth in the modern wireless data and voice communication standards in numerous frequency bands. Modern transceivers for the wireless communication consist of many building blocks, such as low-noise amplifiers (LNAs), mixers, frequency synthesizers (FS), filters and amplifiers. With the advancement of radio frequency (RF) technology and requirement for more integration, new RF wireless architectures are needed. There is a tremendous demand of mobile communication and wireless communication systems in today's modern life. This has placed certain limitations and requirements on the communication channel bandwidths and spacing. The modern wireless communication systems rely strongly on frequency conversion and switching of one frequency band to other frequency bands.

Frequency synthesizer is one of the most critical components in the wireless transceiver. It greatly affects the overall performance of the wireless transceiver system. Frequency synthesizers are commonly used as a local oscillator (LO) in the wireless transceivers for frequency translation and channel selection.

The key idea is to down convert the RF signal to the baseband signal and it is also known as direct conversion or zero-IF receiver.

To avoid the loss of information, the down conversion must provide quadrature outputs for the frequency and phase modulated signals. Therefore, frequency synthesizer requires the accurate quadrature signal generation from local oscillator (LO) . RF transceivers require quadrature signal and quadrature voltage controlled oscillator (QV CO) provides the best solution for the generation of the quadrature signal.

II. LITERATURE REVIEW

Dixit and his friends[15] demonstrate the difference between IMOS and DSB based LC VCO configuration. They have design LC VCO for 5-5.47 GHz oscillation frequency.they have also shown the design tradeoff to obtain better VCO.

Ji and friends[16] introduce self biased VCO in which push pull configuration with resistor is used. This method improves amplitude response and reduce tank loading.

This also reduce the need of choke inductor which require large space of chip. This circuit is implemented on 65nm.

Sadhu[17] achieved tuning range of 87.2 % by using switching inductor technique to design VCO with frequency from 3.3 to 8.4 GHz. Power consume by this design was 6.5 and 15.4 mW.

Hsu and his mates[18] show how to improve the phase noise of VCO and also shown Q enhancement technique. They design body biased VCO that help in reducing power consumption. This circuit is designed on 180 nm technology.

Zhou[19] designed dual band VCO for frequency range from 0.4-6 GHz that covers wireless standard such as WCDMA,GSM,Bluetooth and WLAN. They design this VCO on 130 nm technology which consume 34-77 mW of power.
Xiangning Fan and his friends[20] use switched capacitor array to extend the frequency range and output buffer to drive the output signal and prevent from external intereference. With this circuit arrangement , they achieved -108 dBc/Hz of phase noise at 1 MHz offset.

Mehrabian[21] use active inductor concept which is tuned with the help of active resistor and achieved tuning range of 3.8-7.4 GHz . with this design,-92.05 dBc/Hz of phase noise is obtained.

Hegazi[22] found that the phase noise can be increase by adding extra LC filter to the circuit. To prove this concept, he deisgned three VCO. Out of these three, two are working at 1.1 GHz and one at 2.1 GHz.

Sani and his friend[23] proposed cascade technique that allow current scalable design at low supply voltage, without dissipating extra power and without effecting output voltage swing.they have designed on 65 nm technology and 1 V supply is used.

Siddharth Bhat[24] use bulk driven technique in which input voltage is applied at the bulk of PMOS transistor. Input voltage range was 0-1 V and 0.4 V of supply is used. With this technique, whole circuit consume 350 µW.

III. THEORY

CMOS cross coupled topology has a NMOS cross coupled differential pair, LC tank and in addition to this a differential PMOS pair at top. This CMOS pair is used to achieve more positive gain for same power consumption. The CMOS cross coupled topology without or with tail are show in figure 3.1(a) and figure 3.1(b). The total negative resistance of CMOS pair which include parallel combination of NMOS pair's negative resistance R_{inn} and PMOS pair's negative resistance R_{inp} as show in figure 3.1(c). It express as

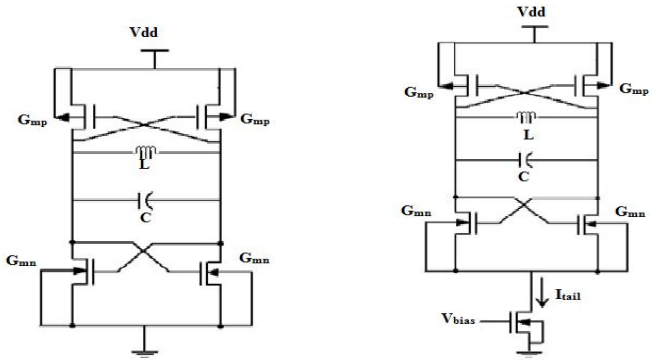
$$R_{negative} = R_{inn} // R_{inp} = \frac{2}{g_{mn}+g_{mp}}$$

It is know that phase noise is contributed by flicker noise of active devices. This active devices up convert this flicker noise in the phase noise region with slop -30dB/decade so called $1/f^3$ phase noise region. This noise can be minimized by equating rising and falling time of oscillation waveform. This condition can be achieved when NMOS and PMOS device has equal transconductance is express as:

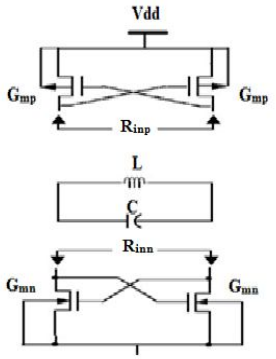
$$g_{mn} = g_{mp}$$

In this condition better rise and fall time symmetry achieve which reduces the up conversion of 1/f transistor noise. Therefore CMOS structure attains a smaller $1/f^3$ noise corner in noise characteristic which exist in NMOS cross coupled differential topology.

There are another advantage of CMOS cross coupled differential topology that it consume less current because for given biased current both NMOS and PMOS attain negative resistance so it is possible to compensate loss in LC tank with lower biased current than in NMOS only structure. The important advantage of CMOS cross coupled differential topology is that CMOS structure attains peak differential output amplitude twice as high NMOS only structure.



(a) **(b)**



(c)

Figure 3.1 (a) (a), (b) CMOS cross-coupled differential oscillator without and with tail current source and (c) calculation of total negative resistance of CMOS differential topology.

The CMOS cross coupled differential topology also experience drawbacks over cross coupled differential topology. The first disadvantage of CMOS cross coupled topology is that this topology offers higher parasitic capacitance which mean lower tuning range. This because the parasitic capacitance contributed by PMOS pair may as high as five times the parasitic capacitance contributed by NMOS pair of cross coupled differential topology.

Second disadvantage is arises when tail current source incorporated with CMOS cross coupled differential topology as show in figure.

Another thing is bulk driven concept. The principle of the bulk-driven technique is that the input is given on the body that is less than the threshold voltage and a voltage is being set on the gate terminal so as to form a channel. The thickness of the depletion zone i.e. the conduction channel is affected by the bulk voltage. A bulk-driven symmetrical OTA operating in weak inversion can result in both reduced power consumption and high linearity.

Bulk-driven MOSFET was first adopted in [12]. While designing an OTA while adopting the bulk-driven technique, the most significant stage is the input stage. In this technique, a fixed voltage is associated with the gate terminal and the input is given into the bulk terminal. With the zero-bias voltage on the bulk terminal, the transistors are in weak inversion. The two fundamental favorable circumstances of utilizing the bulk-driven system are that the bulk- driven differential sets in an OTA and incredibly enhances the transconductance and the threshold voltage of the transistor vanishes and both negative and positive bias voltages (Vbs) are conceivable. Whereas there are a couple of downsides to this technique when contrasted with the gate driven method, for example, little transconductance due to the less input capacitance of the depletion layer and larger parasitic capacitance to the mass which diminishes the fT. Due to the smaller transconductane, the device will have high input referred noise. The advantage of a Bulk-driven device over a gate-driven device is that the threshold voltage limitation disappears and both positive and negative bias voltages (Vbs) are possible. This is especially important in analog low-voltage circuits where the dynamic range of the signal should be maximized with respect to the supply voltage in order to maximize the performance of the circuit.

Finally compounded transistor pair technique is used. This technique increase output impedance and transconductance. Figure 3.2 shows compound transistor pair which is used in this project.

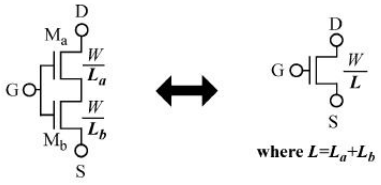


Figure 3.2 Compound transistor pair[23]

IV. DESIGN

4.1 Inductor Design

The inductor used in this thesis were realized in an iterative fashion for an intended use in cross-coupled CMOS LC oscillators. The primary objective in the design process was to design inductors to support the oscillator's operating frequency of RF band. A tank circuit with C_{max}/C_{min} is 0.94pF/0.46pF and L = 1 nH exhibits centre frequency for design is 6 GHz. These obtain centre frequency for design is different from theoretical frequency due to parasitic effect of MOS transistor.

4.2 Varactor Design

The aim for varactor design is to achieve desired range of tuning frequency for LC tank. The tank circuit capacitance is associated with variable varactor capacitance and fixed parasitic capacitance related to inductor and amplifier which limit the tuning range. This PMOS capacitance is implemented by connecting two identical PMOS transistor in series which operate in inversion mode. The varactor has a maximum capacitance 0.94 pF and a minimum capacitance of 0.46 pF. It provides tuning range of

2.35GHz for frequency range 5 GHz-7.35GHz. The PMOS varactor has dimension width,(W) = 8 um, channel length, (L) = 200nm and number of multiplier, (M) = 50.

4.3 L in parallel with C

Figure 5.1 shows the proposed design with high value capacitor is connected in parallel with the current source and shunts the second harmonic noises of the current to the ground. In addition, to provide high impedance and at the same time resonate the parasitic of the current source at the second harmonic (2*fo*) a source inductor is implemented connecting the current source with the cross-coupled transistors[22]. So, L is chosen as 1nH and C is calculated 0.7 pF on the basis of frequency 6 GHz.

V. RESULTS &COMPARISION

5.1Tabulation of Parameters extracted

CMOS LC VCO design has very low power consumption. The low value of power is obtained due to implementation of cross coupled pair of PMOS transistor in design of LC VCO. This design of CMOS LC VCO has very optimized tuning range. The two PMOS are connected back to back and biased in inversion mode in design. The results are summarized in Table 5.1.

Table 5.1
(A) Results of CMOS LC VCO.

S.No.	Parameter	Simulation result	
1.	Technology	45nm	
2.	Power Consumption(mW)	3.9	
3.	Frequency(GHz)	5-7.35	
4.	Tuning Voltage(V)	0.0-1.2	
5.	Tuning Range (%)	39.2	
6.	Phase Noise(dBc/Hz)	@1MHz offset	-118.84
7.	FOM(dBc/Hz)	-197 @1 MHz	

5.2 Phase Noise & Figure of Merit(FOM)

Fig. 5.1 shows that the phase noise at an offset of 1MHz is -118.84 dBc/Hz, respectively.

FOM of the proposed VCO is -197 dBc/Hz/ at 1 MHz offset from 6 GHz operating frequency that is better than other reported works.

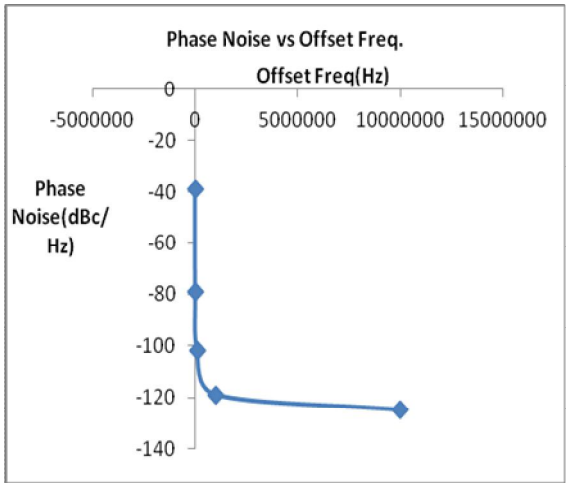


Fig.5.1 Relationship between Phase Noise and Offset freq.

VI. CONCLUSION

Bulk bias LC VCO is shown which is working on 45 nm technology and at 1.2 V supply. In this, a PMOS and a NMOS on both side is added in addition to conventional circuit. 0.1 V is applied at the body of NMOS transistor which reduce's the power consumption to 3.9 mW. This VCO generating frequency from 5 GHz to 7.35 GHz which makes this circuit good candidate for multistandard wireless communication protocol.

With this technique, -118.84 dBc/Hz of phase noise and FOM of -197 dBc/Hz is obtained.

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