Design And Development Of Multilevel Inverter To Improve Power Quality

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Abstract- *H-bridge inverter is capable of generating multilevel output voltage of more fundamental RMS output voltage with less amount of THD.This paper mainly discusses control of H-bridge cascaded multilevel inverter by control circuit and how it can be compensate THD and Triplen harmonic.*

This paper present a single phase cascaded H-bridge multilevel inverter. Cascaded multilevel inverter requires 'N' H-bridge circuit and dc source for '2N+1'level of output voltage. This multilevel inverter comprises a six power MOS-FET in each H-bridge circuit. Switching of power MOS controlled by microcontroller through opto-isolator. Reduction in THD and improve the output voltage and current waveform quality of inverter is achieved by increasing the output stepped voltage level of inverter.

Keywords- Cascaded H-bridge multilevel inverter (CHMLI), Total harmonic distortion (THD), Pulse width modulation (PWM).

I. INTRODUCTION

In area of power conversion application, an inverter plays a vital role. The increase in use of power electronic based devices leads to unwanted harmonics in the power systems which disturb the power quality and life of equipment. Development in multilevel inverter technologies has become very important alternatives in power system. Research is going on to improve performance, optimised control techniques, reduce component count and manufacturing cost. There are several types of topologies have been developed for multilevel inverter system by manufacturer to increase the output levels, reduce component count, number of independent dc source, voltage stresses, losses. The most commonly used topologies are cascaded H-bridge, flying capacitor, diode clamped.

This paper presents cascaded H-bridge multilevel inverter topology. CHMLI requires 'n' H-bridge and dc source for 2n+1 voltage output level. Switching of each power MOS controlled by microcontroller through opto-isolator. Control circuit and power circuit isolated by opto-isolator. Quality of output voltage waveform of CHMLI determines how much close in shape of waveform to required sine wave. Quality of output waveform of CHMLI can be improved by increasing the number of output voltage level.

This paper is organised in following manner. Section II presents block wise description of Cascaded H-bridge multilevel inverter Section III presents the actual design of circuit and operation mode of CHMLI.In section IV conclusion are summarised.

II. BLOCK DIAGRAM AND DESCRIPTION.

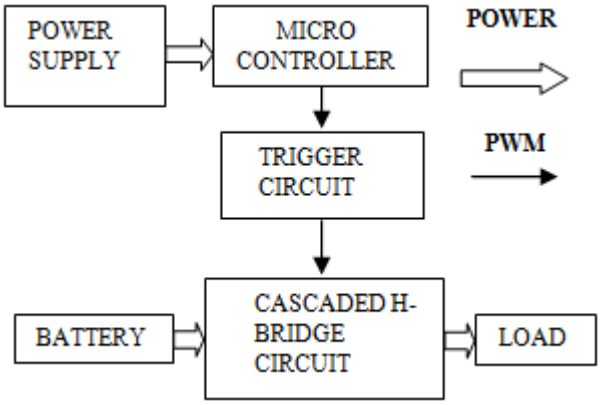

Fig 2[A]: Block diagram of CHMLI and Control Circuit.

Fig 2[A] is the block diagram and control circuits of single phase CHMLI shown. Each cascaded circuit powered by individual battery source in inverter. Output of CHMLI given to the Single phase load. There are Eight Power MOS-FET used in each H-bridge circuit and switching of MOS controlled by microcontroller through opto isolator.Seperate power supply designed for control and trigger circuit. Opto-isolator isolates power and control circuit. Synchronized switching strategy obtained by microcontroller to generate stepped power frequency output voltage.

III. CIRCUIT CONFIGURATION AND OPERATING MODE OF FIVE LEVEL CASCADED H-BRIDGES MULTILEVEL INVERTER.

Fig 3[A] single phase five level CHMLI shows. Two isolated input Dc source Vdc1 and Vdc2 consist in single phase CHMLI.There is eight power MOS-FET switches (P-channel and N-channel) which denoted by

S1,S2,S3,S4,S5,S6,S7 and S8.There is four switches in each H-bridge circuit.V1,V2 and V0 denotes output stepped voltage of First H-bridge, Second H-bridge and 5 level single phase CHMLI respectively. I*(0)* indicate load current. There is no need of feedback diode in H-bridge circuit.

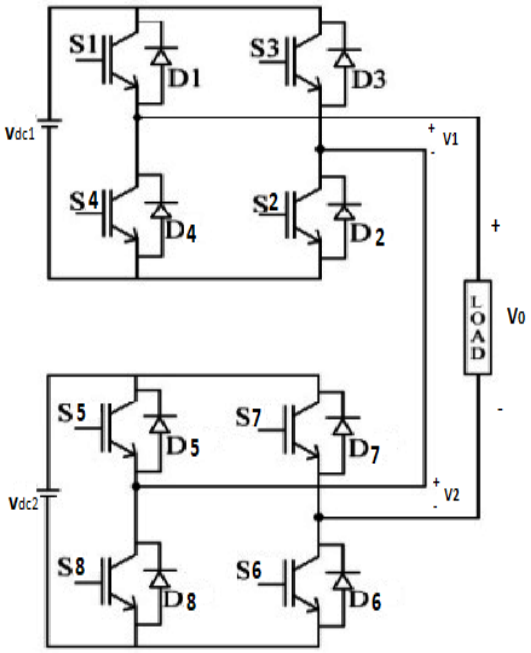

Fig 3[A]: Single phase 5 level cascaded H-bridge multilevel inverter.

Fig 3[B] shows detailed output stepped voltage waveform of single phase CHMLI.There are five level of output stepped voltage waveform consist of 0,+e1,+e2,-e1,-e2.T2 is output voltage time period.

The two H-bridge circuit are connected in cascade in such manner that synthesized total output stepped voltage waveform is the sum of two individual H-bridge circuit output.

Output voltage of circuit is,

$$V0=V1 + V2 \quad \text{--- (1)}$$

Where,
V0=Total output voltage.
V1=first H-Bridge circuit output voltage.
V2=second H-Bridge circuit output voltage.

There are total six different mode of operation of single phase five level CHMLI inverter. There are five levels of output voltage waveform consist of 0, +e1, +e2,-e1,-e2.

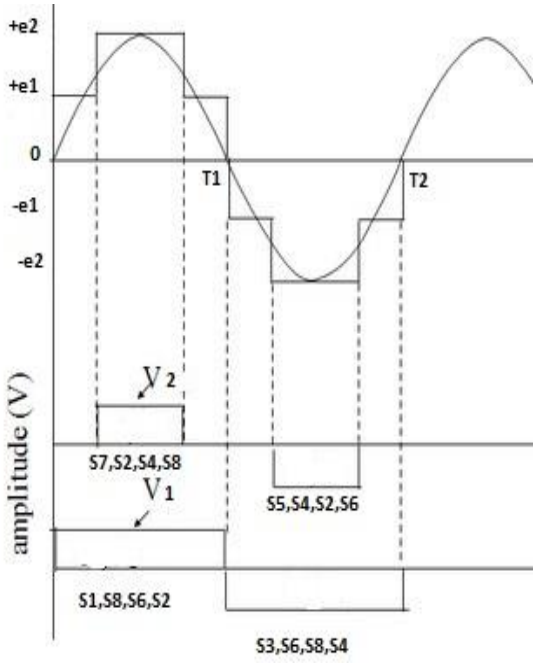

Fig 3[B]: output stepped voltage waveform of single phase cascaded H-bridge multilevel inverter.

Modes of operation are explained below:

Mode 1:

In mode 1, switches S1 to S8 are turned OFF. Dc voltage Source is not connected to load.

Mode 2:

In mode 2, switches S1, S8, S6 and S2 are turned ON. Dc voltage Source is connected to load. Output voltage across the load is +e1.

Mode 3:

In mode 3, switches S1, S8, S7 and S2 are turned ON. Dc voltage Source is connected to load. Output voltage across load is +e2.

Mode 4:

In mode 4, switches S1 to S8 are turned OFF. Dc voltage Source is not connected to load. Output voltage across the voltage is zero.

Mode 5:

In mode 5, switches S3, S6, S8 and S4 are turned ON. Dc voltage Source is connected to load. Output stepped voltage across load is -e1.

Mode 6:

In mode 6, switches S3, S6, S7 and S2 are turned ON. Dc voltage Source is connected to load. Output stepped voltage across load is –e2.

A] *THD MEASUREMENT*:

The total harmonic distortion (THD) measurement represents the harmonic distortion present in an output stepped voltage and current waveform of CHMLI inverter. The total harmonic distortion in output waveform of inverter with respect to pure sin wave measured by power quality analyzer or THD analyzer.

The staircase output voltage waveform of CHMLI becomes more sinusoidal as the number of output voltage levels of increases. In Five level inverter THD is less as compared to Three level inverter. In Seven level inverter the THD is less as compared to Five level and Three level inverter.

IV. CONCLUSION

By using the single phase cascaded H-bridge techniques for multilevel inverter is studied. Analysis of different level is compared. From analysis THD is decreasing if the number of output level goes on increasing and improve the output stepped voltage and current waveform quality.

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