Reconfigurable Cordic Architecture For Rectangular To Polar Conversion

Minakshi Dahake[1].(VLSI) Student), Asst. Prof. Amol Boke[2]
[1, 2]Dept of Electronics & communication
[1, 2] GHRAET

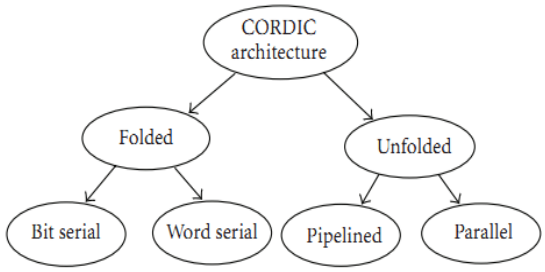
Abstract- *Fixed-angle-rotation operation of vectors is widely used in signal processing, robotics, and graphics. Various opti- mized coordinate rotation digital computer (CORDIC) designs have been proposed for uniform rotation of vectors through known and specified angles. CORDIC (Coordinate Rotation DIgital Computer) is an iterative algorithm which is used to calculate mathematical functions such as trigonometric, hyperbolic, exponential functions and so on. A fully parameterized hardware is presented that allows for extensive exploration of the resources-accuracy design space, from which we generate optimal realizations. CORDIC it can perform several computing tasks such as the calculation of trigonometric, hyperbolic and logarithmic functions, real and complex multiplications, division, square-root, solution of linear systems, eigenvalue estimation, singular value decomposition, QR factorization and many others. As a consequence, CORDIC has been utilized for applications in diverse areas such as signal and image processing, communication systems, robotics and 3-D graphics apart from general scientific and technical computation. In this article, we present a brief overview of the key developments in the CORDIC algorithms and architectures along with their potential and upcoming applications.*

Keywords- CORDIC algorithms, trigonometric function, Xillinx And pipelined CORDIC architecture.

I. INTRODUCTION

The coordinate rotation digital computer (CORDIC) algorithm involves a simple shift-add iterative procedure to perform several computing tasks by operating in either rotation-mode or vectoring-mode following any one among linear, hyperbolic, and circular trajectories [1]. Applications such as singular value decomposition, eigenvalue estimations, QR decomposition, phase and frequency estimations, synchronization in digital receivers, 3-D graphics processor, and interpolators require the CORDIC to operate in both rotation and vectoring-modes. The 3-D structures such as hyperboloids, paraboloids, and ellipsoids require the CORDIC to be operated in both circular and hyperbolic trajectories. The hardware implementation of these applications requires more than one CORDIC processor operating in different modes and different trajectories. A reconfigurable CORDIC, which can operate in rotation and vectoring-modes, for both circular and hyperbolic trajectories can replace multiple CORDIC processors, and would be highly useful for such applications. A reconfigurable CORDIC can be utilized for a variety of applications in communication systems, signal processing, 3-D graphics, robotics apart from general scientific calculations, and waveform generations.

In the last five decades, several algorithms have been proposed for area-delay-efficient and power-efficient implementation of CORDIC algorithms, either for circular trajectory [2]–[7] or for hyperbolic trajectory [8]–[10]. But, we do not find any systematic study on design and implementation of reconfigurable CORDIC in the existing literature. A basic design of reconfigurable CORDIC based on a unified CORDIC algorithm [11] has been proposed recently [12]. The reconfigurable design of [12] is found to involve high reconfiguration overhead and results in low hardware utilization efficiency.



Taxonomy of CORDIC architectures.

Fig 1. Figure show the Taxonomy of cordic architecture

In general, the architectures can be broadly classified as folded and unfolded as shown in Figure 4, based upon the realization of the three iterative equations (6). Folded architectures are obtained by duplicating each of the difference equations of the CORDIC algorithm into hardware and time multiplexing all the iterations into a single functional unit. Folding provides a means for trading area for time in signal processing architectures. The folded architectures can be categorized into bit-serial and word-serial architectures depending on whether the functional unit implements the logic for one bit or one word of each iteration of the CORDIC algorithm. The CORDIC algorithm has traditionally been

implemented using bit serial architecture with all iterations executed in the same hardware [3]. This slows down the computational device and hence, is not suitable for high speed implementation. The word serial architecture [7, 48] is an iterative CORDIC architecture obtained by realizing the iteration equations (6). In this architecture, the shifters are modified in each iteration to cause the desired shift for the iteration. The appropriate elementary angles, αi are accessed from a lookup table. The most dominating speed factors during the iterations of word serial architecture are carry/borrow propagate addition/subtraction and variable shifting operations, rendering the conventional CORDIC [7] implementation slow for high speed applications. These drawbacks were overcome by unfolding the iteration process [1], so that each of the processing elements always perform the same iteration as shown in Figure 5.Themain advantage of the unfolded pipelined architecture compared to folded architecture is high throughput due to the hard- wired shifts rather than time and area consuming barrel shifters and elimination of ROM. It may be noted that the pipelined architecture offers throughput improvement by a factor of n for n-bit precision at the expense of increasing the hardware by a factor less than n. Block diagram of CORDIC Processer is (CorProc)

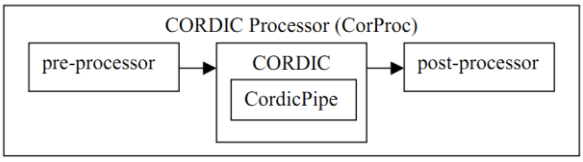


Fig 2. Figure show the Block Diagram of CORDIC Process.

The implementation of CORDIC algorithm has evolved over the years to suit varying requirements of applications from conventional non-redundant to redundant nature. The unfolded implementation with redundant arithmetic initiated the efforts to address high latency in conventional CORDIC. Subsequently, several modifications have been proposed for redundant CORDIC algorithm to achieve reduction in iteration delay, latency, area and power. The evolution of the unfolded rotational CORDIC algorithms is shown in Figure 6. As this taxonomy is fairly rich, the remainder of the review presents taxonomy in top-down approach.

CORDIC is broadly classified as non-redundant CORDIC and redundant CORDIC based on the number system being employed. The major drawback of the conventional CORDIC algorithm [3, 7] was low throughput and high latency due to the carry propagate adder used for the implementation of iterative equations. This contradicted the simplicity and novelty of the CORDIC algorithm attracting the attention of several researchers to device methods to increase the speed of execution. The obvious solution is to reduce the time for each iteration or the number of iterations or both. The redundant arithmetic has been employed to reduce the time for each iteration of the conventional CORDIC. We have analyzed and presented in the following Sections, features of different pipelined and non-pipelined unfolded implementations of the rotational CORDIC.

II. LITERATURE REVIEW

PIPELINED CORDIC ARCHITECTURE AND ITS IMPLEMENTATION ON SIMULINK [1] 3rd IEEE International Conference on "Computational Intelligence and Communication Technology" (IEEE-CICT 2017)

Coordinate Rotation Digital Computer (CORDIC) algorithm is very useful algorithm for the designing of low cost and efficient VLSI circuit's at large scale. It may be suitable for the generation of trigonometric functions, multiplication of complex numbers, matrix inversion and finding the solution of linear equations. The CORDIC algorithm has also been employed in calculation of sine and cosine values. The sine & cosine values are used in various transform of Digital Signal processing like z transform and in communication system. There are different ways to generate the sin & cosine values. These conventional methods require a huge memory space. A good quantization level is required for large memory. So CORDIC algorithm based sine & cosine waves' generation has been used because its flexibility characteristics and low quantization error. In this paper some pipelined CORDIC structures are presented for generation of sine and cosine values, multiplication, division of two numbers and finding out square root or arctangent values. These structures have been implemented and results observed by using Simulink of MATLAB.

An Enhanced Mixed-Scaling-Rotation CORDIC algorithm with Weighted Amplifying Factor [2] 2016 IEEE International Conference on VLSI and signal processing

Mixed Scaling Rotation Coordinate Rotational Digital Computer (MSR-CORDIC) algorithm has found its application in the areas where the rotation angles are known beforehand. The algorithm merges the micro-rotation and scaling operations resulting in the elimination of the overhead caused by the scaling operation. Through this paper, an improved MSR-CORDIC algorithm is proposed. This algorithm provides higher signal-to-quantization-noise ratio (SQNR) performance while preserving the features offered by the original MSR-CORDIC algorithm. The novelty of the paper lies in redefining the amplifying factor by multiplying the rotational sequences to the corresponding signed-power-

of-two (SPT) terms. The proposed algorithm offers a better alternative to MSR-CORDIC without additional hardware complexity.

A Floating-point FFT Twiddle Factor Implementation Based on Adaptive Angle Recoding CORDIC [3] 2017 International Conference on Recent Advances in Signal Processing, Telecommunications & Computing (SigTelCom)

In this paper, a single-precision floating-point FFT Twiddle Factor (TF) implementation is proposed. The architecture is based on Adaptive Angle Recoding CORDIC (AARC) algorithm. The TF design is built and verified on Altera Stratix IV FPGA chip and 65nm SOTB synthesis. The FPGA implementation has 103.9 MHz maximum frequency, throughput result of 16.966 Mega-Sample per second (MSps), and resources utilization of 7, 747 ALUTs and 625 registers. On the other hand, the SOTB synthesis has 16, 858 standard cells on an area of 86, 718um^2, 166 MHz maximum frequency, and the speed of 27.107 MSps. The accuracy results are 1.133E - 10 Mean-Square-Error (MSE) and about 26 part-per-million (ppm) maximum error-ratio

III. PROCESS AND CONVERSION FOR RECTANGULAR TO POLAR USING CORDIC

3.1 Add/Sub Block Diagram

The proposed architecture carried out makes use of n iterations to produce the final value of the function upto an accuracy of n bits. A two's complement 4- bit carry-look ahead adder/subtractor block with carry-save has been implemented as part of the architecture for greater speed. An 8-bit barrel shifter has been implemented for use in the algorithm. An optimum use of edge- -triggered latches and an intelligent clocking scheme has been designed to reduce the number of transistors involved. The iterative sequencing of steps requires a 3-bit counter and a clocking control

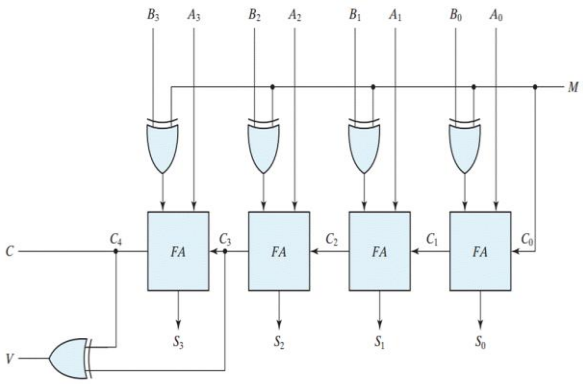


Fig 3. Figure show the Add-Sub block diagram

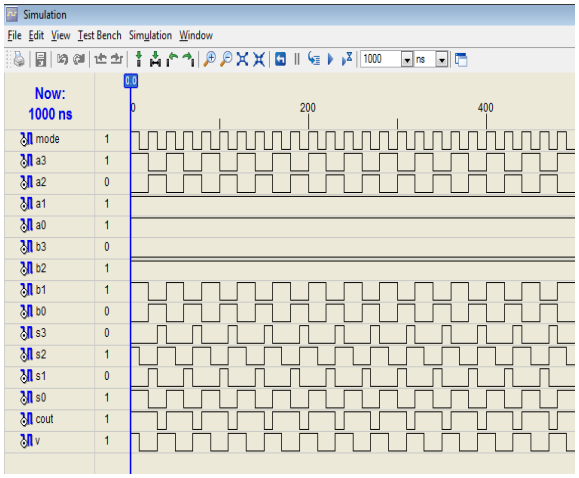


Fig 4. Figure show the simulation of Add-Sub block diagram -triggered latches and an intelligent clocking scheme has been designed to reduce the number of transistors involved. The iterative sequencing of steps requires a 3-bit counter and a clocking control scheme which has been implemented in this project. The CORDIC algorithm requires a certain set of fixed values to be accessed during the implementation of the iterative series of steps. A read-only-memory (ROM) block has been designed for this purpose and can be accessed through a 3-bit address bus whose bits are set by the outputs of the 3-bit counter.

3.2 Conversion using CORDIC Structure.

CORDIC (for Coordinate Rotation Digital Computer), also known as Volder's algorithm, is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions, typically converging with one

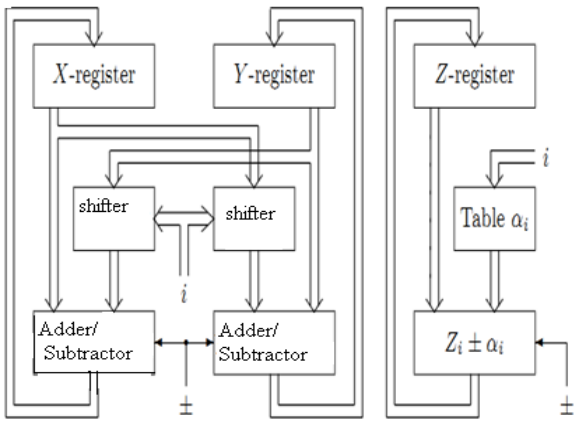


Fig 5. Figure show the CORDIC structure.

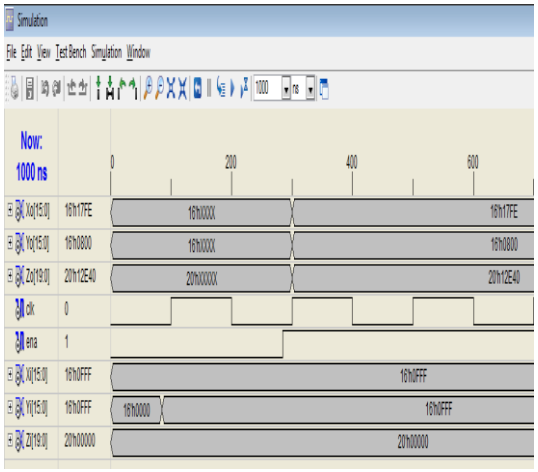


Fig 6. Figure show the simulation of CORDIC structure.

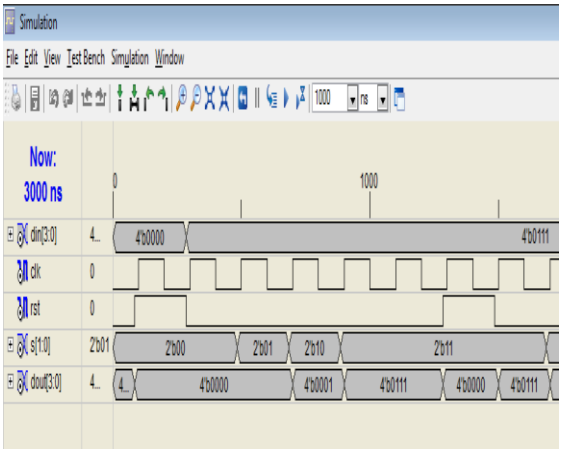


Fig 8. Figure show the simulation of shift register.

digit (or bit) per iteration. It is therefore also a prominent example of digit-by-digit algorithms. CORDIC and closely related methods known as pseudo-multiplication and pseudo division or factor combining are commonly used when no hardware multiplier is available (e.g. in simple microcontrollers and FPGAs), as the only operations it requires are addition, subtraction, bitshift and table lookup. As such, they belong to the class of shift-and-add algorithms.

3.3 Conversion using Shift Register.

CORDIC is a method for computing elementary functions using minimal hardware

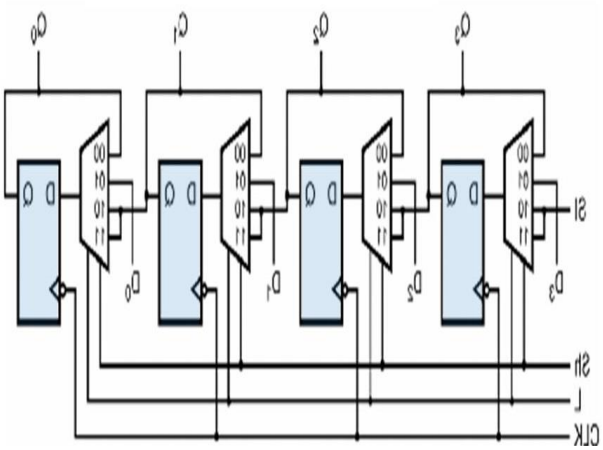


Fig 7. Figure show the shift register.

such as shifts adds/subs and compares. CORDIC works by rotating the coordinate system through constant angles until the angle is reduces to zero. The angle offsets are selected such that the operations on X and Y are only shifts and adds. Instead of using Calculus based methods such as polynomial or rational functional approximation, it uses simple shift, add, subtract and table look-up operations to achieve this objective. It is usually implemented in either Rotation mode or Vectoring Mode.

3.4 CORDIC Pipeline Method.

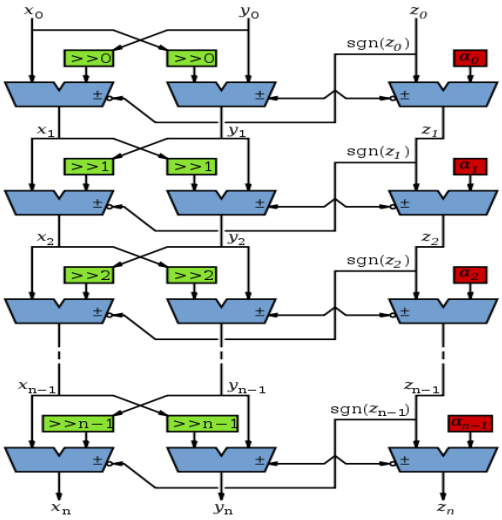


Fig 9. Figure show the CORDIC Pipeline

Coordinate Rotation Digital Computer (CORDIC) was an efficient algorithm to compute elementary arithmetic such as multiplication, division, and root extractions. However, conventional CORDIC algorithm requires high latency to obtain the results. This paper proposes a low latency parallel pipeline CORDIC (PP-CORDIC) to calculate trigonometric functions. The results show that PP-CORDIC can operate at 83.64 MHz frequency with the latency was 10,

15, and 17 clock cycles in the best, average, and worst case, respectively. The hardware architecture occupies 7,035 LUTs, and 3,409 registers on Stratix IV FPGA.

IV. RESULTS

CORDIC core performs the CORDIC algorithm on the input data sent by the pre-processor. It contains various pipelined stages for better performance. The stage performs single iteration step. It contains arc tan table for each iteration and the logic for handling the X, Y, A, R values.

Area Report

Area report, power report and Time reports are showing in below figure. Fig show the comparison of previous paper and these paper calculated result in show in table.

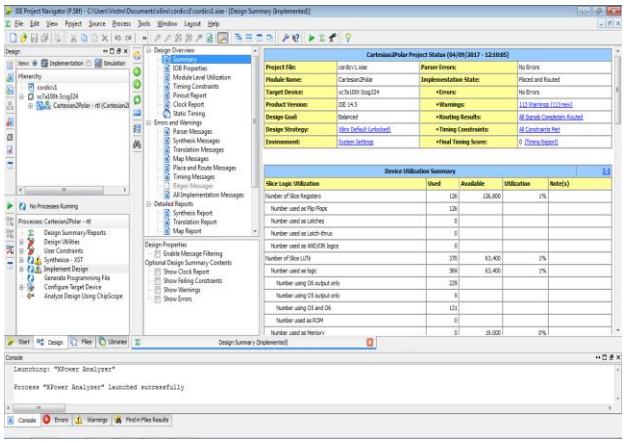


Fig 10. Figure show the Result of Area report.

Timing Report

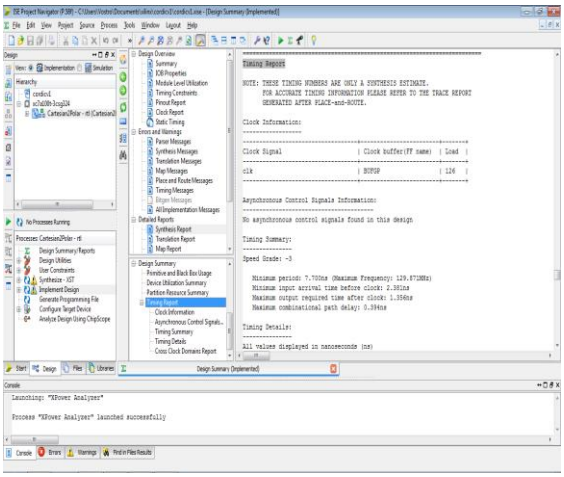


Fig 11. Figure show the Result of Time report.

Power Report

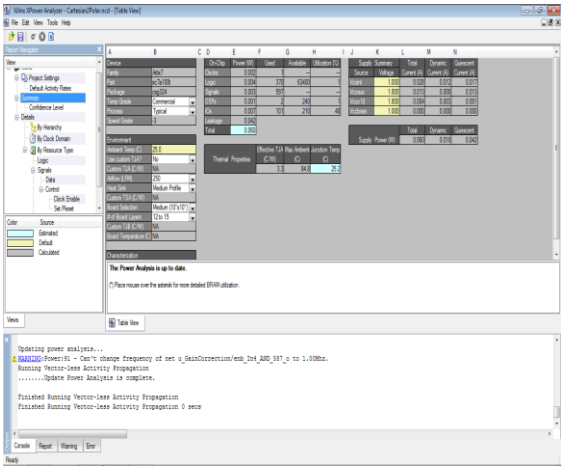


Fig 12. Figure show the Result of Power report.

Final Results

Fig 13. Figure show the Result of previous paper observation.

	2016 ieee khare	2016 iee hong	2016 ieee tiwari	2011 ieee aggarwal	present work
Area (SR)	180	472	76	375	126
Area (LUT)	1095	651	173	2293	370
Power (mW)	na	na	58	na	60
Freq (MHz)	202	84	10	56	126

V. OBSERVATION

The outcomes of the proposed work is

1. RTL description of CORDIC processor
2. Design verification using testbench based simulation results
3. Area, speed, and power results
4. Modification of original design by pipelining.
5. Frequency adjustment to achieve improved power consumption

VI. CONCLUSION AND FUTURE SCOPE

CORDIC is a powerful algorithm, and a popular algorithm of choice when it comes to various Digital Signal Processing applications. Implementation of a CORDIC based processor on FPGA gives us a powerful mechanism of implementing complex computations on a platform that provides a lot of resources and flexibility at a relatively lesser cost. Further, since the algorithm is simple and efficient the design and VLSI implementation of a CORDIC based processor is easily achievable.

In this paper a CORDIC module is designed and simulated using Xilinx ISE using VHDL as a synthesis tool. The output of the CORDIC core is analyzed and verified on the test-bench. This module is subsequently used for the design and simulation of 8-point 2D DCT processor. Finally the DCT processor was implemented on a Spartan 3E FPGA kit. The device utilization summary showed that minimum resources were consumed. The power analysis showed that very less power was consumed during the operation.

The future scope should include the implementation of CORDIC algorithm for higher order DCT systems, DCT computation and simulation for more number of points, implementation and simulation for DHT and DST calculations.

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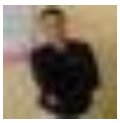
BIOGRAPHIES

Ms. Minakshi. D. Dahake received the B.E degree in Electronics Engg in the year 2015 from RTMNU, Nagpur, India. She is currently doing M.Tech. Degree in (VLSI) from GHRAET, Nagpur, India. She has published Review Paper On CORDIC Algorithm To Make It Self Power in IRJET. Her areas off interest is in VLSI.



Mr. Amol Boke completed her BE, in Electronics and Communication Engineering, from MIET College ,Gondia. and M.Tech in Embedded Engineering from S.R.M University Kattankulathur. He is currently working as Asst. Professor (Electronics & communication Engg) at GHRAET, Nagpur (India). He is having more than 4 Years Teaching Experience. He has published 11 papers in International journal, 1 papers in international conferences