Implementation Of Two Phase Clocked Adiabatic Static Cmos Logic Full Adder Design For Efficient Power Dissipation

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Abstract- *An efficient power dissipation with Adiabatic logic using 2 phase adiabatic static CMOS logic (2PASCL) has been presented. In this research work adiabatic logic is mainly used to minimize the energy loss during the operation of the circuit. The Adiabatic circuits are low power circuits, which performs the "Reversible Logic" to conserve energy and it gives the efficient power dissipation. The Full Adder plays an important role in many arithmetic operations such as adder, multiplier, divider and Processor. This paper proposes a 2PASCL Full Adder using Adiabatic logic, it follows the principle of Adiabatic Switching and Energy Recovery. Normally, Full adder represents the three inputs and two outputs. The proposed 2PASCL Full Adder has been simulated by 125nm technology using tanner EDA tool. The average power dissipation and transistor count has been reduced by using this technique.*

Keywords- Adiabatic logic, Energy recovery, Full Adder, Power dissipation, 2PASCL

I. INTRODUCTION

The power dissipation is a crucial concern in the design of VLSI circuits with increasing package density and working speed. Many low power design methods have been developed to reduce the CMOS digital circuit power consumption. However the adiabatic circuit is an attractive way to obtain extremely low power level in which the conventional CMOS digital circuit can't reach the low power level [1]. At present there are lots of digital systems are embattled to portable and battery-operated systems, so the power dissipation is one of the major design constraints in low power.

To reduce the power dissipation in major circuits, the circuit designer designed a circuit which is used to minimize the switching events, decreases the node capacitance, reduce the voltage swing, or to apply a combination of all of these methods. In all these cases, the energy drawn from the power supply is used only once before being degenerated. To increase the energy efficiency of the logic circuit, other measures can be introduced for recycling the energy drained from the power supply [3]. A narrative class of logic circuits are designed to increase the energy level technique called Adiabatic Logic[2]. This technique offers the possibility of further reducing the energy dissipated during switching events, and the possibility of recycling or reusing, some of the energy drawn from the power supply.

The Proposed Adiabatic technique of two phase clocked adiabatic static CMOS logic(2PASCL)[4] circuit is used to achieve the low power dissipation. This method used for reducing the power dissipation in 2PASCL circuit involves the design of a charging part without using diodes. In such case, during charging the current flows through the transistor. Thus, the 2PASCL circuit is different from other diode-based adiabatic circuits in which the current flows through both the diode and transistor. By using the 2PASCL circuit, we can achieve high output amplitudes and reduces the power dissipation. In 2PASCL technique, we use split level sinusoidal driving voltage to reduce the Power Consumption. The 2PASCL Full Adder consists of three inputs and two outputs. The outputs are followed by the sum and carry of the circuits.

II. CMOS LOGIC

In CMOS inverter the drain of PMOS and NMOS circuit is connected to the output terminal and the gate is connected to both of the input terminal. The source terminal of the PMOS circuit is connected to the supply voltage, and the source terminal of the NMOS circuit is connected to the ground [5]. The CMOS inverter diagram is shown in Figure 1.

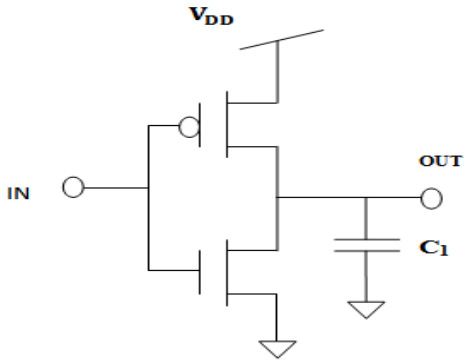

Figure 1.CMOS Logic circuit

Power dissipation in conventional CMOS circuit is due to device switching activity of the circuit. When the input is low PMOS attains ON state and NMOS attains OFF state. Hence, the direct path supply exist between supply voltage and output load capacitance. This stage is said to charging stage [2].

$$E_{charge} = (1/2)\, C_1L\, Vdd_2 \qquad (1)$$

If input is high PMOS reaches OFF state and NMOS reaches ON state. So, there is no supply between supply voltage and output load capacitance. When the charging state attains high level then the output of the load capacitance starts to discharge continuously [6].

$$E_{discharge} = (1/2)\, C_1L\, Vdd_2 \qquad (2)$$

The total amount of energy dissipated during charging and discharging is given by:

$$E=E_{charge}+E_{discharge}= C_1LVdd_2 \qquad (3)$$

III. ADIABATIC LOGIC

In Adiabatic logic the charging process of capacitor 'C_1' is connected series with resistance 'R_1' by using the constant current supply for charging the load capacitor [7]. The starting stage of the voltage capacitor will be zero. 'R_1' is said to be resistance and 'C_1' is said to be capacitor and Vc is said to be voltage across capacitor as shown in the Fig.2.
The charge of capacitor at time T is given by

$$Q = C_1V_c\,(t) \qquad (4)$$

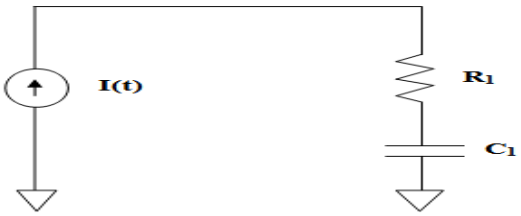

Figure 2. Adiabatic Logic circuit

During the time period '0' to 'T' the current remains constant. So, the energy dissipation is given by

$$E_{dissipation} = R_1I^2(t)\, dt \qquad (5)$$

$$=R_1I^2(t)\, T \qquad (6)$$

The constant current is said to be :

I(t) = Q / T , From equation (4)

$$I(t) =C_1V / T \qquad (7)$$

Substituting the value of I(t) from equation (7) from equation (6)

$$E_{dissipation} = R_1\,(C_1V/T)^2\, T$$

$$=(R_1C_1/T)C_1V^2 \qquad (8)$$

Where $E_{dissipation}$ is the total energy dissipate during the charging.

IV. TWO PHASE CLOCKED ADIABATIC STATIC CMOS FULL ADDER LOGIC

CIRCUIT STRUCTURE

Fig. 3 shows a circuit diagram of 2PASCL logic. A two-diode circuit is used—where one diode is placed between the output node and power clock, and the other diode is placed adjacent to the nMOS logic circuit and connected to another power source. Both of the MOSFET diodes are used to recycle the charges from the output node and to improve the discharging speed of the internal signal nodes. Such a circuit is designed particularly advantageous to all of the low power design circuits.

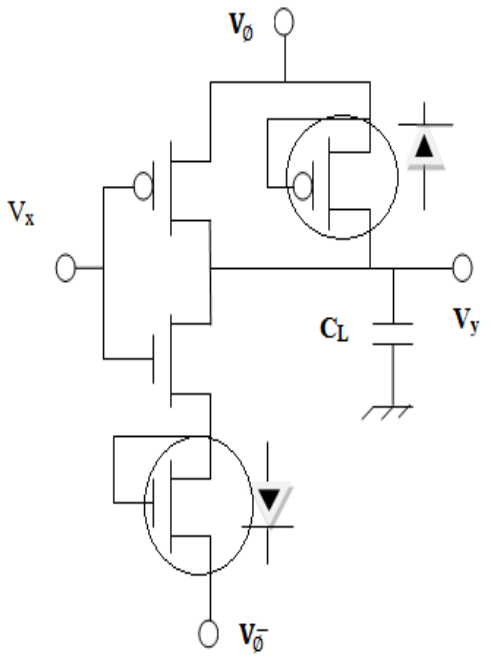

Figure 3. The 2PASCL Adiabatic Logic

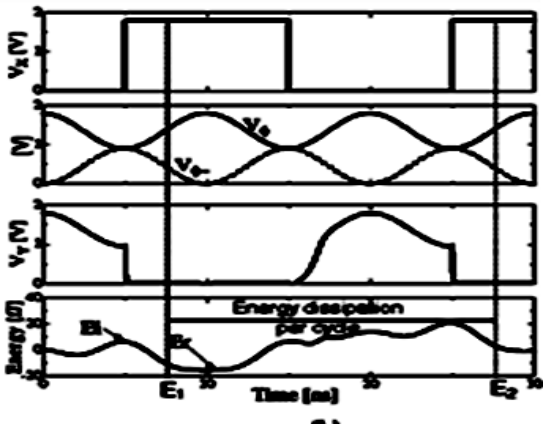

Figure 4. The Simulated waveforms of 4-inverter chain

Figure 4 shows the waveforms illustrating the operation of the 2PASCL 4-inverter chain logic. The transition frequency X=50 MHz, $V\varphi=V\varphi$ =100 MHz. The last graph shows the energy injected from the clock generator to EI and the energy that received back from the circuit capacitance ER; therefore the energy dissipated at each transition is only (EI – ER). If the signal nodes are preceded by a long chain of switches. The proposed system uses a two-phase clocking split level sinusoidal power supply, where in the V φ and V φ replace Vdd and Vss, respectively. One clock is presented in phase whereas while the other is inverted. The voltage level of V φ exceeds that of V φ by a factor of V dd/2. By using these two split-level sinusoidal waveforms, which have peak to peak voltages of 0.9 V, the voltage difference between the current-carrying electrodes can be minimized; and consequently, power consumption can also be suppressed. The substrates of the pMOS and nMOS transistors are connected to V φ and V φ , respectively[8].

Since the criteria for maintaining thermal equilibrium the voltage between the current-carrying electrodes is zero when the transistors are in the ON state [11] are satisfied, the energy accumulated in CL is not dissipated.

Thus the results of the simulation performed using a "simulation program with an integrated circuit emphasis (SPICE)" circuit simulator reveal that adiabatic circuits powered by the split-level sinusoidal waveforms consume less energy than a trapezoidal-waveform clock power supply, even when the rise and fall times of the trapezoidal waveforms are set to their maximum values. Moreover, sinusoidal waveforms can be generated with higher energy efficiency than trapezoidal waveforms [10].

CIRCUIT OPERATION

The circuit operation is divided into two phases: *evaluation* and *hold*, as illustrated in Fig. 10. In the *evaluation* phase, V φ swings up and V φ swings down. On the other hand, in the *hold* phase, V φ swings up and V φ swings down. Let us consider the inverter logic circuit demonstrated in Fig..5 The operation of the 2PASCL inverter is explained as follows:

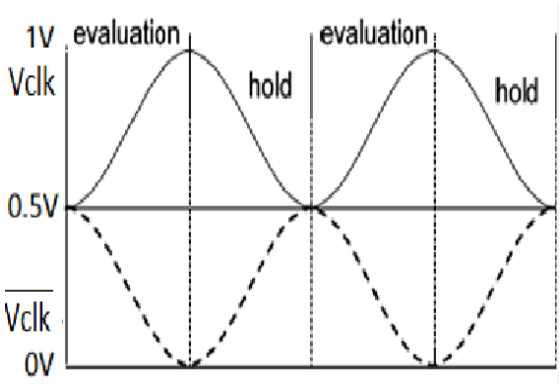

Figure 5. Power clocks in 2PASCL

1) *Evaluation* phase:

a) When the output node Y is said to be 0, the pMOS tree is turned ON, CL is charged through the pMOS transistor; hence, the output is in the HIGH state.
b) When node Y is said to be 0 and nMOS is ON, no transition occurs.
c) When the output node is said to be 1, the pMOS is ON, no transition occurs.

d) When node Y is said to be 1, the nMOS is ON, discharging via nMOS and D2 causes the logic state of the output to be "0" [12].

2) *Hold* phase:

a) When node Y is said to be 0 , the nMOS is ON, no transition occurs.
b) At the point when the preliminary state of the output node is said to be 1, the pMOS is ON, discharging via D1 occurs. The number of dynamic switching transitions occurring during the operation of the 2PASCL circuit decreases since the charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Hence, node switching activities are suppressed to a significant extent, and consequently, power dissipation is also reduced.

V. THE PROPOSED FULL ADDER USING 2PASCL LOGIC

The proposed full adder is being designed using two phase adiabatic static CMOS logic which uses the Split level technology to reduce the power consumption and high amplitude [13]. The system uses a two-phase clocking split-level sinusoidal power supply, wherein clock ($\overline{CLK}$) and clock bar (CLK) replaced by Vdd and Vss, respectively. One clock is placed in phase and the other clock is inverted.

The main aim is to reduce the power consumption which is useful in the upcoming technology.

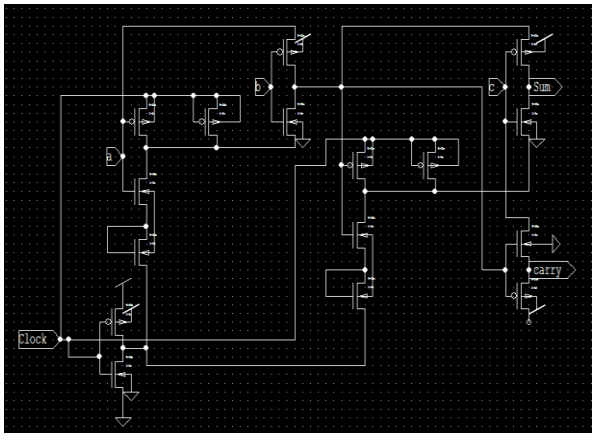

Figure 6. Proposed 2PASCL Full Adder Logic circuit

The basic sum and carry equations are implemented on the bases of P-MOS and N-MOS transistor[9]. And based on the above operation the output is produced separately. Figure 6 consists of 16 transistors that is the inputs are taken as a, b, & c and the outputs are considered as sum and carry.

VI. RESULTS AND DISCUSSION

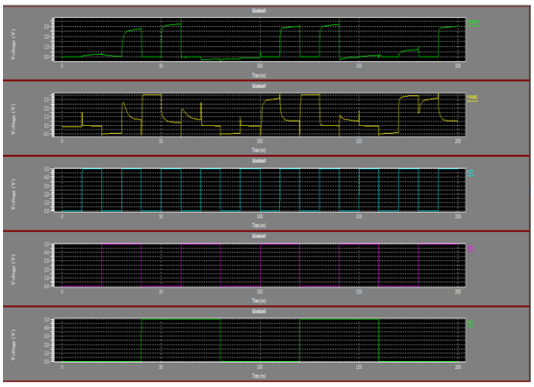

Figure 7. Simulation result for proposed 2PASCL Logic circuit

Figure 7 shows the simulated result for 2PASCL full adder. The input values are based on the truth table of full adder for example the value assigned for 1st bit 2PASCL based full adder is when A=0,B=0,C=0 where the obtained output is Sum=0,Carry=0. Based on this operation the obtained average power is 14.15µw.

The 2PASCL logic gives the better performance in terms of average power dissipation and less delay. Further, by using this technique transistor count can also be minimized

VII. CONCLUSION

The motive is to reduce the power consumption of the circuit in fast growing technology. The proposed full adder of two-phase clocked adiabatic CMOS logic (2PASCL) gives the less power dissipation. The simulation results shows that the average power is dissipated in the circuit. For instance, when the input frequency is simulated using the frequency values from 1 to 100 MHz, the 2PASCL inverter logic dissipates minimally only 21% of the power dissipated by a static CMOS in 4-inverter chain logic circuit. Then the proposed adiabatic logic has less power dissipation of 14.15uw and efficient energy recovery process.

In future, the 2PASCL Full Adder is applied to microprocessors for reducing power dissipation.

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