Power Reduction Using Pulsed Latch Method In Lookahead Clock Gating Technique

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Abstract- *Clock gating is one of the most vital techniques for reducing dynamic power in the sequential circuits where presence of clock signal at undesired instance is a major problem. The major power consuming components in electronics product is the systems clock signal and it is responsible for transition state of the components and this typically leads to the switching power consumption. The two clock gating techniques (Look Ahead Clock Gating (LACG) and Data driven Clock gating) are selected for possible optimization of power consumption in the register file. By comparing both the techniques LACG optimizes low power when compared to data driven clock gating. Multibit method and Pulsed latch methods are introduced with LACG and implemented on the chosen register file for experimentation. Among the two, LACG with the pulsed latch method is found to consume low dynamic power. Experimental results are simulated using MODELSIM Tool and power consumption is analyzed in Xilinx tool. The output shows that the lookahead clock gating technique significantly improves total dynamic power consumption in the chosen register file.*

Keywords- dynamic power, clock gating, cell, latch, flip-flop, LACG, data driven, auto gated flipflop, low power consumption, sequential circuits.

I. INTRODUCTION

The popularity of portable electronic products, low power system has attracted more attention in recent years. The major concerning factor in VLSI circuit is to achieve low power and small size battery with longer life. The important two components that describe power consumption in CMOS circuit are static power and dynamic power. The static power is considered during the standby operation for battery powered and they are due to sub threshold leakage, drain junction leakage and gate leakage due to tunneling. The dynamic power is due to charging and discharging of capacitor, short circuit and flip-flops transition state in the circuit. There are several techniques to reduce power consumption in VLSI circuits; some techniques are power gating, clock gating, adiabatic technique, etc,. Clock gating is one of the most common techniques used for power optimization. The technique used for better optimization and efficiency in clock gating technique is RTL clock gating and they are implemented in system level, gate level and RTL level.

II. CLOCK GATING

The clock gating technique requires an extra logic to generate a clock enabling signal and this will be enabled only when they attain logic 0 or 1 value according to the circuit design, which leads to reduction in power as well as area. The major objective of clock gating technique is to prevent unwanted clock pulses given to the circuit where there will be no change in the output. In registers, the clock consumes more power because of its toggling nature and their logic. And also in flip flop due to transition between 0 to 1 and 1 to 0 the switching activity is increased and they consume more power. First thing to implement clock gating is that to find a best place to use the technique and to create logic to turn off and turn on clock enabling signal. The term clock enabling signal is, when there is no activity at a particular register or flip flop there is no need of clock pulse for that circuit. The dynamic power dissipation is mainly due to change in flip flops transition state between 0 to 1 and 1 to 0. By reducing the switching activity of the flip flop the change in state is reduced so that the area is also gradually reduced. And the simple way is to cut off the idle clock pulses for those circuits in sequential circuit. By this, the power consumption is reduced and similarly this leads to reduction in area.

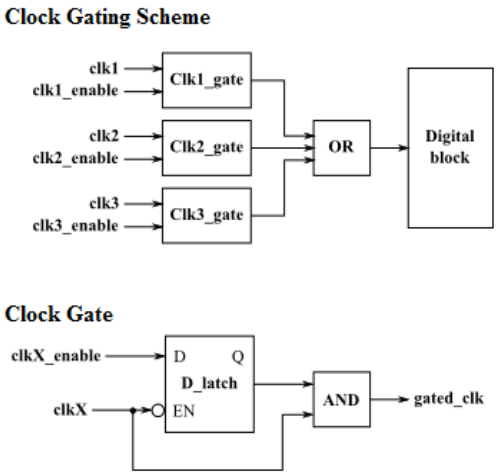

Figure 1: Clock gating technique

The figure 1 describes the simple clock gating technique. In first circuit many clock gating module are used and they require individual clock signal and enable signal for processing. This increases the area and power consumption because each individual module consumes more power by using separate clock signal and enable signal. And they are given to OR gate, OR gates sums the given data and they are given to digital circuit. Whereas the second circuit is compact and less components are used which decreases the power consumed by the components and area is reduced. The second circuit requires only one clock pulse and one enable signal and they are given to AND gate by this the clock activity is reduced.

III. CLOCK GATING TECHNIQUES

In modern VLSI circuits the power utilized by the clock signals has a major part of the whole design. Hence several methodologies have been proposed to reduce the dynamic power consumption in VLSI circuits. The clock gating techniques taken for experimental work is Lookahead clock gating (LACG) and Data driven clock gating in the register file. Both the techniques are implemented in register file and the best optimized technique is implemented with two methods multi-bit and pulsed latch method.

a. Register file
b. Lookahead clock gating in register file
c. Data driven clock gating in register file
d. Lookahead clock gating in register file with multi-bit flipflop method
e. Lookahead clock gating in register file with pulsed latch method

a. REGISTER FILE

The register file in a processor engine acts as an array implemented by using static RAM with multiple ports in central processing unit as shown in figure 2. The data path is generated for whole system by register file. The data can be chosen by any register then stored back into any other register in the register file all in a single clock cycle. Register files can be clubbed together as a register bank and some of the processors have several register banks. The register files have one word line per entry port, one bit line per bit of width per read port and two bit lines per bit of width per write port. Individual VDD and VSS are created for each of the bit cell. This increases the wire pitch area as the transistor size and the square number of ports increases in the system.

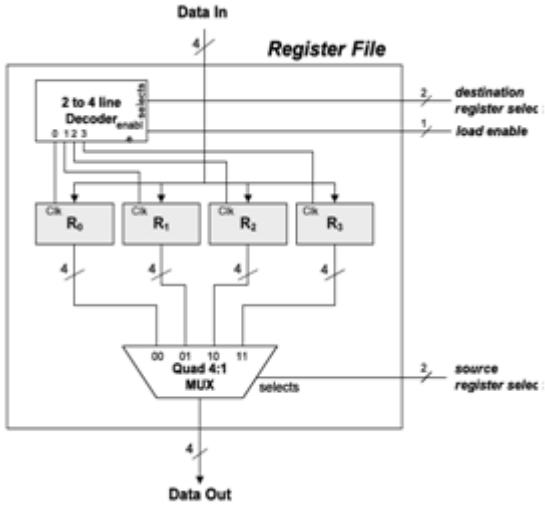

Figure 2: Register file

A quad 4:1 mux allows external data to be inserted into the data path. By that the data can be transferred between any two registers of our register file and that can be loaded with external data. The four registers R0, R1, R2 and R3 in the figure gets the input signal from 2 to 4 decoder. The four registers are designed with four positive edge triggered D flip flop and from that registers the selected register alone will allow the data to the 4:1 mux. For the four registers the clock input is commonly given as clock (clk).

b. LOOKAHEAD CLOCK GATING TECHNIQUE IN REGISTER FILE

Lookahead clock gating techniques is shown in figure 3 and implemented in register file for experimental process using VHDL code. Lookahead clock gating moves a step forward by taking Autogated flipflop (AFF) as a basic circuit addressing goals.

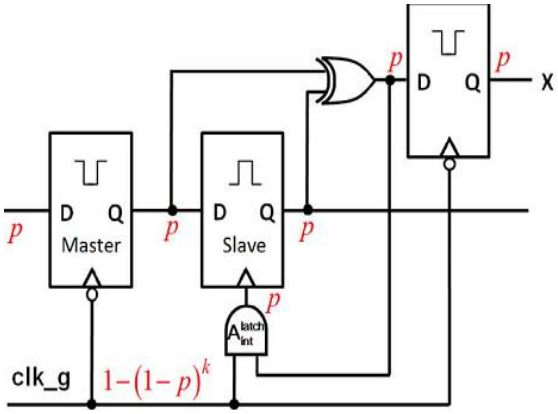

Figure 3: LACG in register file

In AFF the clock pulse is blocked only in the slave latch and no limitation is applied for master latch but in LACG the limitation of clock signal is applied to master latch. LACG is based on how XOR output is generated for clock enabling signals for other flipflops in the circuits that data depends on the flipflop. The XOR output suffers from a narrow window of rising edge in clock pulse. The rising and the falling edge of the clock pulses enables the clock load from the switching. The power consumed by new latch can be reduced by gating its clock pulse. As in Autogated flip flop and data driven clock gating tight timing constraint is reduced in LACG and it is implemented in register. The simulated output in Modelsim is shown in figure 4.

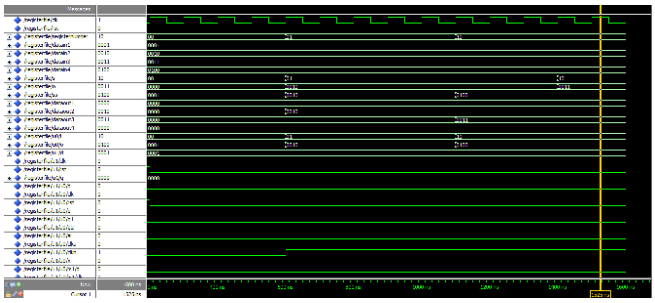

Figure 4: LACG in register file simulated output in modelsim

In a single clock, the register file selects the data from any of the registers and stores the data in any of the register. Datain1, Datain2, Datain3, Datain4 are the 4 bit data inputs of the registers. The register number is decoded by a 2-4 decoder which acts as an enable signal to the registers. A Quad 4:1 MUX is used to select the necessary register output based on the selection line SS. Dataout1, Dataout2, Dataout3, Dataout4 are the corresponding output of the registers. The power analyzed in Xilinx tool is given in figure 5. The optimized dynamic power in the LACG circuit with register file is **158mW**.

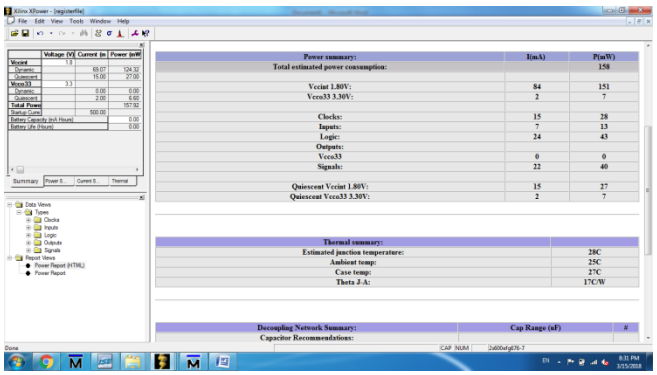

Figure 5: Power report for LACG in register file using Xilinx tool

c. DATA DRIVEN CLOCK GATING IN REGISTER FILE

The data driven based clock gating technique is shown in figure 6. And the technique is implemented in register file by using VHDL code.

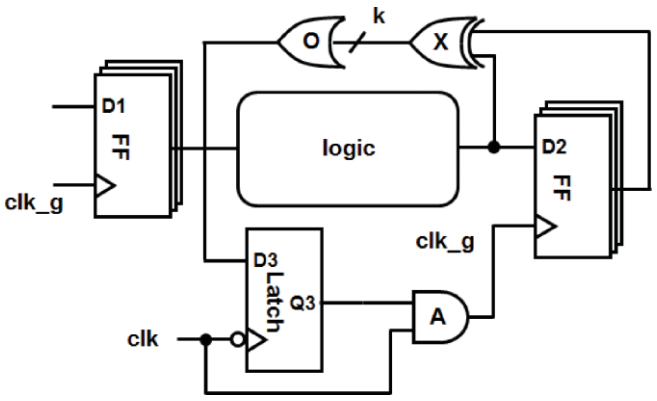

Figure 6: Data driven clock gating in register file

Data driven based clock gating technique is shown in the above figure 6. The flip-flop can be designed without using latch, but here it is used to store the OR gate output for a complete cycle and this helps to remove glitch problem. When comparing with AGFF, the flip flop used in data driven consumes less power because both the latches designed in the D FF are gated. A FF's clock signal can be blocked in the next cycle by XOR- ing its output with the present data input and that output will appear in the next cycle. The outputs of k XOR gates are ORed to generate a combined gating signal for k FFs and they are latched together to avoid glitches. The combination of a latch combined with AND gate is often used and it is called Integrated Clock Gate (ICG). The data driven gating is used for an ultra low power design this tends to reduce the area. A single ICG is mounted over k FFs this gives a clear tradeoff between the number of blocked clock pulses and the hardware overhead. Data driven gating has a drawback is it has a very short time window. Whereas the overall delay

of the XOR, OR, latch and the AND gate donot exceed the setup time of the FF. The percentage increases with the increase of critical paths in the circuit, suppose if a critical situation arise by downsizing or turning transistors of non critical path gradually increases to high threshold voltage (HVT) for further power savings. The data driven gating has a complex design methodology when compared to other gating techniques. In order to maximize the power savings, the FFs should be grouped together so that their toggling nature is highly correlated.

The simulated output in Modelsim is shown in figure 7.

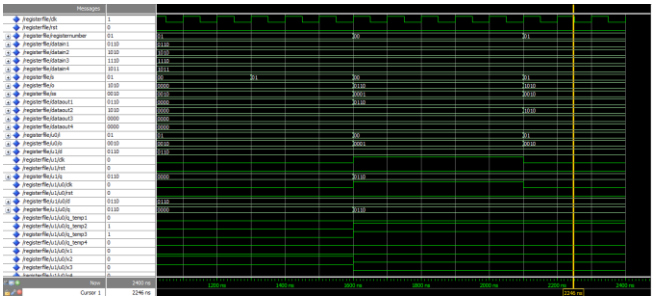

Figure 7: Data driven technique in register file simulated output in modelsim

The generated power report for data driven clock gating in Xilinx tool is shown in figure 8. And the generated dynamic power for data driven clock gating in register file is **173Mw**

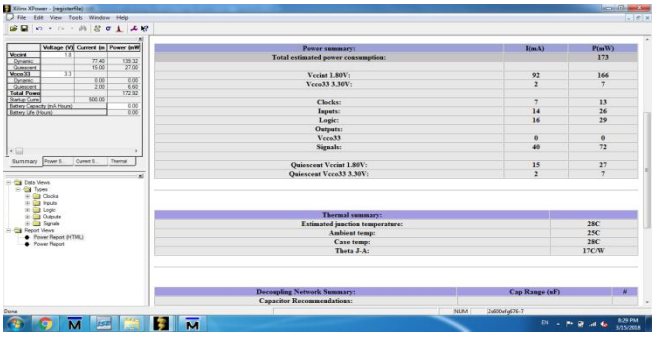

Figure 8: Power report for data driven clock gating in register file using Xilinx tool

d. LACG IN REGISTER FILE WITH MULTI-BIT FLIPFLOP METHOD

In the current scenario power consumption in digital circuits takes a major role. A novel approach is introduced to reduce the power consumption by replacing some flip-flops with fewer multi-bit flip-flops. The flip flops replacement without placement capacity and timing constraint causes severe problem in the circuit design. To compensate the difficulty several proposed techniques are introduced. The first is to perform a transformation to identify those flip flops that can be merged. It shows how to build a combination table to enumerate possible combinations of flip-flops provided by a library. Finally, use a hierarchical way to merge flip-flops as shown in figure 9.

Merge algorithms generally run in time proportional to the sum of the lengths of the lists; whereas that operate on large numbers of lists at once that will multiply the sum of lengths with the list by the time to figure out which of the pointers points to the lowest item, which can be accomplished with a heap-based priority queue in O(log n) time, for O(m log n) time, where n is the number of lists being merged and m is the sum of the lengths of the lists. The power consumed by clocking can be reduced by replacing several other flip flops by using multi bit flip flops. During clock tree synthesis few numbers of flip flops that are less number of clock sinks. Thus the clock network consumes less power consumption and utilizes less routing resource.

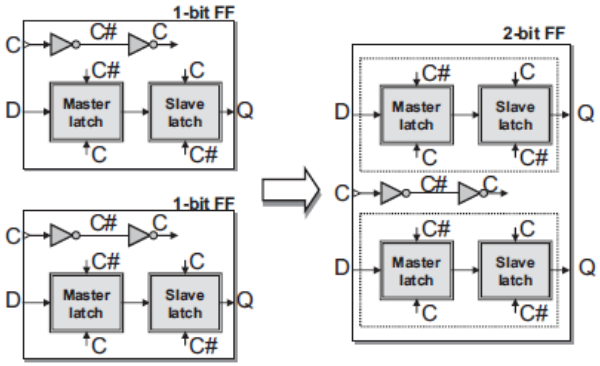

Figure 9: 2-one bit flipflop and one-2 bit flipflop

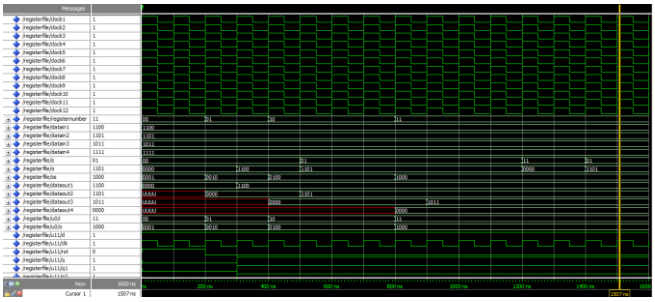

Figure 10: LACG in register file using multibit flipflop simulated in modelsim

Though, the location of flip flops can be changed after the replacement. Thus the length of the wire in nets connecting the pins to the flip flop is also changed. To avoid violating the timing constraints, restrict that the wire lengths of nets connecting pins to a flip-flop cannot be longer than specified values after this process.

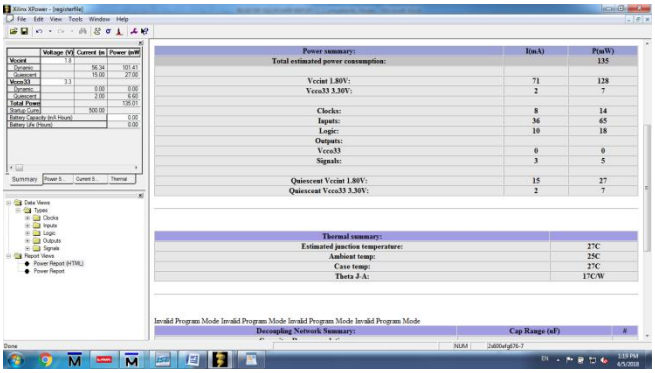

Figure 11: Power report generated for LACG in register file using multibit flipflop in Xilinx tool

For LACG in register file using multibit method the simulated waveform is shown in figure 10 and the power report is generated using Xilinx tool is shown in figure 11. The power optimized by LACG in register file using multibit method is **135mW.**

e. LACG IN REGISTER FILE WITH PULSED LATCH METHOD

The conventional delayed pulsed clock circuits in Fig. can be used to save the AND gates in the delayed pulsed clock generator in figure 12. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. The clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals.

The numbers of latches and clock-pulse circuit's change according to the word length of the sub shift register is selected by considering the area, power consumption, speed. When a pulsed clock signal passes through delay circuit the delayed signal is generated. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch.

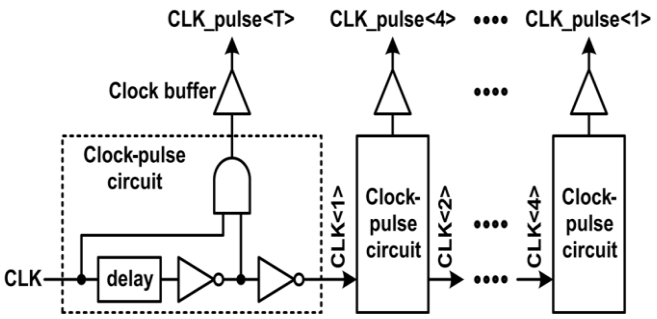

Figure 12: pulse clock generator

Hence, the latch updates the data once in each of the data arrives. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. The simulated waveform is shown in figure 13.

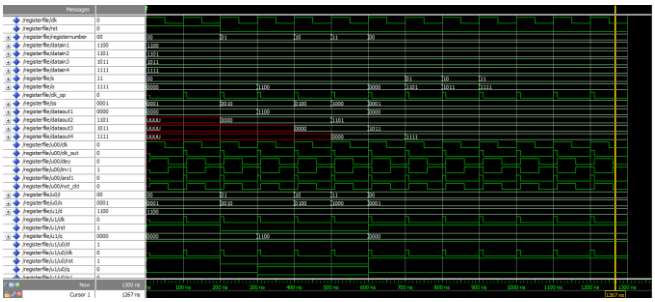

Figure 13: LACG in register file using pulsed latch method

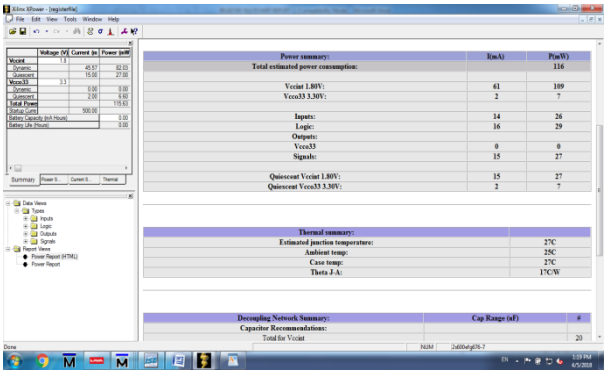

Figure 14: Power report for LACG in register file using pulsed latch method

LACG depends on the XOR output to generate clock signals of some other flip flops in the system this leads the data to depend on that particular flip flop. Instead of applying clock to the FFs, pulsed clock generator is used to generate pulse for the latch present. A small transition of pulse makes less transition and thus reducing power consumption. Datain1, Datain2, Datain3, Datain4 are the 4 bit data inputs of the registers. The register number is decoded by a 2-4 decoder which acts as a enable signal to the registers. A Quad 4:1 MUX is used to select the necessary register output based on the selection line SS. Dataout1, Dataout2, Dataout3, Dataout4 are the corresponding output of the registers. The power optimized by the LACG implemented in register file using pulsed latch method is **116mW**.

IV. COMPARISON OF CLOCK GATING TECHNIQUES

Two new approaches multi bit flip flop method and pulsed latch method are introduced in LACG and implemented in register using VHDL code and they are simulated using Modelsim and Xilinx tool. The generated power report is tabulated in table 1. By experimenting the LACG and data driven clock gating techniques in register file,

the LACG techniques reduces the dynamic power in the register file with 158mW. Whereas the data driven technique optimizes 173mW. The LACG with multi bit optimizes the power of 135mW.

The multi bit method splits the number of bits and for that bit the clock signal is given only when it is required. Though the technique reduces dynamic power but not that much efficient as compared to LACG with pulsed latch method. The pulsed latch method has an accurate rise and fall time in the clock pulse. Because in pulsed latch method the clock pulse are given instead of clock signal, this reduces the power consumption in the design. The best optimized method is LACG using pulsed latch and the power consumption in the circuit is 116mW as compared to LACG in register file with multi bit method.

Table 1: Comparison of clock gating techniques

S.No.	Clock gating techniques	Power
1	Register file using LACG	158mW
2	Register file using data driven	173mW
3	Register file using LACG multibit ff method	135mW
4	Register file using LACG pulsed latch method	116mW

V. CONCLUSION

Low power is the most critical issues in today's ASIC design, as the feature size is scaled down. Clock gating is one of the most elegant and classic techniques for reduction of dynamic power, major contributor in total power consumption of any VLSI circuit. It ensures power saving by turning on/off a functional logic block clock, but only when required. Among the clock gating techniques, Look-ahead clock gating and data driven clock gating are implemented in register file and while comparing the outputs, it is found that LACG yields low dynamic power in register file. Then, two methods are introduced in register file with LACG technique. First method is multibit based flip-flop method and the second method is pulsed latch method. Upon experimenting, LACG using pulsed latch method is found to have low dynamic power consumption in register file.

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