Design And Simulation of LFSR For Random Sequence Generation Using MCML Technology: A Review

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Abstract- *In this review paper introduction to LFSR(linear feedback shift register) using modified MCML(mos current mode logic) for high speed application is given. From the D-latch with switch based MCML tri-state buffer and MCML D-latch using traditional MCML style along with modified switching model proposed LFSR is design. All simulation and designing work will be carry out tanner with 180nm technology. TSPICE and S-edit module of tanner tool are used for parametric simulation of the proposed circuit. The LFSR is used for random sequence generate which is used to test DUT(Design under test) so the noise problem will also analyzed for better and accurate result.*

Keywords- LFSR; MCML

I. INTRODUCTION

As the process technology of CMOS is scaling down rapidly, The power consumption of the CMOS ICs is increasing.High power implies more heat dissipation, Which lower the performance as well as the reliability of the overall system and also limits the density of integration A linear feedback shift register(LFSR) ,designed using MOS current mode logic(MCML). MCML Technology has emerged as a promising Technology due to it's various advantages over other logic style.

At high frequency power dissipation in MCML circuit is significantly less as power dissipation in MCML is independent of it's operation frequency. MCML Technology generate low swiching noise as current supplied during switching is constant .They offer high performance due to low voltage swing , high noise margin and high switching speed. MCML style is appropriate for designing high performance digital circuit. With the rapid increase in transmission speeds of communication systems, the demand for very high-speed low-power VLSI circuits is on the rise. The development of these high-speed circuits has three main driving forces: 1) higher levels of integration to provide higher performance at lower cost; 2) the use of popular VLSI technologies such as CMOS; and 3) the ability to provide low-power system-on-chip implementations. Although the performance of CMOS technologies improves notably with scaling, conventional CMOS circuits cannot simultaneously satisfy the speed and power requirements of these applications. Moreover, conventional CMOS circuits generate significant supply noise, thus hindering the on-chip integration of sensitive analog and digital circuits.

LFSRTHEORY AND APPLICATIONS

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and has a very long cycle.

Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences. Both hardware and software implementations of LFSRs are common.

RANDOM SEQUENCE GENERATOR

A pseudorandom number generator (PRNG), also known as a deterministic random bit generator (DRBG), is an algorithm for generating a sequence of numbers whose properties approximate the properties of sequences of random numbers. The PRNG-generated sequence is not truly random, because it is completely determined by an initial value, called the PRNG's seed (which may include truly random values). Although sequences that are closer to truly random can be generated using hardware random number generators, pseudorandom number generators are important in practice for their speed in number generation and their reproducibility. PRNGs are central in applications such as simulations (e.g. for the Monte Carlo method), electronic

games (e.g. for procedural generation), and cryptography. Cryptographic applications require the output not to be predictable from earlier outputs, and more elaborate algorithms, which do not inherit the linearity of simpler PRNGs, are needed.

MCML BASED LFSR DESIGN

In this section architecture of MCML circuit and design of traditional exclusive-OR (XOR) gate using series-gating approach is explained.

MOS Current-Mode Logic (MCML) is a low-noise alternative to CMOS logic for mixed signal applications. If properly designed, MCML circuits can achieve significant power reduction compared to their CMOS counterparts at frequencies as low as 300MHz. MCML logic has, however, fallen out of favor because of its high design complexity and the lack of automated design and optimization tools. In this work, simple and accurate propagation-delay models for MCML circuits, that are suitable for mathematical programming, have been developed and verified. The models are based on a modified version of the differential-pair MCML universal gate. The modified universal-gate performance has been compared to the standard universal gate topology.Simulations have shown th at the modified universal gate has better DC symmetry, lower switching noise and higher operation frequency.

II. LITERATURE REVIEW

1. ***Samiksha Agraval, Neeta Pandey, "Design of MCML-based LFSR for low power and mixed signal applications".2015***

In this paper, A Linear feedback shift register (LFSR) is a very important digital circuit which generates pseudo-random patterns of 1s and 0s with wide number of applications in the fields of digital system design and testing, computer networks and wireless communication. A MCML-based LFSR is presented in this paper, which has been implemented in three different ways and it's performance is compared with the traditional CMOS based LFSR reduce the power consumption by 60.1% and thus addresses the major concern of low power consumption in VLSI chip. Due to the MCML based circuitry, the digital switching noise of LFSR is also very low which makes it suitable for mixed signal applications.

2. **Maintaining the Integ *Radhika, N. Pandey,K.Gupta, and M. Gupta, "New design of Exclusive-OR (XOR) gate by using low-power MCML tri-state buffer".2014***

In this paper, new Exclusive-OR (XOR) gate design by using MCML low-power tri-state buffer is presented. Theoretically we can understand that traditional XOR gate is implemented by using multiple levels of source-coupled transistor pairs, whether new design of XOR gate is implemented by using only one level of transistor pairs. Thus application of tri-state buffer is demonstrated in digital circuits like multiplexers and fundamental gate like exclusive–OR (XOR).

3. ***M. Anis, M. Elmasry, "Impact of on-chip process variations on MCML performance,".2002***

In this paper , As technology scales down, CMOS is the least affected logic style. Its performance and robustness are enhanced compared to other logic styles. Domino's performance and power will deteriorate because of the leakage currents and contention caused by the keeper transistor, while DCVS will also suffer from leakage power, but doesn't have any contention problems during evaluation. Because interconnects are not scaled linearly with technology, the percentage of power consumed in the clock tree will grow. CPL performance degrades much faster than other logic styles because of the reduction of the ratio VDD/VTH with technology scaling. Hot carrier effect makes it even worse by increasing VTH over the long term. CPL area will tend to grow with more power dissipation for the larger area and the complex routing. Although CML tops the logic styles in many circuit implementations in terms of minimum EDP, it is yet not very widely used. This is attributed that CML cannot be used as standard cells, because the RC delay of each gate varies for every gate, according to the Funin and Funout**.** MCML may also have some trouble with VTH variations caused by the hot carrier effects. But if MCML is used at a lower supply voltage, the effect of the hot carrier will be less significant.

4. ***Hassan Hassan , "MOS Current Mode Circuits: Analysis,Design,and Variability".2005***

In this paper,This work presented an automated optimization-based design strategy for MCML circuits to achieve minimum power dissipation while satisfying other constraints on the delay, gain, voltage-swing ratio, and noise margin. The analytical formulations for MCML circuits given in this work are intended to provide MCML designers with design guidelines. The design methodology is based on the BSIM3v3 model with accuracy within 11%.Parameter variations are integrated into the design methodology to design MCML circuits for variability. The degrading impact of parameter variations on MCML circuits as technology

scales is shown to be almost doubled from 180-nm to 45-nm technologies.

5. BIJAN DAVARI, "CMOS Scaling for High Performance and Low Power".1995

In this paper, Scaled CMOS technology is ideally suited as the engine for both tomorrow's high performance systems and for the coming low power revolution. Within the next decade, there will be an explosive growth of capability in silicon chips, made possible by CMOS scaling. This growth will affect all aspects of human life as the integration of high performance systems on a single chip (as powerful as today's supercomputers) becomes a reality. In this The biofertilizer (10g/1Kg) markedly enhanced the plant sh article,a guideline for CMOS scaling over the next 10 years has been presented, with emphasis on the optimization of high-peormance and low-power scenarios aimed at logic applications such as microprocessors. After considering key device and technology bottlenecks and various nonscalable elements, it is projected that the performance, density, and active power dissipation will all improve dramatically as scaling proceeds along the path presented in the guideline.

6. Osman Bakri Musa Abdulkarim, "DESIGN AND OPTIMIZATION OF MOS CURRENT-MODE LOGIC CIRCUITS".

MOS Current-Mode Logic (MCML) is a low-noise alternative to CMOS logic for mixed signal applications. If properly designed, MCML circuits can achieve significant power reduction compared to their CMOS counterparts at frequencies as low as 300MHz. MCML logic has, however, fallen out of favor because of its high design complexity and the lack of automated design and optimization tools.

III. METHODOLOGY

1. Study of MCML technology

MCML Technology has emerged as a promising Technology due to it's various advantages over other logic style. At high frequency power dissipation in MCML circuit is significantly less as power dissipation in MCML is independent of it's operation frequency. MCML Technology generate low swiching noise as current supplied during switching is constant .They offer high performance due to low voltage swing , high noise margin and high switching speed. MCML style is appropriate for designing high performance digital circuit. With the rapid increase in transmission speeds of communication systems, the demand for very high-speed low-power VLSI circuits is on the rise.

2. Tri-state buffer based design

In this section MCML based low-power tri-state buffer circuit is briefly reviewed and Exclusive-OR (XOR) gate design implementation using novel method of tri-state buffer is also explained.

3. MCML low-power tri-state buffer

The fundamental MCML low-power based tri-state buffer is design in this project.

4. Exclusive-OR (XOR) gate design based on tri-state buffer

MCML tri-state buffer circuit is used to implement 2-input MUX using two tri-state buffers with common latched output, and complementary enable signals.

5. Study and installation of Tanner

Study LFSR design techniques and methodology for simulation. Developed software and performed the operation in tanner s-edit.

IV. EXPECTED OUTCOME

The random sequence generate proposed in this project is faster.The modified design of MCML is responsible for high speed and low noise results of sequence generator LFSR.

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