# Design of Digital Fir Filter Using Linear Phase Realization

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***Abstract-*** *Area efficient VLSI implementation Linear phase FIR digital filter of various length which involves in designing an Inner Product Unit of FIR filter architecture. In this paper optimization of digital FIR filter Linear Phase Realization is proposed. This reduces hardware complexity of the system, it shows the reduction of multipliers results in improving the performance of FIR filter and hence the area delay product is highly reduced in linear phase, the overall length of the filter is also minimised. Simulation results are obtained for odd length ad even length structures using Xilinx. From the simulation results it is observed that the performance of the proposed technique is better than that of existing structure.*

***Keywords***- Digital Signal Processor (DSP), Finite Impulse Response (FIR), Inner Product Unit (IPU), Frequency Sampling Method, Linear Phase realization

## I. INTRODUCTION

In Signal Processing, a filter is a device that helps in removing some unwanted components or features from signal. Filtering is a class of signal processing, the defining feature of filters being the complete or partial suppression of some frequencies and not others in order to suppress interfering signals and reduce background noise. However, filters does not properly behave in the frequency domain;mainly in the field of image processing. Correlations are removed for certain frequency components and not for others without having to act in the frequency domain. The filters classified based on their overlap that occur in many different ways; there is no simple hierarchical classification. Filters such as Linear or Non-Linear, Time Variant or Time Invariant, Casual or Non Casual, Analog or Digital, Discrete Time (sampled) or Continuous Time, Finite Impulse Response (FIR) or Infinite Impulse Response (IIR).The design of FIR filter involves some techniques such as designing, implementation in low power circuits for digital signal processing (DSP) applications.The major two types of filters are Analog Filter and Digital Filter.

The digital filters are further classified into Finite duration impulse response (FIR) and Infinite duration impulse response(IIR). FIR filters are determine by their impulse response coefficients that indicating the multiplication constants with the input signals. These multipliers are power and area consuming devices such as portable wireless devices like mobile phones, tablets, laptops etc. The implementation of Linear Phase realization are discussed which results in highly multiplierless structure of an FIR filter. A small number of shifters, adders and filpflops resulting in corresponding improvement in the area and power efficiency can replace multipliers. Low area and low power design of FIR filter can also be implement in parallel or block processing which is also found to be suitable to increase the effective throughput.The various methods involves in implementing the IPU structure for FIR filter such as Linear phase realization structure,Polyphase realization,Canonical and Non canonical structure,Direct form or Transpose Structure,Transversal Structure etc…..

## II. PROPOSED SYSTEM

Linear Phase refers the condition in which the phase response of the filter is a linear straight-line function of frequency excluding phase wraps at 180 degree phase difference. The delay that occurs through the filter will be same at all frequencies. Therefore, the filter does not cause phase distortion or delay distortion. The absence phase or delay distortion that can be more advantage of FIR filters when compare to IIR filters.The most commomly used analog filters in certain systems."For example:Digital Data Modem". The four types of linear phase FIR filters are Symmetric sequence of odd length, Symmetric sequence of even length, Anti-symmetric sequence of odd length,Anti-symmetric sequence of even length. All frequency components of the input signal are shifted in time (usually delayed) by the same constant amount, which is referred to as the phase delay. For discrete-time signals, perfect linear phase is easily achieved with a finite impulse response (FIR) filter**.**

The block diagram of FIR filter has adder unit,coefficient storage unit,register unit and inner product unit.The register unit in FIR filter has small set of data holding storage places,it also consists of instructions,address etc…The input coefficients values are stored in coefficient storage unit for performing the further operations of all filters.The adder

unit is a digital ciircuit which performs the addition operation.An adder is the core of an arithmetic logic unit(ALU).The IPU in FIR filter perform inner-product computations.

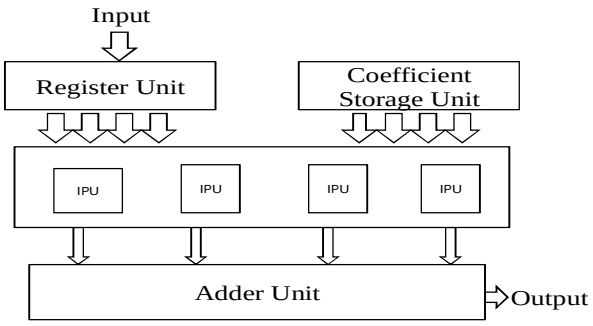


Fig :2 Block Diagram Proposed FIR Filter

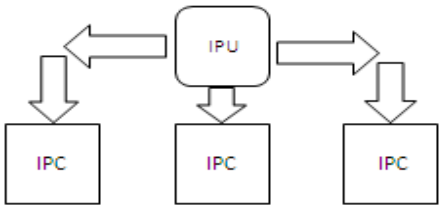


Fig : 3 Internal Structure of IPU

The structure of IPU consists of number of inner-product cells (IPCs). The IPC receives the transfer function coefficient values, and computes a result.These inner products results are added in the adder unit.The proposed IPC of FIR filter is implemented by using Linear phase realization.Linear phase realization structure results in reducing the area,power consumption and hardware complexity.

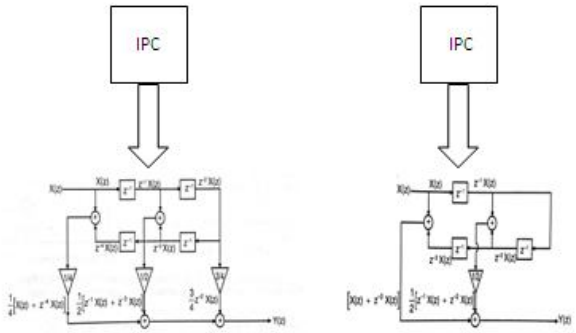


Fig: 4 Internal Structute Of IPC Linear Phase

## III. FILTER RESPONSE CONDITION

Consider the impulse response, h(n) of FIR system,

$$h(n) = \{b_0, b_1, b_2 \dots\dots\dots\dots b_{N-1}\} \quad (1)$$

FIR system, for linear phase response the impulse response should be symmetric.

The condition for symmetry is,

$$h(n) = h(N-1-n) \quad (2)$$

$$H(Z) = Y(Z)/X(Z) \quad (3)$$

$$Y(z)=\frac{1}{4}[X(z)+z^{-4}X(z)]+\frac{1}{2}[z^{-1}X(z)+z^{-3}X(z)]+\frac{3}{4}z^{-2}X(z)] \quad (4)$$

$$Y(z) = X(z) + \frac{1}{2}z^{-1}X(z) + \frac{1}{2}z^{-2}X(z) + z^{-3}X(z) \quad (5)$$

When the impulse response is symmetric, the samples of impulse response will satisfy the condition,

$$b_n = b_{N-1-n} \quad (6)$$

By using the above symmetry condition, it is possible to reduce the number of multipliers required for the realization of FIR system. Hence, **the linear phase realization is also called realization with minimum number of multipliers.**

## IV. RESULTS OF PRPOSED SYSTEM

Let, N=7, h(n) = h(6 − n),h(n) = h(n-6) where N=0,12,3,4,5,6

| LENGTH | TRANSFER FUNCTION |
|---|---|
| WHEN N=0; | h(0) = h(6) |
| WHEN N=1; | h(1) = h(5) |
| WHEN N=2; | h(2) = h(4) |
| WHEN N=3; | h(3) = h(3) |

*TABLE 1 TRANSFER FUNCTION VALUES FOR ODD LENGTH*

| LENGTH | TRANSFER FUNCTION |
|---|---|
| WHEN N=0; | h(0) = h(7) |
| WHEN N=1; | h(1) = h(6) |
| WHEN N=2; | h(2) = h(5) |
| WHEN N=3; | h(3) = h(4) |

*TABLE 2 TRANFER FUNCTION VALUES FOR EVEN LENGTH*

The transfer function values h(n) for odd and even length filter are determine by the input co-efficients and according to the N values.

TABLE 3 RESULTS OF PROPOSED SYSTEM

| S.NO | UNITS | EXISTING SYSTEM | PROPOSED STRUCTURE I | PROPOSED STRUCTURE II |
|---|---|---|---|---|
| 1 | 8bit adder | 2 | 15 | 7 |
| 2 | 1bit adder | 28 | 7 | 7 |
| 3 | 8bit register | 18 | 16 | 12 |
| 4 | Multipliers | 16 | 3 | 1 |

The table shows the comparison of proposed and existing system. It consists number of 1 bit adders,8 bit adder, register and multipliers are minimised when compared to existing system.

## V. CONCLUSION

The designing a INNER PRODUCT UNIT(IPU) of Linear Phase Realization structure for FIR filter which results in reducing the hardware complexity.The simulation results demonstrate significantly reduction in area of designing an IP unit and no performance degradation,when compare to an existing direct form structure in IPU. Linear phase as the advantages of combining the closely related coefficients value of the input and output transfer function i.e H(z). Multipliers are the major portions in hardware consumption for the FIR filter implementation. The proposed new structures exploit the nature of co- efficient of even length and further reduce the amount of multipliers required. The further work has be implementing in hardware desiging for analysing an overall power consumption of FIR filter.

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