Comparative Analysis of Diverse Realizations For Digital Controller Implementation on FPGA

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Abstract- *The digital controller plays an important role in manufacturing and process industries. For implementation and realization of digital controller, we need to use and design multiplier and adder blocks in FPGA. When there is a specific standalone controller requirement at remote place, we can use controller implementation on FPGA chip. To improve the speed of response and accuracy, we can go with some advance method like Distributed Arithmetic (DA) architecture. The main perspective of this paper is to design and develop digital controller structure and its implementation on FPGA for better performance in terms of speed and optimal utilization resources. The digital controller will be designed using MATLAB and Simulink to generate a set of coefficients associated with the desired controller characteristics. The controller design, synthesis and analysis will be done using Xilinx ISE 14.2 software. The controller coefficients will include in VHDL that implements the digital controller on to FPGA. Digital controller structure equation will be implement on Xilinx Spartan 3E FPGA board.*

Keywords- Distributed arithmetic algorithm,VHDL,PID controller,Matlab,Xilinx ISE 14.2,FPGA.

I. INTRODUCTION

The digital controller plays an important role in manufacturing and process industries. A plant and a controller, the control system consists these two subsystems. The digital controller implementation includes the use of microprocessors or microcontrollers. The memory holds the application program while the processor fetches, decodes, and executes the program instructions. In this method the disadvantage is in speed of operations because this operations depend on software which has a sequence of instructions and commands which needs many machine cycles to execute. Therefore, FPGA-based digital PID controller is proposed because the operations on FPGA are hardware compatible operations.

In the Field programmable gate array-based digital controller there are two realizations, one is multiplier based and another is multiplier less. In the multiplier based realization, the multipliers will diminish the speed of preparing time on the grounds that the increasing stage is an utilization procedure which presents spread deferral and uses substantial piece of silicon territory. In this way, these augmentations are change to Distributed Arithmetic (DA) architecture which is multiplier less strategy. The implementation based on look up tables method in Distributed Arithmetic (DA) architecture.

II. DIGITAL PID CONTROLLER STRUCTURE

The proportional, integral, and derivative control actions can be brought together to create a PID controller. The block diagram of PID controller is shown in Fig.1.[1]

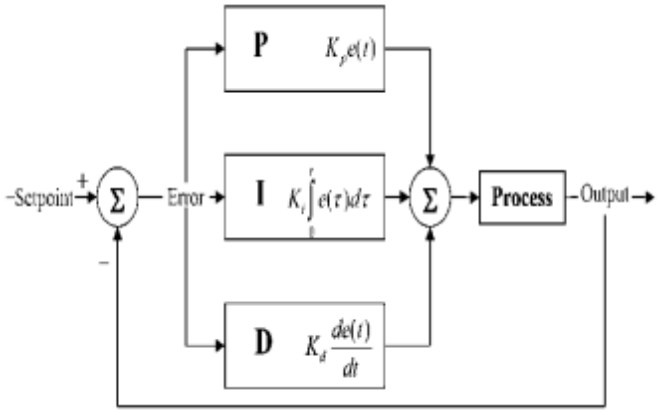

Fig. 1 Block diagram of PID controller

The simplest form of the PID control equation is given by,[4]

$$u(t) = K(e(t) + \frac{1}{T_i}\int_0^t e(t)\,dt + T_d\frac{de(t)}{dt}) \quad (1)$$

Taking Laplace transform of (1) we get,

$$U(s) = K(E(s) + \frac{1}{sT_i}E(s) + sT_dE(s)) \quad (2)$$

Now the transfer function of PID controller is:

$$G_c(s) = \frac{U(s)}{E(s)} = K(1 + \frac{1}{sT_i} + sT_d)$$
(3)

Now, Discretized equation (3) we get,

$$\frac{U(z)}{E(z)} = K(1 + \frac{T_s}{2T_i}\frac{z+1}{z-1} + \frac{T_d}{T_s}\frac{z-1}{z})$$
(4)

By simplifying the equation (4) we get,

$$U(z) = z^{-1}U(z) + s_0E(z) + s_1z^{-1}E(z) + s_2z^{-2}E(z)$$

Now, discrete controller equation is given as,

$$u(k) = u(k-1) + s_0e(k) + s_1e(k-1) + s_2e(k-2)$$
(5)

Where,

$$s_0 = K(1 + \frac{T_s}{2T_i} + \frac{T_d}{T_s})$$
$$s_1 = K(-1 + \frac{T_s}{2T_i} - 2\frac{T_d}{T_s})$$
$$s_2 = K\frac{T_d}{T_s}$$

The control law, as given by Equation (5), is in the difference or incremental formulation. This equation represents the digital PID controller structure.

III. DESIGN OF DIGITAL CONTROLLER IN MATLAB SIMULATION

Here, DC motor speed control system is used for case study to design digital controller in matlabsimulink and to derive controller parameters for digital controller structure

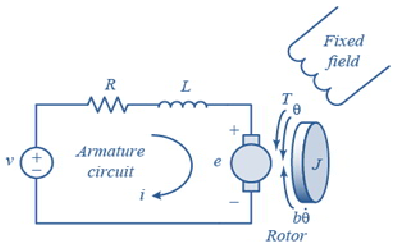

Fig.2.1[2] Electrical scheme of DC motor

Here,the rotational speed is output and armature current is input. So the Transfer function can be derived as,[2]

$$G(s) = \frac{\dot{\theta}(s)}{V(s)} = \frac{K}{(Js+b)(Ls+R)+K^2}$$
(6)

The parameter values of this system are as follows:

Moment of inertia of the rotor	0.01 kg.m^2
Motor viscous friction constant	0.1 N.m.s
Electromotive force constant	0.01 V/rad/sec
Motor torque constant	0.01 N.m/Amp
Electric resistance	1 Ohm
Electric inductance	0.5 H

Now, putting all these values in equation (6) we can derive the system transfer function as follows,

$$G(s) = \frac{0.01}{0.005s^2 + 0.06s + 0.1001}$$
(7)

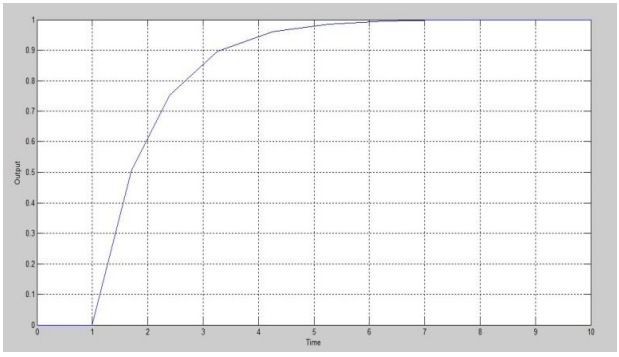

Fig.2.2 Open loop test response of the system

In this open loop test response, The Ziegler-Nichols tuning method is used to tune the PID controller parameter.

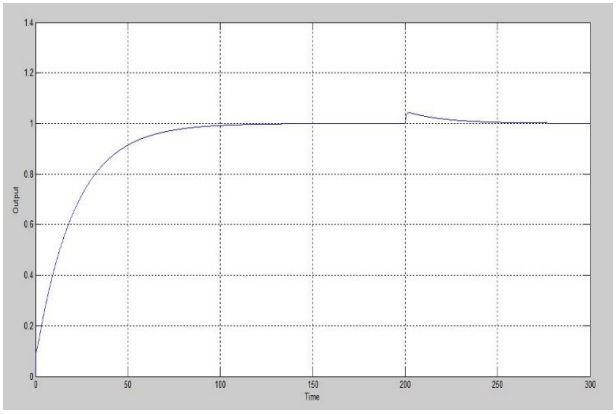

Fig.2.3 Response of close loop system of digital controller Design

By this controller design the controller equation is given as ,

$$u(k) = u(k-1) + s_0 e(k) + s_1 e(k-1) + s_2 e(k-2) \quad (8)$$

Where,

$$s_0 = 28$$
$$s_1 = -55$$
$$s_2 = 27$$

This equation represents the digital PID controller structure, this will be design in Xilinx using distributed arithmetic algorithm in VHDL language and implement on Xilinx Spartan 3E FPGA board.

IV. DISTRIBUTED ARITHMETIC(DA) ALGORITHM

Distributed arithmetic is a bit level rearrangement of a multiply accumulate to hide the multiplications. Distributed Arithmetic is the bit serial algorithm which performs efficient multiplication by using LUT's .It is a powerful technique for reducing the size of a hardware that is well suited to FPGA designs. It can be implemented on LUT "Look-up-table" and values stored in ROM.

Digital controller structure is MAC operation and it gives output as multiply all current and previous sample value of input signal with coefficients of controller parameters and sum all products. DA algorithm replace MAC operation by Look-Up Table method.

Now we step ahead to DA algorithm and see where ROM is come in picture.

The digital controller structure equation is derived as above,

$$u(k) = u(k-1) + s_0 e(k) + s_1 e(k-1) + s_2 e(k-2)$$

Here,

$$s_0 = 28$$
$$s_1 = -55$$
$$s_2 = 27$$

All the possible values of u(k) are stored in ROM. There will be 8 different possible values of u(k) which is illustrated in the Table.1.

Table 1 Values Stored in ROM Look up table

Xb[2]	Xb[1]	Xb[0]	F(c[n],x[n])
0	0	0	0
0	0	1	s_0
0	1	0	s_1
0	1	1	$s_1 + s_2$
1	0	0	s_0
1	0	1	$s_0 + s_2$
1	1	0	$s_0 + s_1$
1	1	1	$s_0 + s_1 + s_2$

The size of ROM is very important for high speed implementation as well as area efficiency. ROM size grows exponentially with each added input address line. The proposed multiplierless based architecture is obtained using DA.[9]

V. MULTIPLIER BASED DIGITAL CONTROLLER

The digital PID controller equation (8) will be design in Xilinx using VHDL language.

Based on the equation, the direct multiplier implementation of the digital PID controller is shown in Figure Fig.5.The architecture of the multiplier Based PID controller had been designed in Xilinx ISE 14.2 using VHDL language.

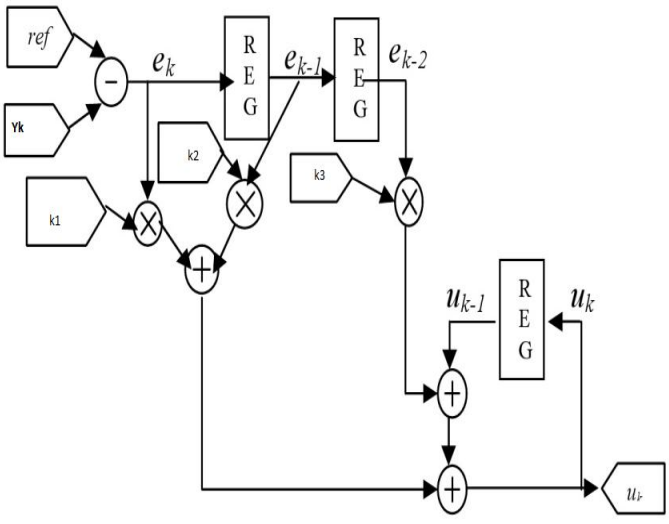

Fig. 5 Architecture of the MULTIPLIER based PID controller

VI. SIMULATION RESULT AND HARDWARE IMPLEMENTATION

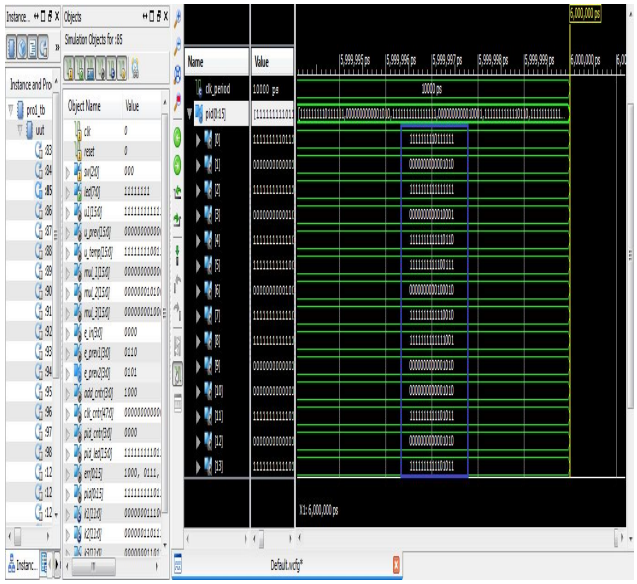

Fig. 6.1 simulation result of multiplier based PID controller

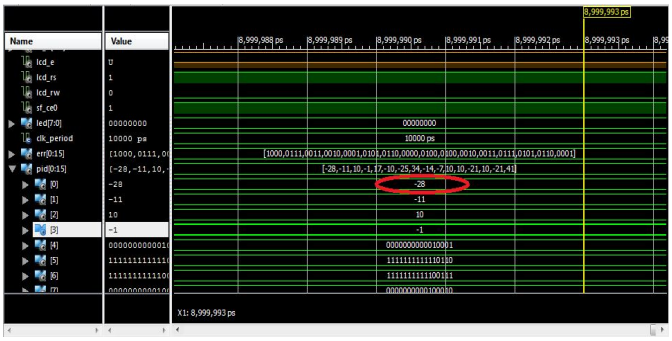

Fig. 6.2 snapshot of Xilinx simulation output of DA based digital controller

Fig. 6.3 DA output1 displayed on LCD on Spartan 3E board

Here, the main difference between multiplier based and DA based architecture is, in DA based architecture the values are stored in forming LUTs and it hides explicit multiplication. So, by this DA uses less FPGA resources and this technique is area efficient that will be shown in device utilization report.

VII. COMPARATIVE ANALYSIS OF TWO DIVERSE REALIZATION

Logic Utilization	Used	Available	Utilization
Number of slices	131	4656	2%
Number of Slice Flip Flops	102	9312	1%
Number of 4 input LUTs	238	9312	2%
Number of bounded IOBs	9	232	3%
Number of MULT18X18SIOs	2	20	10%
Number of GCLKs	1	24	4%

Table.2 Device Utilization Report Summary Of multiplier based digital controller

Logic Utilization	Used	Available	Utilization
Number of slices	111	4656	2%
Number of Slice Flip Flops	129	9312	1%
Number of 4 input LUTs	195	9312	2%
Number of bounded IOBs	9	232	3%
Number of GCLKs	1	24	4%

Table.3 Device Utilization Report Summary Of DA based digital controller

VIII. CONCLUSION

The main aim of this paper is to implement Distributed arithmetic (DA) algorithm on FPGA using VHDL language. Here, two realizations of FPGA based PID controller are considered, one is multiplier based and other is DALUT based. Implementation of Multiplier based PID controller requires large number of hardware resources , whereas DALUT based PID controller is a compact design with optimal utilization of hardware resources, which shows in the device utilization summary report.

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