Digital Phase Locked Loop: An Fpga Implementation

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Abstract- *A PLL is a negative feedback system where an oscillator generated signal is phase and frequency locked to a reference signal. To overcome the drawbacks of the conventional PLL, the analog PLL is modified using all digital components. In this paper, ADPLL is designed using VHDL in Xilinx ISE Design suite 13.4 and implemented on FGPA.*

Keywords- Phase detector, loop filter, DCO, FPGA.

I. INTRODUCTION

Phase locked Loop is a control mechanism whose objective is to make the difference between the phase of VCO output and the input reference signal very small. Hence, at the PLL input these two quantities are subtracted by the phase detector and the result is applied to the loop filter and VCO to ensure that in a stable steady state the difference is small. Phase locked loop mechanism can be implemented as either analog or digital circuit. Both implementation use the same basic structure i.e, Phase Detector, low pass filter, variable frequency oscillator and a feedback path which may include a frequency divider. PLL is Classified into four types (a) Linear PLL (b) Digital PLL (c) All Digital PLL (d) Software PLL [1]. Linear PLL consists of all analog circuit components. Due to High power consumption and large area of the analog circuit, digital PLL was proposed. In DPLL only the phase detector was digitized where as the other components were analog. The design of these circuits becomes sensitive due the presence of both analog and digital components which increases design cycle time and time to market. To overcome the disadvantages of Digital PLL, All Digital PLL was designed. The ADPLL consists of all digital blocks. The Phase Detector can be a simple EX-OR gate, Edge triggered J K flip flop, Phase frequency detector etc. The loop filters which can be used are k counter loop filter, up/down counter, N before M loop filter. The DCO block can be divide by N counter DCO or Increment decrement counter DCO [1].

PLL goes through three states (i) Free running (ii) Capture (iii) Lock.

Initially no input signal is applied to PLL. Under this condition, phase detector and filter outputs will be zero. At this time, VCO operates at free running frequency. This is the normal operating frequency of vco. Once the input frequency is applied the vco starts to change and PLL is said to be in Capture mode. The vco frequency continues to change until it equals the input frequency and the PLL is in phase lock mode.

PLL finds wide range of applications in Frequency demodulation, signal recovery from a noisy communication channel, frequency synthesis etc. Since a single integrated circuit can provide a complete phase locked loop building block, the technique is widely used in modern electronic device with output frequency from a fraction of hertz to many gigahertz [2].

HDL is very flexible for modifying the design parameters. Therefore, ADPLL is designed and synthesized using VHDL language and Xilinx ISE 13.4 respectively, and implemented using Spartan 6 FPGA board [9].

II. ADPLL DESIGN

The basic block of the ADPLL consists of a Digital phase detector, Digital loop filter, Digital controlled oscillator. The three main parts of the ADPLL are same as that of a PLL but they are designed and constructed differently for the fact that the input signal dealt by the different system and FPGA is digital. Usually a clock or the output of the analog to digital converter forms the input to the ADPLL [11].

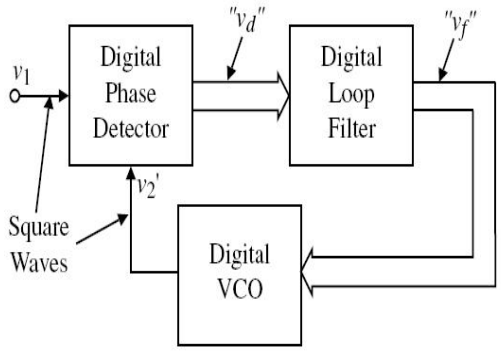

Fig.1: General Block Diagram of ADPLL

A. Phase Detector

Phase detector is a circuit that is capable of delivering an output signal that is proportional to the phase

difference between its two input signals. In this paper a simple Exclusive OR gate is used as a phase detector. It compares the error between the phase of the input signal *v1* and the phase of the DCO output *v2'*. This error signal is used to denote the direction signal of the loop filter. The phase limit of the EX-OR phase detector is -90° to +90° [1]. The advantage of using a EX-OR gate is that it is a simple logic gate which is easy to implement and is reliable.

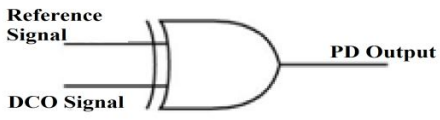

Fig.2: EX-OR Phase Detector

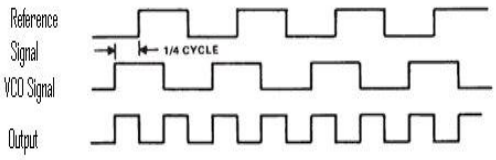

Fig.3: EX-OR gate Waveform

B. K loop filter

K loop filter is employed when the phase detector is either a EX-OR gate or Edge triggered JK flip flop. The K counter consists of two independent counters up counter and down counter respectively, but both counters count upwards. K is the modulus of two counters, i.e., the contents of counters is in a range from 0 to K-1. K can be controlled by the K modulus input and it is always a integer power of 2. The frequency of the clock signal is set M times of the centre frequency Mf_o [10].

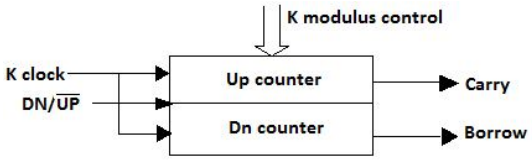

Fig.4: K loop filter

The operation of K counter is controlled by UP/DN signal. If UP/DN=1, down counter is active and up counter contents are frozen. If UP/DN=0, up counter is active and down counter contents are frozen. Both counters recycle to zero when the contents exceed K-1. The MSB of the up counter is used as Carry output and the MSB of the down counter is used as Borrow output. The UP/DN input is controlled by the output of the phase detector.

Positive going edges of the carry and borrow control the digital controlled oscillator [1].

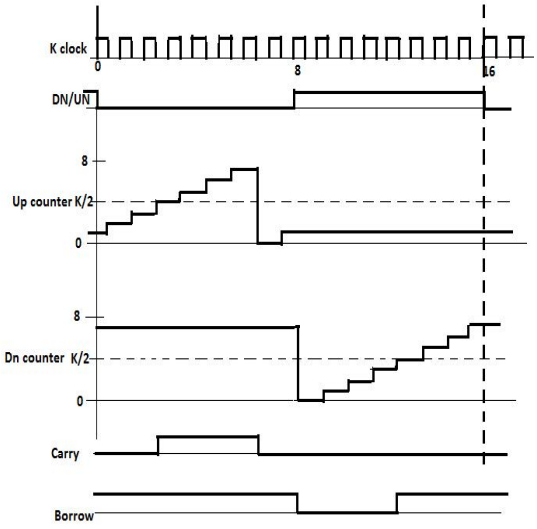

Fig.5: K loop filter waveform

C. Digital Controlled Oscillator

In this paper Increment Decrement counter is used as DCO which is intended to operate in conjunction with those loop filters that generate carry and borrow pulses such as K counter loop filter. The ID Counter has three inputs, clock (ID clock), increment and decrement. Carry pulses are fed to increment input and borrow pulses to decrement input. The ID clock is 2N times the centre frequency, where N is an integer. The output of the ID counter is IDout [8].

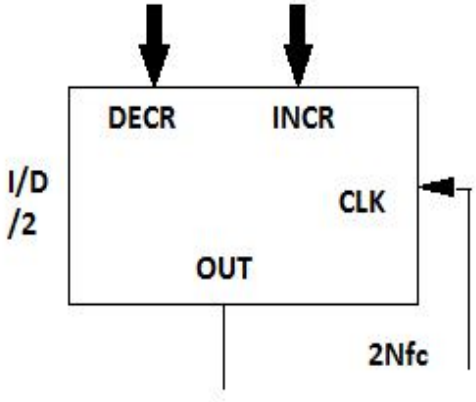

Fig.6: Increment Decrement Counter

The DCO works on the positive edges of carry and borrow pulses supplied by the loop filter. In the absence of the carry and borrow pulses, the ID counter simply divides the ID clock frequency by 2.

If carry is present then half cycle is added and if borrow is present then half cycle is deleted from IDout [2]. Fig.7 shows the output waveform of ID counter [9].

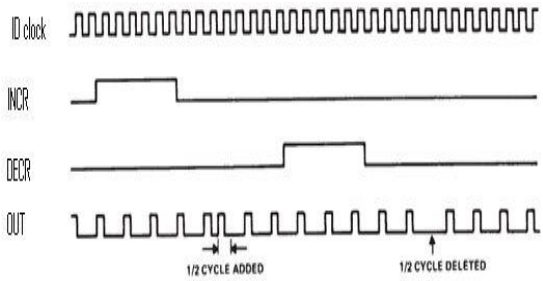

Fig.7: Waveform of Increment Decrement counter

The overall internal diagram of ADPLL is as shown in Fig.8.

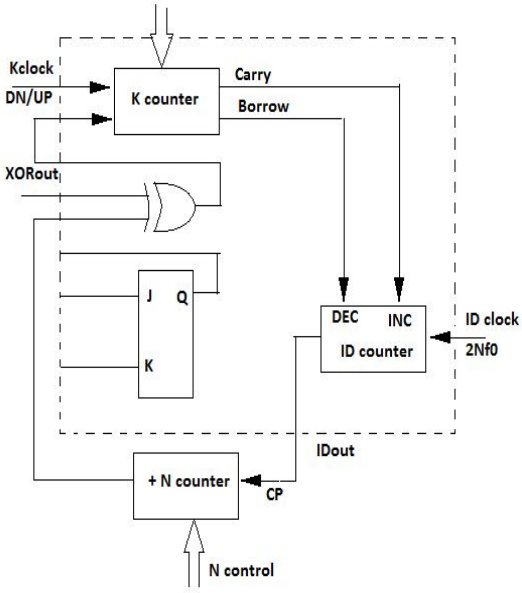

Fig.8: Internal Structure of ADPLL

III. ADPLL PARAMETERS

The parameters considered in this paper are mainly power dissipation and Area Utilization [11].

A. Power dissipation

Power dissipation is an important metric in any electronic circuit. Power dissipation is proportional to the heat generated by the chip or system, excessive heat dissipation may increase operating temperature and cause gate circuitry to drift out of its normal operating range which causes gates to generate improper output values. Thus power dissipation of any gate implementation must be kept as low as possible.

B. Area Utilization

The continuous scaling down of technology has minimized the effective area of digital circuits. Furthermore, by employing better designing techniques area utilization can be reduced considerably.

IV. SIMULATION RESULTS

The simulation result of the phase detector and ID counter is shown Fig.9 and Fig. 10 respectively.

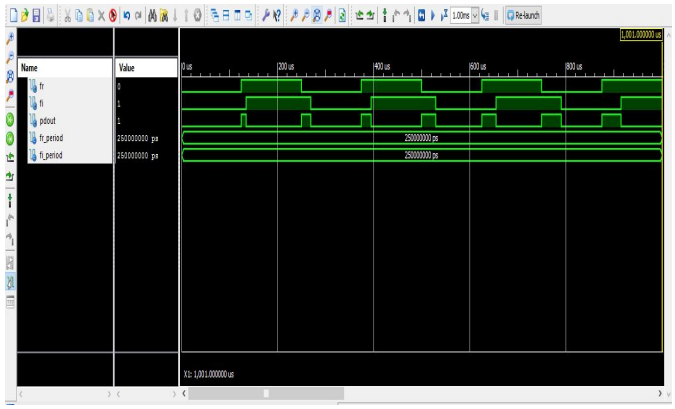

Fig.9: EX-OR Phase detector output

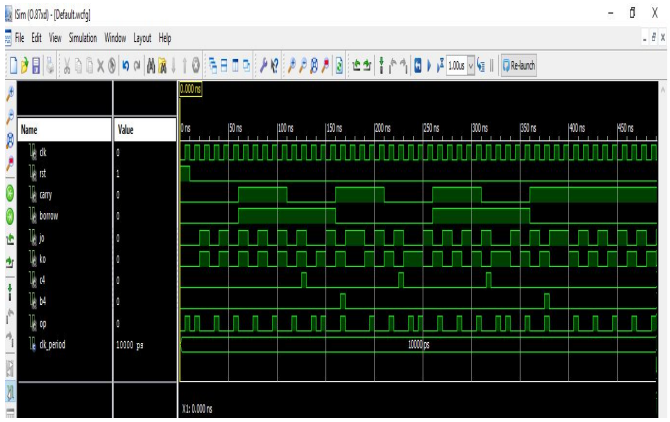

Fig.10: ID counter output

V.CONCLUSION

The ADPLL was implemented to analyse the design parameters such as power dissipation and slice logic distribution. The above ADPLL design can be further improved to obtain better system performance. The All Digital Phase Locked Loop is designed and synthesized using VHDL

language and Xilinx ISE 13.4 respectively and implemented using Spartan 6 FPGA board.

REFERENCES

[1] Roland E. Best, "*Phase Locked Loops Design Simulation and Applications"*, McGraw-Hill, 5th Edition.

[2] Qiang Zhang, "Research and application of all digital phase locked loop", *Intelligent Networks and Intelligent Systems School of Electrical Engineering and Automation*, Hebei University of Technology, Tianjin, China Conf., 2009.

[3] K.T.lbrahim,and A.E Salama, "Digital Of ADPLL for Good Phase and Frequency Tracking Performance", *Nineteenth National Radio Science Conference, Alexandria, March 2002*.

[4] Riad Stefo, Jorg Schreiter, Jens-Uwe SchliiOler and Rene SchiiRny, "High Resolution ADPLL Frequency Synthesizer for FPGA- an based Applications", *Department of Electrical Engineering and Information Technology Dresden University of Technology, Germany.*

[5] Indrani Hatai, and Indrajit Chakrabarti, "FPGA implementation Digital FM Modem", *Information and Multimedia Technology Electronic and Electrical Communication Engineering Indian Institute of Technology, Kharagpur, India, Conf., 2009.*

[6] Martin Kumn, and Harald Klingbeil, "An FPGA-Based Linear All Digital Phase-Locked Loop", *IEEE transaction on circuit and systems, VOL 57, NO.9, September 2010.*

[7] Aniruddha Chandra, "Phase Locked Loop", ECE Department, NIT Durgapur, *Winter School on VLSI Systems Design, WB, Jan24, 2009*.

[8] Rosink,W.B., " All-Digital Phase-Locked loops Using the 74HC/HCT297 ", Philips componenets,1989.*(Available in the United states from Philips Semiconductors),811 east Arques Ave.,Sunnyvale , CA 94088*

[9] Manoj Kumar andKusumLata, "ADPLL Design and implementation on FPGA", 2013 International Conference on Intelligent Systems and Signal Processing (ISSP)

[10] Manoj Kumar andKusumLata, "ALL Digital Phase-Locked Loop (ADPLL): A Survey", Proceedings of the 4th IEEE International Conference on Electronics Computer Technology (ICECT 2012), April 6-8 2012, Kanyakumari, India.

[11] Supreetha Rao and Kiran Kumar V G, "VHDL Implementation of Optimized ADPLL and TMDS encoder for serial communication" June 2015 International Journal of Innovative Research in Technology.