Implementation of 2-Bit and 4-Bit Magnitude Comparator Using Fuller Adder

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Abstract- *In today's era, the digital VLSI circuit should have low power, high speed and small in size, these parameters plays very important role in VLSI designing. In this paper we present a new technique to implement 2-bit magnitude comparator and 4-bit magnitude comparator with the help of 2 –bit full adder and 4-bit full adder respectively. The Results of this paper is simulated on the Xilinx 12.1 tool.*

Keywords- full adder, VLSI, Low power, magnitude comparator.

I. INTRODUCTION

As in VLSI design there are some parameter on which design of a circuit is based for efficient design and results. Regularity in circuit designing decomposes into in similar block so that designing of different modules requirement vanishes. In ALU designing if similar modules are used then extra modules are not required, full adder can be used as adder/sub tractor. Here full adder is used to design comparator .As the number of bits increases for comparison n-bit full adder is required.

Comparator is a combinational circuit that compares two binary numbers and determines their relative magnitude and decides which number is greater, smaller or both are equal. Comparison between two binary numbers is widely used in computer systems. Digital comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of inputs. In this circuit we are having two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

A.1-Bit Magnitude Comparator

A comparator used to compare one bit binary number each number if 1- bit called a 1-bit Magnitude comparator. It consists of two inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

The truth table for a 1-bit comparator is given below:

Table 1. Truth table for a 1-bit comparator

Inputs		Outputs		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Form the truth table-I we get expressions of three outputs which are as follows:

$$(A>B)= AB' \quad (1)$$

$$(A=B) = AB'+A'B \quad (2)$$

$$(A<B) = A'B \quad (3)$$

Circuit diagram of 1-bit comparator is shown below:

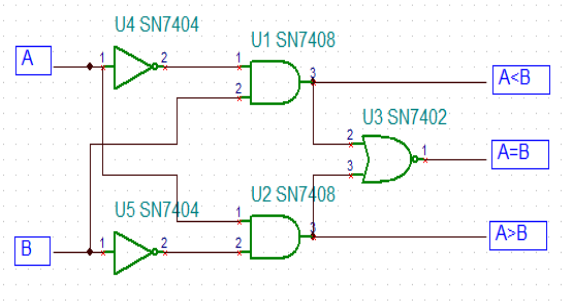


Figure 1. Circuit diagram of 1-bit comparator

B.2-Bit Magnitude Comparator

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

The truth table for a 2-bit comparator is given below:

Table 2. Truth table for a 2-bit comparator

Inputs				Outputs		
A1	A0	B1	B0	G	E	L
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Simplified expressions for compared results from Table 2 are obtained with the help of K-map and by the equations are given below:

$$(A > B) = A1\ B1 + A0\ B0\ X\ 1;$$

where $X\ 1 = A1B1 + A1\ B1$ (4)

$$(A = B) = X\ 1\ X\ 0;$$

where $X\ 0 = A0\ B0 + A0\ B0$ (5)

$$(A < B) = A1B1 + A\ 0\ B0\ X\ 1 \quad (6)$$

According to the above mentioned equations the circuit diagram of 2-bit comparator is as follows:

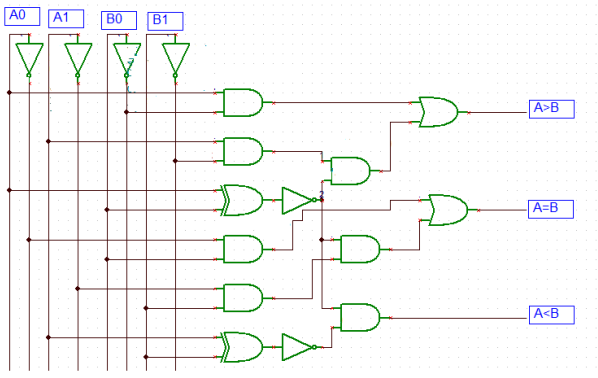


Figure 2. Circuit diagram of 2-bit comparator

II. PROPOSED DESIGN TECHNIQUES FOR MAGNITUDE COMPARATOR

Magnitude comparator can be implemented by using different techniques; here the proposed design of comparator is implemented by using the Full adder.

A. Designing of comparator by using full adder.

In full adder we have three inputs and two outputs. For designing of comparator, uses only two inputs and third input is grounded always.

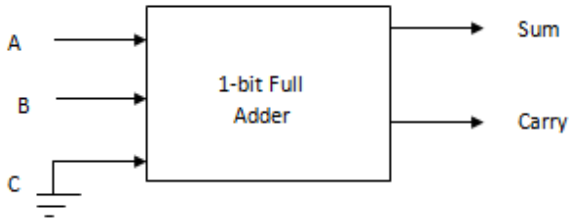


Figure 3. Circuit diagram of full adder as comparator

Since full adder has only two outputs, so to make it compatible with comparator only two outputs of comparator is taken while the third output will be obtained by these two outputs.

III. SIMULATION RESULT ANALYSIS

The proposed comparators are implemented in Verilog and designs are synthesized using Xilinx ISE 12.1. Simulation is done to verify the functionality of each design. Further, design metrics such as area, power and delay are extracted. Following subsections provides the simulation results and their analysis for the proposed comparator.

A.1-bit magnitude comparator

The 1-bit comparator is coded in Verilog and implemented on Vertex7. The designs are synthesized using Xilinx ISE 12.1 and schematic is created. The RTL schematic of the comparator and is detailed view is shown in fig.4

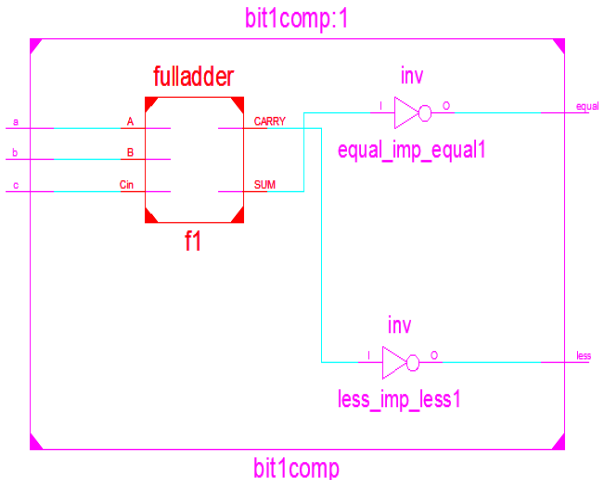


Figure 4. Schematic of 1-bit comparator

Further to check the functionality, the input is applied and output is checked. The simulation waveform of the 1-bit comparator is shown in Figure 5.

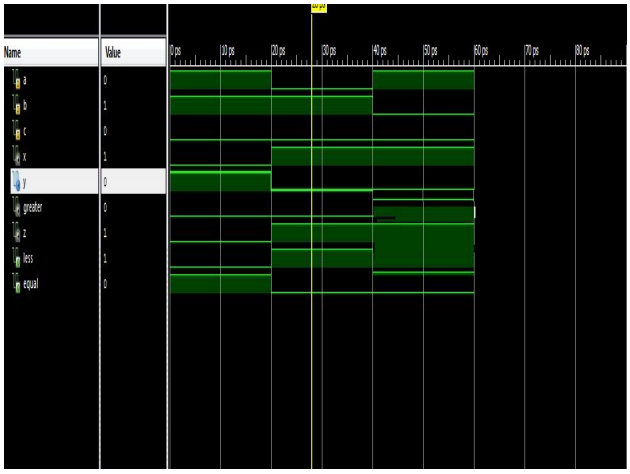


Figure 5.Waveform showing input output of 1-bit comparator

B.2-bit Magnitude comparator

Similarly 2-bit and 4-bit comparator is coded in Verilog and implemented on Vertex7. The designs are synthesized using Xilinx ISE 12.1 and schematic is created. The RTL schematic of the comparator and is detailed view is shown in fig.4

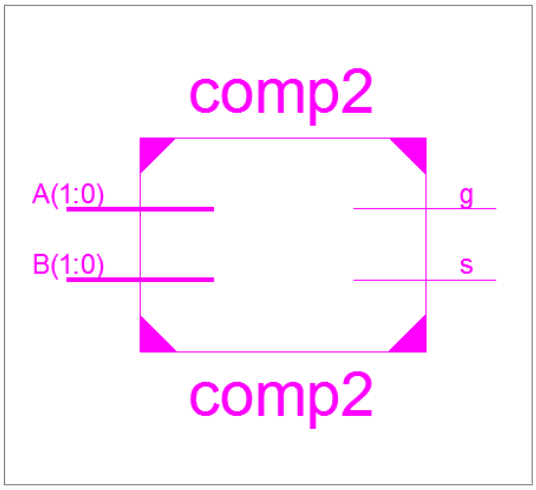
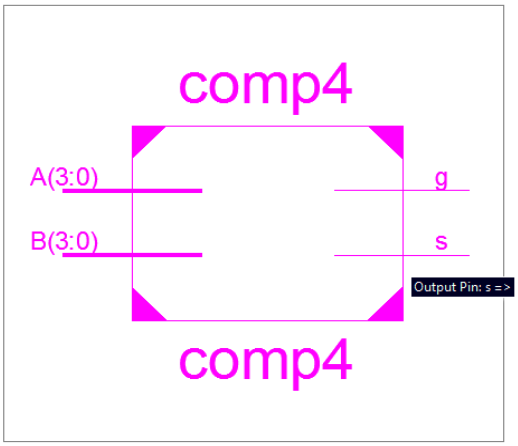


Figure 6. (a) Schematic of 2-bit comparator



(b) Schematic of 4-bit comparator

Waveform of 2-bit and 4-bit comparator is shown below.

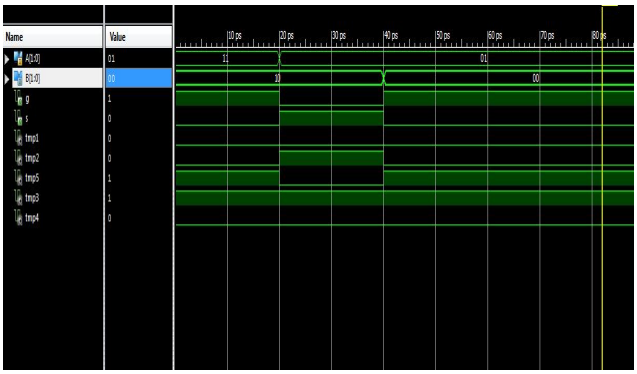


Figure 7. (a)Waveform showing input output of 2-bit comparator

(b)Waveform showing input output of 4-bit comparator.

Table shows the important parameter of design such as area, power and delay of proposed designs.

Table-3 Design Parameters of proposed designs

N-bit comparator	Area (LUTs)	Delay (ns)	Power (mW)
1-bit	2	5.776	3.4
2-bit	2	5.776	3.4
4-bit	6	6.774	3.4

IV.CONCLUSION

This paper presents the concept of designing magnitude comparator using full adder . The proposed magnitude comparators are implemented in Verilog and processed with Xilinx ISE tool chain. Further the designs are synthesized and post synthesis results are extracted. Using full adder to implement comparator will play important role in ALU designing due to regularity in whole design.

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