A Dual Output High Gain Step Up Coupled Inductor DC-DC Converter With Avmn for Multiple Applications

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Abstract- *A dual output ultra large gain step up inductor coupled DC-DC Converter with AVMN (Asymmetric voltage multiplier network) for multiple applications for sustainable energy system is proposed. This paper discuses on how the dual output can be achieved along with a very high voltage gain. For that a high step converter, a lossless passive clamped circuit, three winding coupled inductor are used. The circuit in [8] is again cascaded by using one extra winding to the secondary of the coupled inductor, hence achieving two outputs. The benefit of the proposed circuit is, with a single input it can serve two loads which are independent of each other and outputs can be used for different applications. Finally, a prototype circuit with switching frequency 50KHz, with the single input voltage of 20v, dual output up to 230v and 240v output voltage is attained and output power of 230 W from the proposed system is achieved using MATLAB/ SIMULINK.*

Keywords- AVMN, three winding coupled inductor, high step-up converter.

I. INTRODUCTION

As renewable energy sources are in great demand nowadays because of the increase in population and due to energy crunch especially in the field of power systems that are reliable on the renewable energy sources, which includes fuel cells, solar photovoltaic panels,etc. and these energy sources are associated with power converters that can efficiently convert various energy sources to work through modern electrical grid systems [1]. But, these renewable energy sources cannot offer adequate dc voltage for producing ac line voltage. Thus, the step-up converters are often implemented for conversion of low-power applications.

Ideally voltage gain can be improved by using a conventional boost converter. Though the voltage gain is achieved it includes a very high duty ratio. And having a high duty ratio would cause reduction in efficiency, electrical disturbances, and diode reverse recovery issues. Many research were made in order to get high voltage gain with less duty cycle. A circuit which integrates a switched-capacitor (SC) circuit within a boost converter was proposed [2]. By simply increasing the number of capacitors, high voltage ratio can be achieved, but this circuit would cause high surge current. Switched-inductor technology also encompasses the voltage gain and reduces the voltage strain of the switch. However, the voltage stress of the switches of converters is still high, and so the high--rated voltage switch persuades serious conduction losses [3]. By the voltage lift method, large step-up voltage gain could be attained by the transmitted energy from the intermediate capacitor, but unfortunately, the voltage and current stress on the intermediate capacitor are severe [4].In [5] the coupled-inductor technique had been used, the converters could attain the high step-up voltage gain by changing the turn's ratio of coupled inductor. However, the leakage inductance of leakage inductance of the coupled inductor will cause a high voltage spike on active switches when the switch is turned OFF. The active clamp circuit is proposed to absorb the energy of voltage spike on active switch so the voltage spike is effectively reduced, but reduction is efficient and extra cost adds [6].A negative clamp circuit technique is adopted [7] in the converters which not only reprocess the energy of the leakage inductor to increase efficiency, but also increases the voltage gain and hence high step-up converter, which successfully integrates coupled-inductor technology and voltage lift technology. Here the proposed converter can achieve a high step-up voltage gain and reduce the voltage stress on the main switch. However, the leakage inductor of the coupled inductor may cause high power loss and voltage spike. Thus, a passive lossless clamped circuit that is the part of the proposed is introduced, and it not only can recycles the leakage energy and reduce the voltage spike on the main switch, but also improves the voltage gain effectively. Moreover, three diodes have no reverse-recovery problem due to ZCS turn-off, the reverse recovery problem of the output diode is also alleviated by the leakage inductor. Thus, the performance of the conventional converter can be further improved [8]

In this paper, the circuit in [8] is modified to obtain dual outputs which can be used for multiple applications. . The benefit of the proposed circuit is, along with high voltage gain we can also achieve multi outputs with single input. Thus making the converter more efficient, multipurpose, and cost effective.

II. PRINCIPLE OF OPERATION

Fig 1 shows the equivalent circuit of Step-Up Coupled-Inductor with AVMN DC–DC Converter by combining a traditional boost converter with AVMN. The voltage-doubler circuit lifts of the output voltage by increasing the turns ratio of coupled-inductor. The advantages of proposed converter are as follows: 1) through adjusting the turns ratio of coupled inductor, the proposed converter achieves high step-up gain that renewable energy systems require 2) leakage energy is recycled to the output terminal, which improves the efficiency and alleviates large voltage spikes across the main switch 3) due to the passive lossless clamped performance, the voltage stress across main switch is substantially lower than the output voltage.

In order to make the circuit analysis simpler, the following assumptions are made. They are as follows:

- Consider the capacitors C1, C2, and C0 are sufficiently large so that for one switching period the voltages on them are considered to be constant.
- Assume zero voltage drop across diodes and switch and the unwanted turning on and off of the switch is ignored.
- The coefficient of coupling ‘k’ of coupled inductor with turns ratio ‘N’ is equal to Lm /(Lm + Lk1).

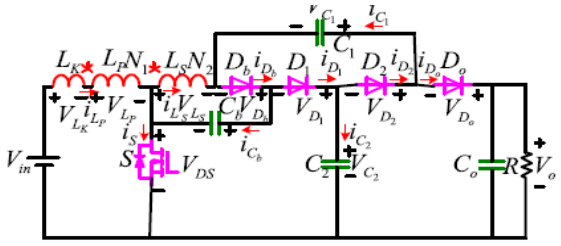

Fig.1 Equivalent circuit of Step-Up Coupled-Inductor with AVMN DC–DC Converter.

A. Modes of Operation

MODE 1: (t0 ≤ t ≤ t1)

During time interval t0 switch S is turned The diode Db is turned ON and D1 , D2 , and Do are turned off. The current I_{lp} is still increased and the clamp capacitor Cb is still charged by the secondary side winding. Moreover, the output capacitor C0 provides its energy to the load. When the current of the secondary side winding is equal to zero, this operation ends.

MODE 2: ($t_1 \le t \le t_2$)

Mode II [t1, t2]: During this time interval, the switch S is still turned ON. The diodeD2 is turned ON and the diodes D1, Db , and Do are turned OFF. The current-flow path is shown in Fig. 2(b). The capacitor C1 is charged by the secondary-side winding LS and capacitor C2. Besides, the energy needed by the load is supplied by the output capacitor Co .When switch S is turned OFF, this operating mode ends. Therefore, VC1 can be expressed to be

$$VC1 = NV_{lp}^{II} + Vc_2 \qquad 1$$

MODE 3: ($t_2 \le t \le t_3$)

Mode 3 [t2, t3]: At t = t2, D1 and D2 are turned on Moreover, Db and Do are turned off. The current-flow path is shown in Fig. 2(c). The capacitor C2 is charged by the input source, primary winding, and clamp capacitor Cb. Therefore, the passive lossless clamped circuit not only recycles leakage energy, but also effectively reduces the voltage spike on the switch S. Besides, the capacitor C1 is charged by the secondary-side winding LS and the capacitor Cb though the

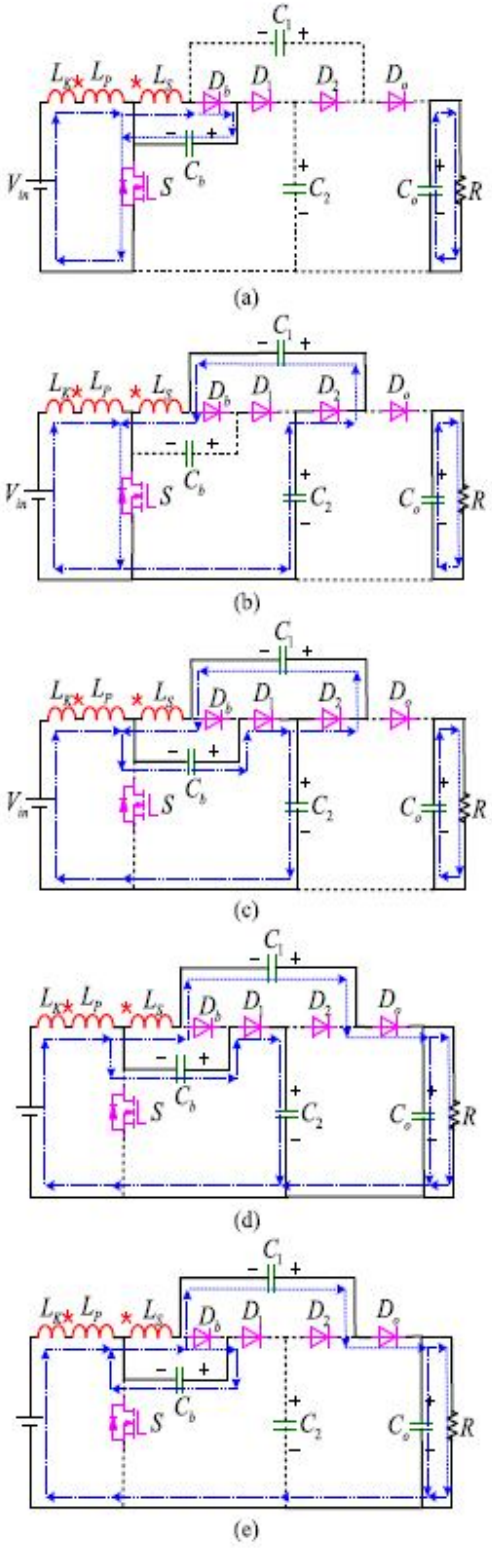

Fig. 2. Current-flow path of he operating modes during one switching period at CCM operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.[8]

diodes D1 and D2, . As soon as the current i_{D2} is equal to zero, operation goes to mode 4.

MODE 4: ($t_3 \le t \le t_4$)

Mode 4 [t3, t4]: During this time interval, the switch S is still turned off. Diodes Db and D2 are still turned off. Besides, the diodes D1 and Do are turned on. The current-flow path is shown in Fig. 2(d). Therefore, the energy that is from the input source, the secondary-side winding, and the primary-side winding of the coupled inductor and C1 is released to the output capacitor Co and load. At the same time, the capacitor C2 is charged by the input source and clamp capacitor Cb .When current iD1 is equal to zero, this mode ends. Therefore, V_{Cb} and Vo can be expressed as

$$V_{C2} = V_{in} - V_{lk}^{IV} - V_{lp}^{IV} + V_{Cb} \quad (2)$$

$$V_0 = V_{in} - V_{lk}^{IV} - (N+1)\, V_{lp}^{IV} + V_{C1} \quad (3)$$

MODE 5: ($t_4 \le t \le t_5$)

Mode 5 [t4, t5]: At t = t4, during this time interval, theswitch S is still turned OFF, and diodes D1 and D2 are turned OFF. The current-flow path is shown in Fig. 4(e). Besides, the clamp diode Db and output diode Do is turned ON. Therefore, the secondary-side winding LS charge the clamp capacitor Cb via clamp diode Db. Also, the input source, primary-side winding secondary-side winding, and C1 provide their energy to Co and load, and the current of the primary-side winding decreases. Therefore, V_{Cb} and V_{lp} can be expressed asandC1 provide their energy to Co and load, and the current of the primary-side winding decreases. Therefore, V_{Cb} and V^{V}_{lp} can be expressed as

$$V_{Cb} = -NV_{lp}^{V} \quad (4)$$

$$V_{lp}^{IV} = V_{lp}V \quad (5)$$

The same working principle of circuit (A) in Fig 1 is carried out for circuit (B) also of the proposed converter which can be clearly seen in simulink model as shown in Fig 3.

III. DESIGN GUIDELINES OF PROPOSED TOPOLOGY

A. Turns Ratio Design

Since the turns ratio of the coupled inductor determines the voltage stress of the switch and the operational duty-cycle of the converter, it is the key parameter in the circuit parameter design. A proper turns ratio can be obtained once the duty cycle is designed (in general, the optimal duty cycle is about 0.4−0.6), which is given by

$$N = \frac{V_o(1-D) - 2V_{in}}{V_{in}(1+D)} \quad (6)$$

B. Magnetizing Inductance Design

The magnetic average current of the coupled inductor can be represented by

$$I_{lm} = \frac{(N+2)I_o}{(1-D)} \quad (7)$$

The magnetizing inductor can be designed by setting an acceptable current ripple on the magnetizing inductor, which is given by

$$L_m \geq \frac{DV_{in}}{K_{lm}\, I_{lm}\, F_s} \quad (8)$$

From equations 7 and 8, the magnetizing inductance can be computed as

$$L_m \geq \frac{DV_{in}\,(1-D)}{K_{lm}(N+2)\, I_o\, F_s} \quad (9)$$

Where, K_{lm} is the ripple current coefficient

C. Output Capacitor Design

The aim of the output capacitor Co is to limit the output voltage ripple ΔV to a reasonable range. When the switch is turned ON, the capacitor Co released energy to the load, the electric charge can be written as follows:

$$\Delta Q = I_o D T_s \leq C_o \Delta V \quad (10)$$

Therefore, the output capacitor can be chosen as

$$C_o \geq \frac{DV_o}{\Delta V\ R\ F_s} \quad (11)$$

Using the above equations we get the values of the parameters to be used for the practicle implementation and for conducting simulation.

IV. SIMULATION RESULTS AND PRACTICLE IMPLEMENTATION

Using MATLAB/ Simulink, simulation is carried out for the proposed converter and the parameters and their specification are mentioned below

MOSFET Switch S	IRFP4568
Diodes Db, D1, D2, Do	VF30200
Output capacitor Co	470 µF
Capacitors C1, C2	2.2 µF
Coupling inductors Core,	N = N2 : N1 = 2,
LP	137.6 µH,
LS	548.5 µH

The simulink model of the proposed Step-Up Coupled-Inductor with AVMN DC–DC Converter is shown in Fig 3. For a single input voltage V_{In} of 20v is given and here we get two high gain output voltage (Vo) on both circuit A and B. The output voltage of circuit A is obtained around 230v as shown in Fig 4 and that of circuit B is 240v a shown in Fig 5.Therefore proving that the change in load of one circuit will not affect the load in other circuit. Power more than 200W is achived with the proposed topology.

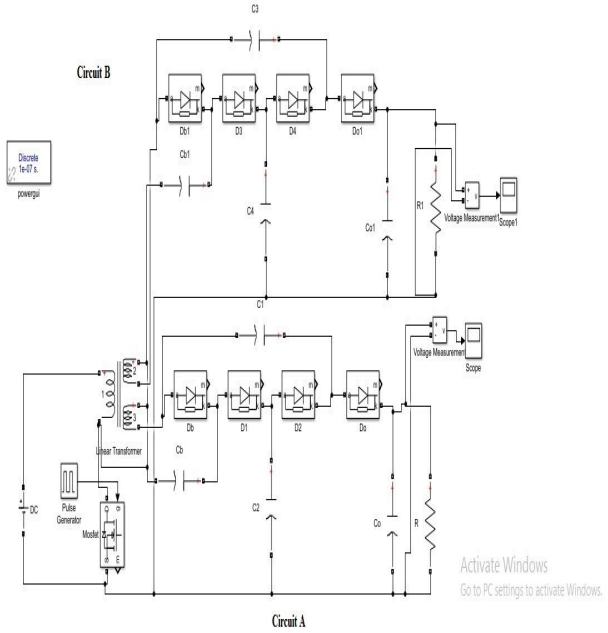

Fig.3 Simulink model of proposed Step-Up Coupled-Inductor with AVMN DC–DC Converter.

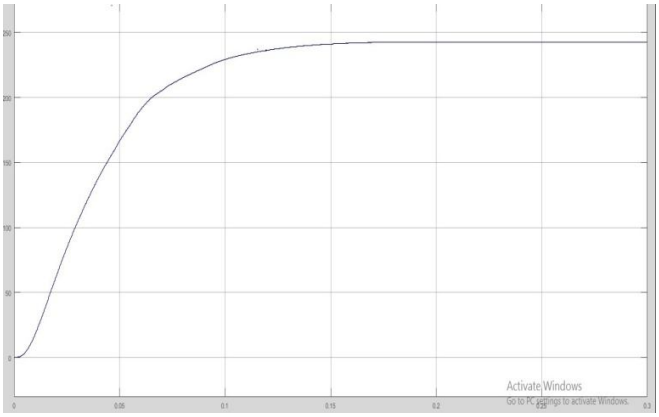

Fig 4 Output voltage of circuit A

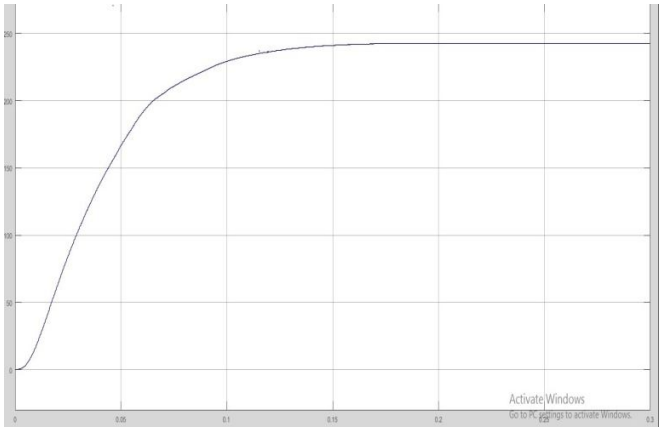

Fig 5 Output voltage of circuit B

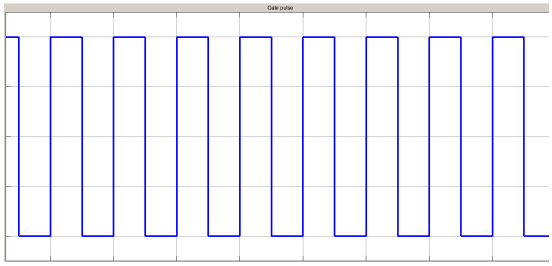

Fig 6 Gate pulses

Hardware implementation

The hardware model for proposed topology is shown in figure 7. T he block diagram is as shown in Fig 7. It consists of a 12v input battery which drives the Gate driver circuit, three winding coupled inductor, a MOSFET switch, DC converter with AVMN, Voltage regulators and load. In the experiment for a 12v input we can get around 110 step up dual output voltage .

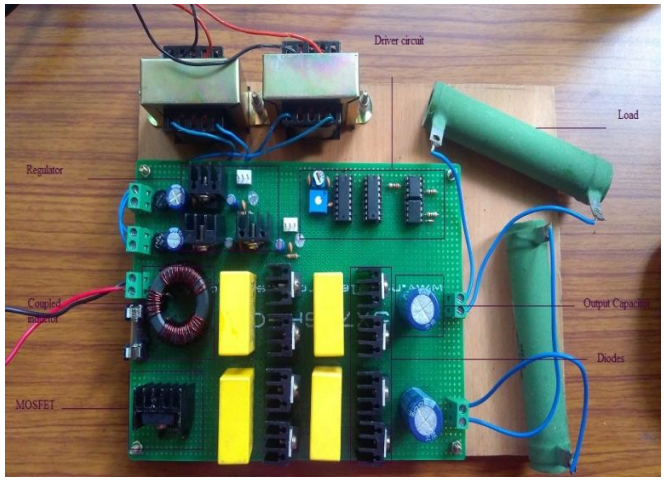

Fig 7 Hardware prototype

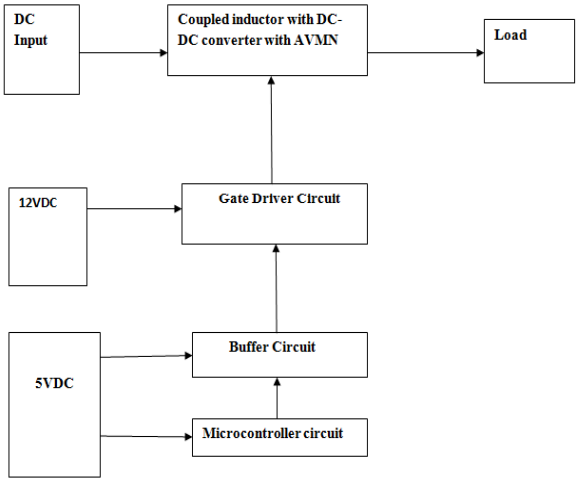

Fig 7 Block diagram of Hardware prototype

V. CONCLUSION

The circuit in [8] is modified to obtain dual output along with high voltage gain which can be used for multiple applications. Voltage strain on the main switch is reduced and therefore reduction losses. The design and experimental results proves the same. It can be used in HVDC systems, where one output can be used in transmission and other one can be used as home load accordingly.

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