A Simple Current Fed Quasi-Resonant Push-Pull Converter With Reduced Components And Improved Efficiency

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Abstract- *A Simple Current fed Quasi-Resonant Push-Pull Converter with Reduced Components and Improved Efficiency is presented which is suitable for low-voltage solar power cell conditioning system. The presented topology contains inherent advantages of voltage conversion ratio is high and low input stress of conventional push pull converter. At light load power switches can obtain soft switching improving the overall efficiency. Similar feature can be achieved with fewer components with the dynamic clamped current fed type push pull converter and current fed type push pull resonant converter, which enables to reduce the cost and system reliability..Proposed topology with design operations, output characteristics and proposed converter is simulated using MATLAB Simulink model at 100kHz and presented in the paper.*

Keywords- Current-fed, push-pull converter, fewer components, step-up.

I. INTRODUCTION

Renewable energy resources have become an important aspect in present scenario as it helps in achieving environ-mental friendly energy. This is possible as it reduces fossil fuel dependence which leads to harmful emissions affecting health and environment. Renewable energy resources achieve regeneration ratings quickly on regular standards considering the usage over indeterminate time period.

Solar energy is heat and light energy obtained from Sun. This energy is harnessed utilizing several developing technologies like photo voltaic, molten salt power plant, solar heating, artificial photo synthesis etc. Its harnessing technology can be broadly classified as either active solar or passive solar based on how this energy is captured, converted and distributed.

The solar energy which can be utilized varies depending on geography, cloud cover, time variation etc. This energy is not uniformly distributed over the entire globe and thereby is affected by geography. For example, solar radiation is more in regions near to equator than in regions away from equator. However, for regions that are far from equator, usage of Photovoltaics having capability to follow the sun's position can considerably increase harnessing of solar energy .

During night time availability of solar energy is very less for PV panels to absorb energy and hence time variation affects solar energy potential limiting amount of solar energy that can be captured per day by solar panel. Similarly cloud cover affects solar energy potential as clouds tend to block light coming from Sun and thus reduce availability of light to solar cells.

For generation of electricity using solar energy the output of PV cells are generally low and thus step up dc-dc converter with higher frequency, low input current ripple, higher conversion ratio and galvanic isolation to obtain higher voltage for interfacing PV cells to the grid.

Among the various dc-dc converters, step-up converter are available for solar cell application. They may be categorized as voltage fed converter[2]-[3] or current fed converter type[4]-[6].The significant property of voltage-fed type has the lower switching voltage rating that allow usage of devices which has low R_{ds}. This is enormously valuable in the high current low voltage application.

Another advantage of this converter is that , it doesn't have a self start problem which in turn reduces the system complexity. Even though with all the advantages mentioned above, the voltage fed converter has some of the limitations in the applications of solar cell, that is it contains high transformation ratio, which will result in higher leakage inductances which leads to greater duty cycle loss, greater pulsating input current, which will require an Inductor-Capacitor filter effecting in additional size and power loss , high circulating current through primary switches, and severe ringing of the secondary diodes.

To overcome the limitations of voltage fed converter , current fed converters are utilized. The Current fed type converter will naturally have low input ripple and High frequency transformer with low turns ratio due to which input inductor will provide voltage boosting and filtering, rectifier diode with lower rating because of negligible ringing of diode and effective clamping of voltage, no difficulty in duty cycle and lower risk of transformer saturation. Thus current fed type converters are found to be preferable than voltage fed type converters specifically for high current low voltage input applications. Usually there are many types of current fed converter topology are Full bridge converter[6], L-type Half bridge converter[7], Dual Boost converter[8] and Push-Pull converter.[9]-[11]

rectifier diodes.

Above mentioned converters have their own advantages and disadvantages. However Push-Pull converter is found to be more attractive because of simple circuit design with two switches only at the primary side as well as galvanic isolation, improved utilization of transformer and high conversion ratio of voltage. Nevertheless typical current fed type push pull converter has many disadvantages such as High frequency transformer leakage inductance results in high voltage spikes of switches, high voltage ratio, high reverse recovery effect of rectifier diode of the secondary side, power loss is increased when power devices are switched in hard switching mode.

A simple current fed quasi resonant push-pull converter with reduced components and improved efficiency is presented in this project work for low voltage applications. The presented topology is current fed type quasi resonant push-pull converter.

The typical current fed push-pull type converter mitigates the disadvantages of voltage fed type converter as mentioned in previous section. However typical current fed push-pull converter as many disadvantages such as high frequency transformers leakage inductance it will cause high voltage spikes in switches, high voltage ratio, reverse recovery effect of secondary rectifier diodes and power devices operating in hard switching mode will cause increased power loss.

The presented topology helps to resolve these problems as well as preserve default advantages of typical current fed type push-pull converter such as voltage conversion ratio is high and input current stress is low . Also , this topology offers soft switching of active power switches for light loads resulting in improvement of overall efficiency.

II. WORKING PRINCIPLE

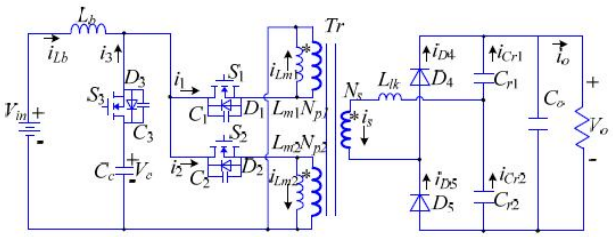


Fig. 1. Current Fed Push-Pull Quasi Resonant Converter

Figure 1 represents the schematic diagram of proposed converter. The main components of the presented topology are two main power switches S_1 and S_2 , one auxiliary switch S_3, input voltage source Vin, clamping capacitor C_c and input inductor L_b located at the transformer primary side . The primary winding N_{p1} N_{p2} and secondary windings Ns represented high frequency transformer Tr. The leakage inductance of transformer is referred to secondary side by L_{lk}. Voltage doubler rectifier circuit comprising of diodes D_4; D_5 and capacitors $C_{r1}C_{r2}C_o$ constitutes the output. Diodes $D_1D_2D_3$ are the anti-parallel body diodes of power switches $S_1S_2S_3$ respectively.

Following are few assumptions considered. They are,

Power switches S_1 S_3 are assumed to be ideal switches having anti-parallel body diodes D_1 D_3 and body ca-pacitors C_1 C_3.

1) Capacitors C_0 and C_c are considered to be very large such that the voltage across them is constant.

2) $C_{r1}=C_{r2}=C_r$ and $C_1 = C_2 = C_3$ so that symmetric working is realized.

3) Diodes D_4 D_5 are assumed to be ideal.

4) The turns ratio of transformer is N_s:N_{p1} = N_s : N_{p2} = N, and magnetizing inductance is $L_{m1} = L_{m2} = L_m$; here magnetizing inductance is higher than leakage inductance.

5) The inductor L_b at the input side is assumed to be large enough such that input current flowing through it is constant during switching interval.

Interval 1: ($t_o \leq t < t_1$)

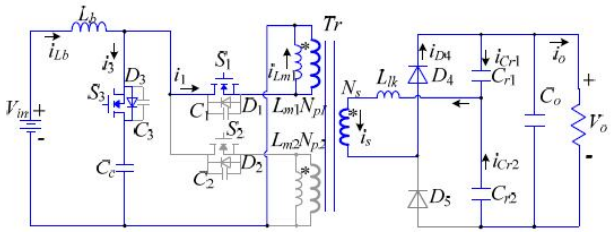


Fig. 2. Equivalent circuit for Interval 1

During time interval t_o, switch S 3 is ON by means of ZVS, S_1 is ON, S 2 is made OFF and diode D_4 gets forward-biased and results in free-wheeling. Consequently, power is supplied from source to load. Due to the effect of voltage clamping V_c on primary winding N_{p1} resulting nV_c across secondary winding, N_s. Owing to voltage difference between nV_c and v_{cr1}, leakage inductor, L_{lk} resonates with C_{r2} and C_{r1}.

$$L_{lk}\frac{di_s(t)}{dt} = nV_c - v_{cr1}(t) \qquad (1)$$

$$i_s(t) = C_{r2}\frac{dv_{cr2}(t)}{dt} - C_r1\frac{dv_{cr1}(t)}{dt} \qquad (2)$$

$$V_o = v_{cr1}(t) + v_{cr2}(t) \qquad (3)$$

where
v_{cr1} = voltage across C_{r1}
v_{cr2} = voltage across C_{r2}
Solving above equation , we get,

$$i_s(t) = [\frac{(nV_c - v_{cr1}(t_o))}{Z_r}]\sin\omega_r(t-t_o) = I_{speak}\sin\omega_r(t-t_o) \qquad (4)$$

$$v_{cr1}(t) = nV_c - [nV_c - v_{cr1}(t_o)]\cos\omega_r(t-t_o) \qquad (5)$$

where, $I_{spea\,k}$= peak value of i_s

Z_r and ω_r , are given as

$$Z_r = \sqrt{\frac{L_{lk}}{2C_r}}$$

$$w_r = \frac{1}{\sqrt{2L_{lk}C_r}}$$

where,
Z_r = Resonant impedance
ω_r = angular resonant frequency

Since $C_{r1} = C_{r2}$ and half-bridge circuit is similar to voltage-doubler rectifier, C_{r2},s charging current and C_{r1},s discharging current flow through D4 together as shown below

$$i_{Lm}(t) = -i_{cr2} = \frac{i_s(t)}{2} \qquad (8)$$

i_{Lm} = Transformer Magnetizing Current.
i_1 and i_3 are switch currents and given as,

$$i_{Lm}(t) = i_{Lm1}(t) = i_{Lm1}(t_o) + \frac{V_c(t-t_o)}{L_m} \qquad (9)$$

$$i_(t) = ni_s(t) - I_{Lb}(t) \qquad (10)$$

$$i_3(t) = i_(t) - i_{Lb}(t) \qquad (11)$$

where input current of inductor reduces linearly which results in the difference of voltage between V_m and V_c. Such as

$$i_{Lb}(t) = I_{Lb_max} + \frac{(V_in - V_c)(t-t_0)}{L_b} \qquad (12)$$

where I_{Lbmax} = peak value of i_{Lb} when secondary current (i_s) resonates to zero at t = t_1. i_1 is switching current which reaches magnetizing current i_{Lm1} and switch current i_3 the inductor input current i_{Lb}.

Interval 2: ($t_1 \leq t \leq t_2$)

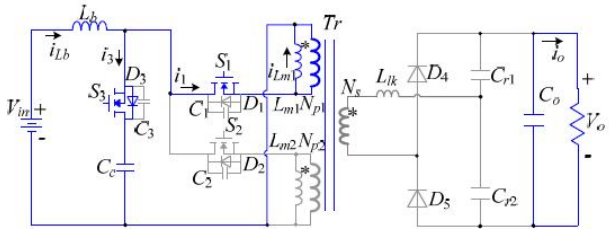


Fig. 3. Equivalent circuit for Interval 2

When t=t1 , i_s is the secondary current reduces to zero and the diode D_5 is made off with current being zero, in order to eliminate the reverse recovery problem . The i_{Lb} current reduces with same slope as interval 1 and magnetizing current flows through the switch S_1. The currents i_1 and i_3 can be expressed by

$$i_(t) = i_{Lm1}(t) = i_{Lm1}(t) + \frac{i_{Lm1}(t) + V_c(t - t_1)}{L_m} \quad (13)$$

$$i_3(t) = i_{Lm1}(t) - i_{Lb}(t) \quad (14)$$

When currents i_{Lb} and i_{Lm1} reach to their maximum and minimum values I_{Lm} and I_{Lbmin} respectively , at that time t = t_2 the switch is made OFF and interval is ended.

Interval 3: ($t_2 \leq t \leq t_3$)

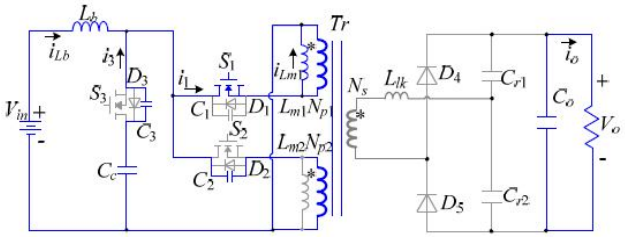


Fig. 4. Equivalent circuit for Interval 3

During time t = t2 switch current i_{3s} direction is determines either the voltage across C_3 will be charged to V_c that further results in the two cases .

Such as

Case 1 : Positive current i_3 implies that I_{Lm} & I_{Lbmin} discharges C_2 and charges C_3 it can be shown as

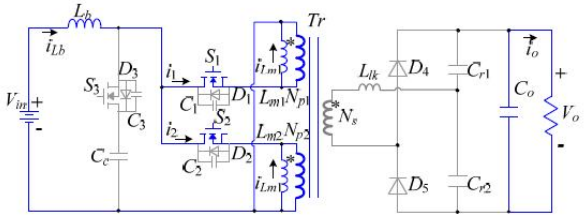
$$v_{C2}(t) = V_c - \frac{(I_{Lm} - I_{Lbmin})(t - t_2)}{2C} \quad (15)$$

$$v_{C3}(t) = \frac{(I_{Lm} - I_{Lbmin})(t - t_2)}{2C} \quad (16)$$

During the time t = t_3, voltage v_{c3} increases to V_c and v_{c2} decays to zero, then D_2 conducts providing ZVS condition for S_2.

Case II: Switch current i3 is negative, that also means I_{Lm} & I_{Lbmin} . In that case , the input current flows through anti parallel body diode D_3 until the next interval occurs.

Interval 4 : ($t_3 \leq t \leq t_4$)



Switch S_2 is made on with ZVS in the condition mentioned in interval 3 Case I, while S_2 is made on with hard switching and current which has been passing across D_3 flows into S_2. Since the main power switches S_1 and S_2 are made on voltage across the transformer winding is zero and input current i_{Lb} increases linearly which is given as

$$i_{Lb}(t) = \frac{I_{Lbmin} + V_m(t - t_3)}{L_b} \quad (17)$$

Due to the transformer flux balance relation and zero winding voltage, the magnetizing current is provided by two windings. Current iLm1 decreases from I_{Lm} to $I_{Lm}/2$ and i_{Lm2} increases from zero to $-I_{Lm}/2$ reversely.

The input inductor current i_{Lb} is equally divided and flows into S_1 and S_2 and therefore , i1 and i_2 can be obtained as

$$i_1(t) = \frac{i_{Lb}(t) + I_{Lm}}{2} i_2(t) = \frac{i_{Lb}(t) - I_{Lm}}{2} \quad (18)$$

The secondary rectifier diodes D_4 and D_5 are reverse biased and the output capacitor C provides energy to the load . The voltage across the secondary diode D_4 which is given by

$$v_{D4} = \frac{V_o}{2} - \Delta V_{cr} \quad (19)$$

where V_{cr} = maximum capacitor voltage ripple, which can be derived from average voltage

$$\Delta V_c r = \frac{I_o T_s}{[2(C_{r1} + C_{r2})]} \quad (20)$$

Interval 5: ($t_4 \leq t \leq t_5$)

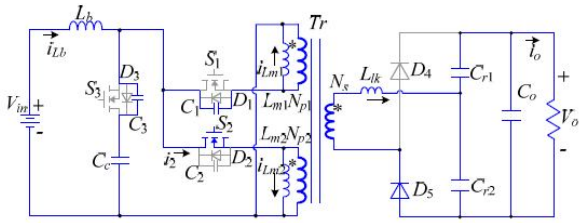


Fig. 6. Equivalent circuit for Interval 5

During the time t = t_5 I_{Lb} reaches to its maximum value I_{Lbmax} and turned made off. The current through S_1 is diverted into the auxiliary switch path causing the capacitor C_1 charges to $2V_c$ and C_3 discharges to zero quickly. Then , D_3 conducts providing ZVS turn-on condition for S_3.

During this interval, the magnetizing current that had been flowing through the winding N_{p1} transfers to N_{p2} and secondary current is starts slowly rising reversely due to the decrease of primary current i_1.

After t = t_5, S_3 is turned on with ZVS and the half cycle interval begins working, and the operation principle is similar with that of the former half cycle.

A. Control Strategy

PWM controls the output voltage with consistent switching frequency. In order to drive the main switches S_1 and S_2, and a complementary pulse with S1 and S2 to drive the auxiliary switch S3 gating signals are provided with two 180 out of phase with equal width owing the duty cycle more than 50% Main purpose of maintaining the duty cycle more than 50 % of main switches S_1 and S_2 to prevent the increased circulating current through auxiliary active clamped circuit. Operating duty cycle lower than 50%results in unwanted conduction power loss and low efficiency.

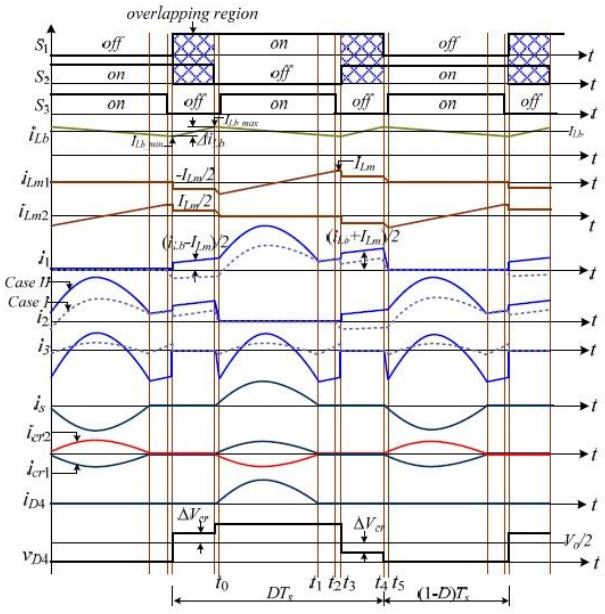


Fig. 7. Theoretical waveform of proposed converter

Fig. 7 represents the waveforms of the presented converter operating at the steady state, where Ts is the switching period of main switches. The overlapping region varies with duty cycle, which varies with the input voltage changing. Each switching period in the steady-state operation can be separated into ten phases. Because of the symmetry of the topology, only the former five stages are analyzed at length here and the corresponding equivalent circuits for each stage are illustrated in the intervals.

III. OUTPUT CHARACTERISTICS

From the equation (5) we know that the average voltage value of v_{cr1} is nV_c and v_{cr2} has the same average value. As the addition of v_{cr1} and v_{cr2} is V_0 , relation between V_c and V_o can be given as

$$V0 = 2nVc \qquad (21)$$

According to the volt-second balance principle of inductor L_b during the half switching period, then V_{in} and V_c can be related as

$$V_{in}(D - 0:5) + (V_{in} - V_c)(1 - D) = 0 \qquad (22)$$

by solving equation 22 voltage Vc can be written as

$$V_c = \frac{V_{in}}{2(1-D)} \qquad (23)$$

Hence, voltage gain can be give as

$$V_o = \frac{n V_{in}}{1-D} \qquad (24)$$

From equation (24) shows that voltage gain becomes hat of boost converter. It clarifies that the presented converter functions as step up converter in order to interface solar cell for the purpose of conditioning power.

A. Input Ripple Current

From the analysis of steady state operation, the input current i_{Lb} increases with slope of V_m=L_b and time duration is (D- 0.5)T_s. Hence the current ripple can be obtained by

$$\Delta I_{Lb} = \frac{V_m}{L_b}(D - 0.5)T_s \qquad (25)$$

with equation 24 and 25,we can written as

$$\Delta I_{Lb} = \frac{V_o(1 - D)(D - 0.05)}{nL_b f_s} \qquad (26)$$

where f_s = switching frequency.

IV. SIMULATION

Simulation is carried for open loop Current fed Quasi resonant Push- pull converter for fuel cell application is shown in figure 9 and Closed loop Current fed Quasi resonant Push pull converter for solar cell application is shown in figure 11. The components parameters are V_{in} = 50V, L_b = 45μH, C_r =10μF and C_o = 470μF.

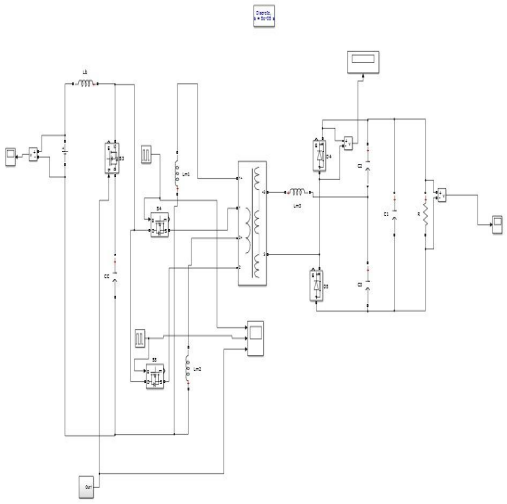


Fig. 9. Open loop simulation model for the presented converter topology

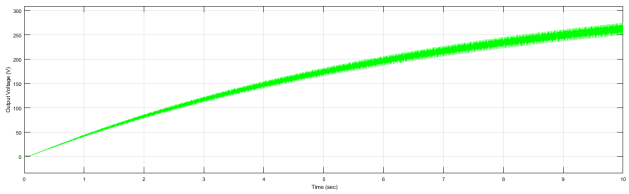


Fig. 10. Output waveform of open loop simulation model

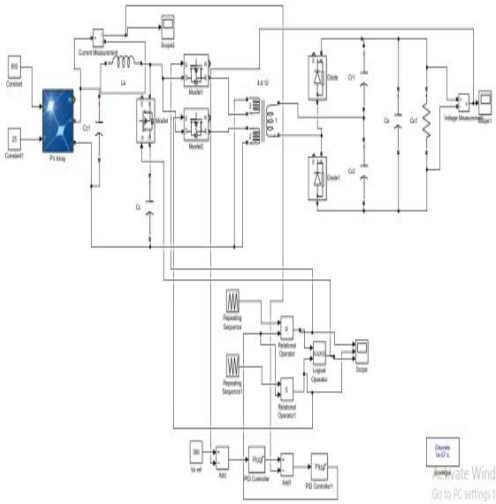


Fig. 11. Closed loop current fed quasi resonant push pull simulation model for solar cell application

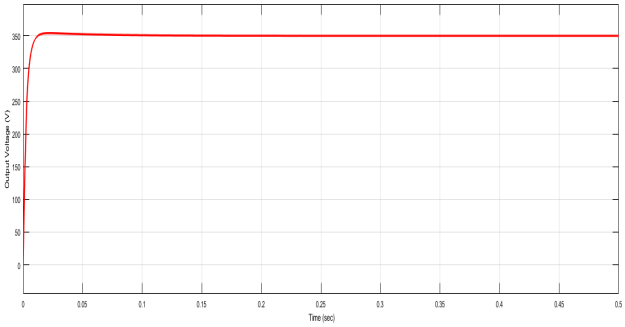


Fig. 12. Output Waveform of closed loop simulation model for solar cell application

V. EXPERIMENTAL RESULTS

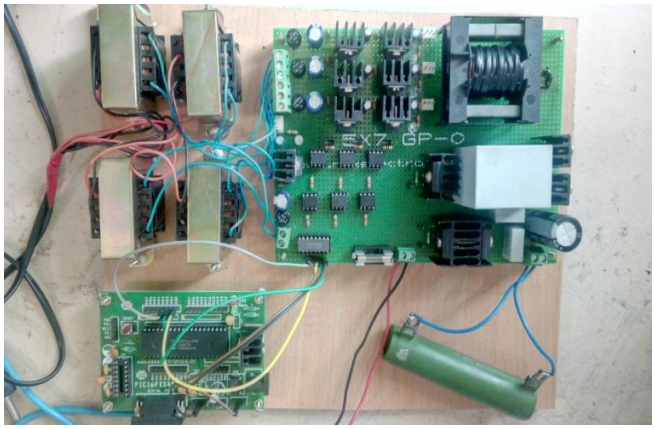


Fig. 13. Hardware Model

TABLE I COMPONENTS AND KEY PARAMETERS OF THE PROTOTYPE

Components	Parameters
Input voltage	12V
Output Voltage	84V
Switching Frequency	100kHz
Output power	126 W
Input Inductance	$L_b = 45\mu H$
Primary Switches S_1 - S_3	FDPF190N15A
Secondary Diodes D_4 ad D_5	SF5A400H
Resonant capacitor C_{r1}, C_{r2}	0.47μ F
Output filter capacitors C_o	$470\mu F$

The experimental result for output power and input voltage condition is shown in the table. Hardware model implementation gives the analytical study about steady state operation mentioned in the section II.

VI. CONCLUSION

A simple high step up quasi resonant push pull converter for solar cell was presented in this paper. By adopting the features of current fed structure and voltage doubler rectifier , voltage conversion ratio of higher standard is obtained without large turns ratio of transformer. Voltage doubler circuit helps to eliminate the reverse recovery problem of rectifier diodes and voltage spikes are suppressed by active clamped circuit and recycled energy is been stored in the leakage inductance. However compared to reported topologies, presented converter realizes the similar features with fewer components.

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