Design of Modified Data Driven Clock Gating And Look Ahead Clock Gating For Low Power

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Abstract- *Clock signal is considered as an immense source of power dissipation in synchronous circuits because of large frequency and load. It does not carry any information but consumes high power at the switching activity which is to be avoided. So, by using clock gating we can save power by reducing unnecessary transition activity inside the gated module.Hence modified design of data driven clock gating and look ahead clock gating is designed to obtain the less power in the circuits.These two techniques are compared among them and by the results obtained through cadence virtuoso tool we can conclude that look ahead clock gating consumes low power, low noise response and higher performance.*

Keywords- Multibit Flipflop,DDCG,LACG,Clock gating

I. INTRODUCTION

The sequential circuits in a system are considered as extensive contributors to the power dissipation.This is because that one input of sequential circuits is the clock, which is the only signal that switches every time for the appearance of inputs.The major dynamic power consumers in electronic products is the system's clock signal. In many cases, transition of the clock causes a great deal of irrelevant gate activity. Thus, the circuit power can be greatly decreased by reducing the clock power dissipation.So that, circuits are being developed with administrable clocks.Hence Clock gating can be enforced at all levels like system architecture, block design, logic design, and gates.So,this will allow the clock signal to be applied in the circuit in the controllable level. The clock signal applied to a flipflop is disabled when the flipflop state is not allowed to shift in the next clock cycle period. To reduce the aerial of the gating logic,several flip flops are combined and given the clone clock signal for its all operation.The combined all flipflop are named as multibit flipflop which also provides way for lesser power consumption the electronic devices.In this paper data driven clock gating and look ahead clock gating with modified design is done in the cadence virtuoso tool to obtain the very low power,low noise response,lesser delay,lesser bandwidth and efficient reliability in the electronic devices.The power consumption detail is obtained accurately in the cadence virtuoso power calculator window and also the noise response is also calculated using the same calculator window.The DC response analysis is also obtained for the modified design.

II. DATA DRIVEN CLOCK GATING

The data driven clock gating prospective is defined by its operation in a very clear manner.A FF finds out that its clock cannot be applied in the following cycle by XORing its output with the current data input that will also presented at its output in the following cycle. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, where those gating signal are latched to avoid flaw. The aggregation of a latch with AND gate is basically used by economic tools and is named as integrated clock gating.The modified part of this paper is in the combinational logic that is present in the circuit diagram where a new logic called Half Adder is used as combinational part which provides the clock enabling/disabling signal for the flipflop at the change of its each state in the circuit.

The half adder logic does not provide the clock power to the flipflop when the previous output of the flipflop and the present input of the flipflop are at same state.So that the clock power is not supplied to the flipflop because there is no switch of state. So the previously given clock power is itself enough to supply for the flipflop.Additionally it is not needed to give the clock signal power again in the following clock cycle.

The half adder logic gives the clock power to the flipflop when the earlier output of the flipflop and the present input of the flipflop are at different state that is toggle of the other input.So that the clock power is supplied to the flipflop because there is a change of state. So the previously given clock power is not enough to supply for the flipflop.Additionally,we demand to provide the clock signal power in the next clock cycle.By these logic at each clock cycle the power utilization is getting reduced which is required by all electronic circuits.

The circuit diagram of the data driven clock gating is shown fig.1 which performs the operation that is explained above.This modified design is implemented in cadence

virtuoso tool to analyse the power details, noise details and its other circuit parameters.

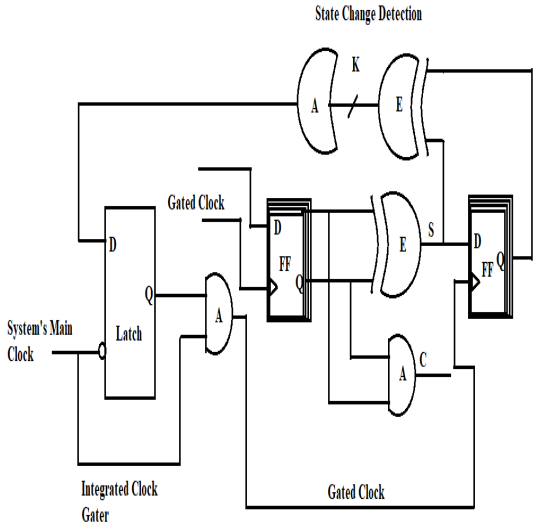

Fig 1. Data Driven Clock Gating

III. LOOk AHEAD CLOCK GATING

Look Ahead Clock Gating determines the clock start up signals of each FF one cycle beforehand of time, based on the current cycle input of those FFs on which it is purely based. This is advance than data driven clock gating because the clock gating circuit consists of flipflop based circuit for gating the clock power.Hence this reduces the majority of unnecessary clock pulses. It has a great advantage of eliminating the tight timing constraints data driven clock gating, by giving a full clock cycle for the enabling signals to be calculated and propagated to their gaters.

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The circuit diagram of the look ahead clock gating is shown in fig.2 which performs the operation that is explained above. This modified design is implemented in cadence virtuoso tool to analyse the power details, noise details and its other circuit parameters.

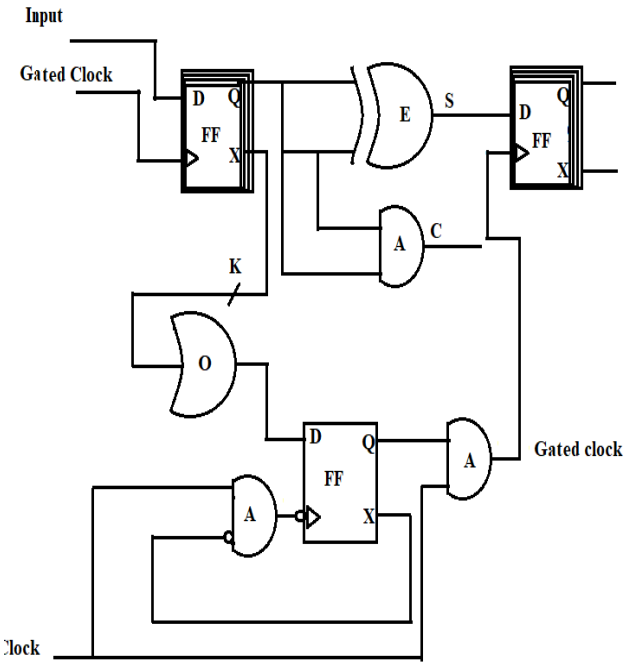

Fig 2. Look Ahead Clock Gating

The biggest advantage of the look ahead clock gating over data driven clock gating is that LACG provides largest timing window.Hence the biggest drawback of the DDCG is the shortest timing window.Further this advantageous clock gating logic(LACG) is applied in an application called LFSR(Linear Feedback Shift Register).LFSR is also implemented in cadence virtuoso tool as without LACG logic and with LACG logic.Both logic performance are compared and it is found that LFSR with LACG shows lesser power consumption and higher performance over the LFSR without LACG logic.So look ahead clock gating logic is the best suit for the devices to obtain the low power.

IV. LINEAR FEEDBACK SHIFT REGISTER

LFSR is a well-known circuit for pseudo-incidental number generation, which consists of N registers joined together as a shift register. The input to the LFSR comes from the XOR of distinct bits of the register.The output is moved into the leftmost bit of the register and the rightmost bit is moved into the output.LFSR is a sequential circuit basically worn in VLSI circuits, Communication field and in Spread spectrum communications.In the applications like pseudo-random bit generators (PRBGs), LFSR is used to generate an incidental sequence. An excellent PRBG is identified by repeatability and randomness.Linear feedback shift register circuit is very simple to be implemented, but the clock-path of all flip-flops (FFs) toggle at each and every clock cycle, so they consume a huge amount of power. The circuit diagram of the linear feedback shift register without look ahead clock gating (LACG) is shown below:

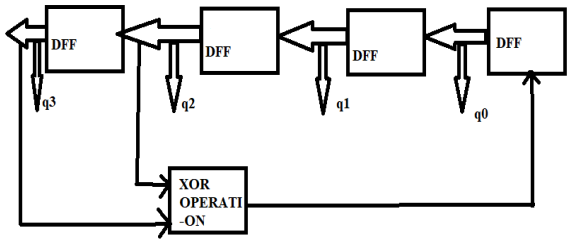

Fig 3. Schematic of LFSR without LACG Technique

The circuit diagram of the linear feedback shift register with look ahead clock gating (LACG) is shown below:

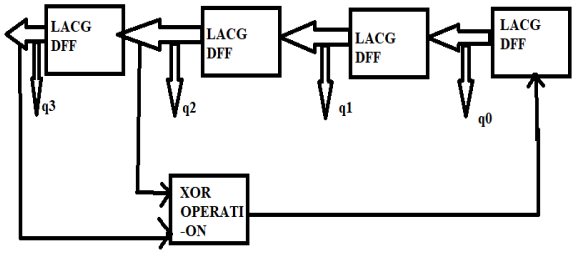

Fig 4. Schematic of LFSR with LACG Technique

Hence LFSR with LACG circuit shows low power consumption while implementing in cadence virtuoso tool.For this also noise response, DC response is obtained in the cadence virtuoso calculator window.

V. SIMULATIONS

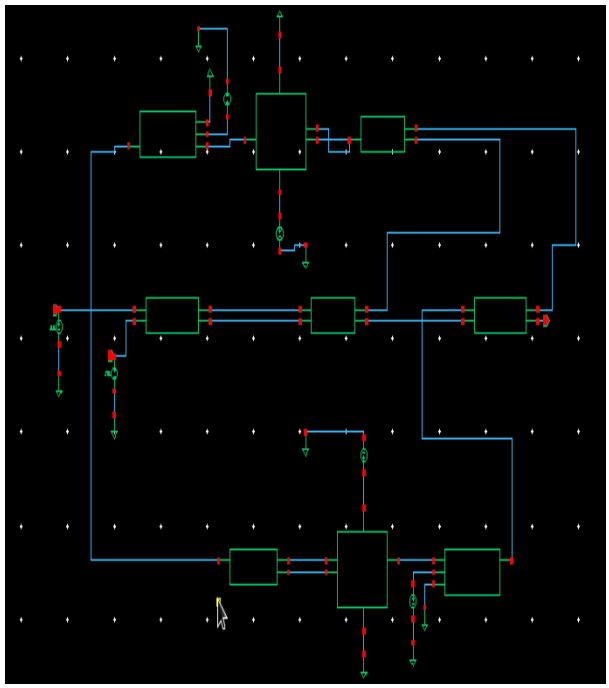

Fig 5. Data Driven Clock Gating in Cadence

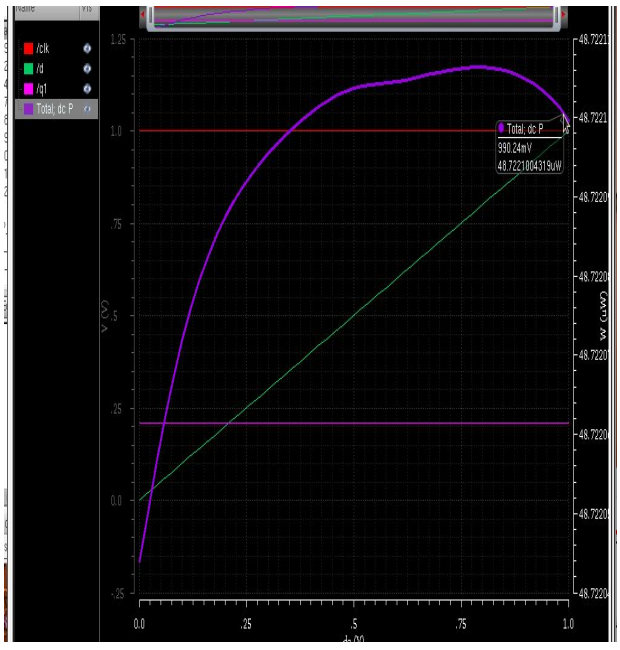

Fig 6. Power Response of data driven clock gating

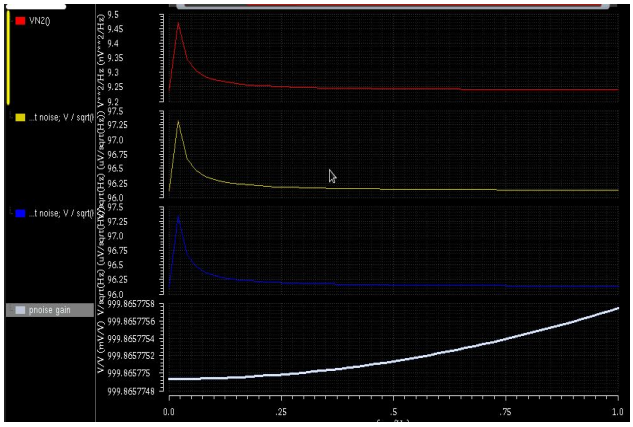

Fig 7. Noise Response of Data driven Clock Gating

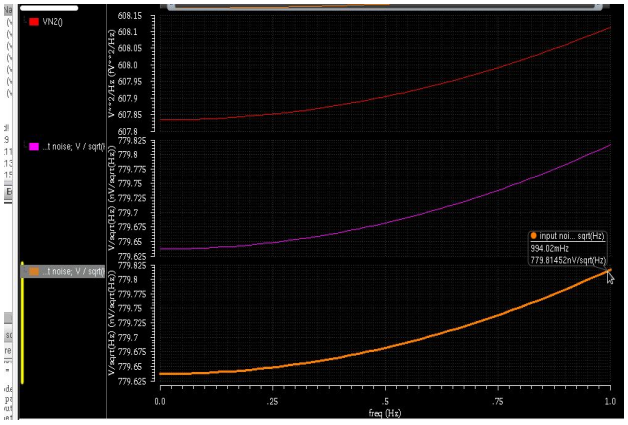

Fig 10. Noise Response of Look Ahead Clock Gating

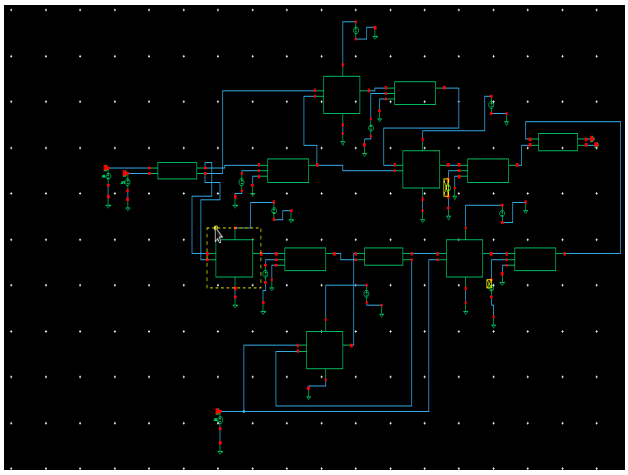

Fig 8. Look Ahead Clock Gating in Cadence

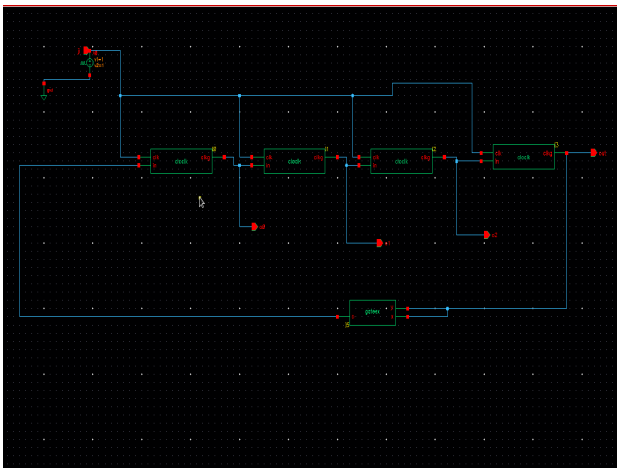

Fig 11. LFSR with LACG Clock Gating

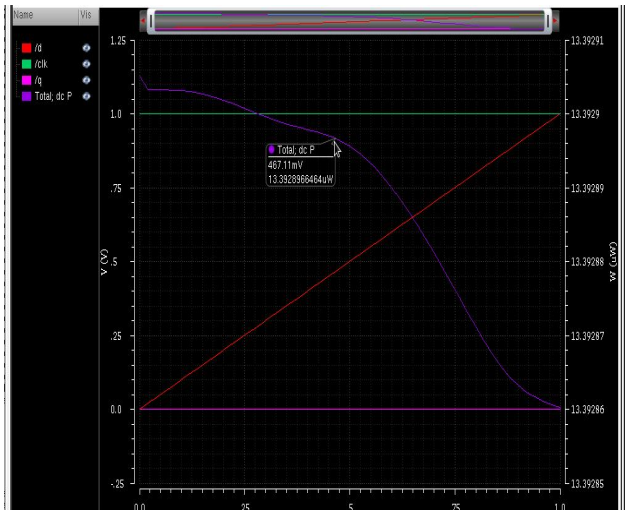

Fig 9. Power Response of Look Ahead Clock Gating

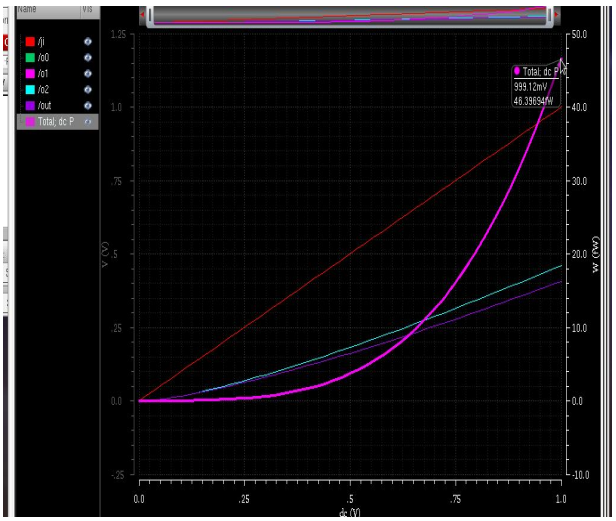

Fig 12. Power Response of LFSR with LACG Clock Gating

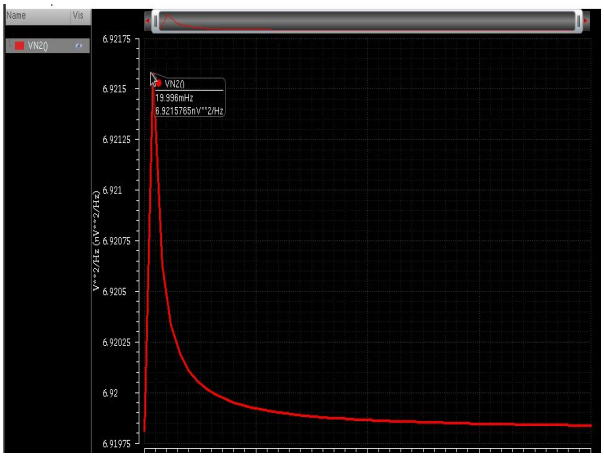

Fig 13. Noise Response of LFSR with LACG Clock Gating

TABLE I

S.NO	CLOCK GATING TECHNIQUES	TOTAL POWER	TOTAL NOISE
1.	DATA DRIVEN CLOCK GATING TECHNIQUE	48.7221uW	9.4710nV/sqrt(Hz)
2.	LOOK AHEAD CLOCK GATING TECHNIQUE	13.39288uW	0.6081pV/sqrt(Hz)

TABLE II

S.NO	LFSR	TOTAL POWER	TOTAL NOISE
1.	LFSR WITHOUT CLOCK GATING	0.0921pW	5.754nV/sqrt(Hz)
2.	LFSR WITH LACG CLOCK GATING	0.0463pW	1.126nV/sqrt(Hz)

VI. CONCLUSION

The modified design of data driven clock gating and look ahead clock gating is designed using cadence virtuoso tool and the power result is obtained which is compared as shown above in the table.As well as noise is also compared and it is found that look ahead clock gating is the best suitable clock gating technique with efficient performance.This clock gating can disable the redundant clock pulses in the devices and pave the way for low power devices in the electronic world.This can be applied at all sequential level circuits where clock power is a great source of power dissipation.

REFERENCES

[1] Hsu, Chih-Cheng, Mark Po-Hung Lin, and Yao-Tsung Chang, “Crosstalk-aware multi-bit flip-flop generation for power optimization,”Integr. VLSI J. vol. 48, pp. 146–157, 2015.

[2] C. Xu, P. Li, G. Luo, Y. Shi, and IH-R. Jiang, “Analytical clustering score with application to post-placement multi-bit flipflop merging,” in Proc. ACM Int. Symp. Phys. Design, 2015, pp. 93–100.

[3] S. Wimer and I. Koren, “Design flow for flip-flop grouping in data driven clock gating,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 4, pp. 771–778, Apr. 2014.

[4] Shmuel Wimer and Arye Albahari “A Look-Ahead Clock Gating Based on Auto-Gated Flip-Flops”, IEEE, 2014, Pp 1465-1472.

[5] Dr.Neelam R.Prakash and Akash,”Clock Gating for Dynamic power reduction in synchronous circuits”, IJETT, vol.4, issue 5, may2013.

[6] J. A. Kathuria, M. Ayoub, M.Khan, and A.Noor, “A review of clock gating Technique,” MIT Int. J. Electron. And Commun. Engin. vol.1, no.2, pp.106-114, Aug. 2011.

[7] S.-H. Wang, Y.-Y. Liang, T.-Y. Kuo, and W.-K. Mak, “Power-driven flip-flop merging and relocation,” in *Proc. ISPD*, 2011, pp. 107–114.

[8] W. Aloisi and R. Mita, “Gated-clock design of linear-feedback shift registers,” IEEE Trans. Circuits Syst., II, Brief Papers, vol. 55, no. 5,pp. 546–550, Jun. 2008.

[9] Qing Wu, Massoud Pedram and Xunwei Wu. “Clock-Gating and its Application to Low Power Design of Sequential Circuits”, IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, Vol. 47, No. 103, March 200