A Notch Filter For Biomedical Signal Acquisition System Using 22nm Technology For 50 Hz And 60 Hz Frequency

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Abstract- *This paper show the notch filter which is working at ±150 mV and 50 pA bias current. This is designed for EEG.ECG and EMG application where there is need of low power filter. The notch filter is sixth order and designed with the help of operational transconductance amplifier(OTA) . This OTA is bulk driven which makes this notch filter better candidate for biomedical system.*

This paper show attenuation for 50 Hz and 60 Hz of 57.73 dB and 52.45 dB and achieved lowest transconductance(gm) of 0.114 pA/V.also better phase shift as compared to other researches. This notch filter is consuming 10 pW from the supply. Whole circuit designed on 22 nm technology using tanner eda software.

Keywords- Notch filter, Biomedical, tanner eda, Transconductance, OTA.

I. INTRODUCTION

With the advancement in integrated circuit (IC) technology in the last few decades, it has been easy to realize portable acquisition systems which can monitor biomedical signals like electrocardiogram (ECG), electro-encephalogram (EEG),electro-oculogram (EOG)(figure 1.1) etc. However,these signals have relatively weak voltage levels and low frequencies and therefore design of such systems differs from conventional analog design. In addition to this, the development of such conventional analog design which can continuously and efficiently monitor physiological (biomedical) signals, at low 'cost' and with clinical accuracy, is gaining momentum. The 'cost' generally has two distinct components *viz.* the cost of the chip itself (which in turn is governed by the silicon area and the fabrication process) and the cost incurred to operate the device *i.e.* its power consumption. Good electronic design targets minimization of both these individual components of the cost. Further, the human physiological signals present design challenges in the form of very low-voltage and low frequency operating ranges. Therefore, the design of ultra-Iow power, low frequency biomedical signal acquisition analog front-ends has been an active area of research for the past years, and is still an open area of attention.

Signal	Amp. Range (mV)	Freq. range (Hz)
ECG	0.05 – 3	0.01 – 300
EEG	0.001 – 1	0.1 – 100
EOG	0.001 – 0.3	0.1 – 10

Fig.1.1 voltage and frequency range for EEG, ECG and EOG

Power line interference is also taken consideration while designing biomedical acquisition systems. Power line interference (noise due to AC mains at 50 Hz in countries like India or 60 Hz in the US) is one of the most intractable noise during physiological signal acquisition [1]-[2] which exists in most clinical situations**.**

The weak physiological signal can be easily contaminated by the power interference through electrode cables, electrical devices and/or the patient being monitored. For biomedical analogue front-end (AFE) circuits design, an effective way to eliminate the power line interference is with a notch filter following the pre-amplifier. However, a monolithically-integrated notch filter cannot be implemented by means of active RC structures due to the large resistors and capacitors values needed. Typically, integrated resistors and capacitors range from 1 ohm to 40 kilo ohms and 0.5 to 50 pF respectively [3]. These components may affect the functionality as well as die size will also become large.

Two effective ways of achieving low power consumption for biomedical applications are: *(i)* reduce the operating current, or *(ii)* lower the supply voltage. For designing in the ubiquitous

CMOS technology, lowering the operating current is achieved by biasing the MOSFET in the subthreshold or weak inversion region. In this region, the operating current is reduced to a

value much smaller than those in regions above the threshold voltage, which reduces power consumption. Although the 'poor' frequency response is often cited as a major pitfall of using the subthreshold region, in the case of design for biomedical applications, this limitation does not hamper the performance significantly. This is because the signals of interest are themselves of low frequencies (well below the 1 KHz mark for ECG, EEG, and EOG signals, and extending only up to 3 KHz for EMG signals). Lowering the threshold voltage can be achieved by making use of bulk-driven MOSFETs, in which the drain current is controlled by bu1k-to-source voltage with a constant gate-to-source bias, causing it to work as a Junction Field Effect Transistor (JFET) like device with negative, zero or slightly positive bias voltage.

II. LITERATURE REVIEW

Mohd. Samar Ansari[4] include design of CMOS OTA using 32nm technology and obtained transconductance of 65pA/V and attenuation of 17dB with supply of ±0.15V for 50 and 60 Hz.

Kaidi Du[5] designed low pass notch filter using tranconductance-conductance(Gm-C) for EEG application and obtain attenuation of 61.64 dB deep notch for 60Hz. Microcontroller and a feedback circuit can be added in future.

Haixi Li, Jinyong Zhang, and Lei Wang[6] integrate two NMOS current steering transistor in continous time integrator to design notch filter for 50Hz and obtained attenuation of 55.4dB at 50Hz notch frequency.

Chetali Yadav[7] focused on designing operational amplifier by keeping all transistor in sub-threshold region.
Tapsi Singh[8] designed and analyse folded cascode OTA in all the region of operations of mosfet.

Joel Gak and his friends[9] implemented cmos OTA using bulk degeneration concept where source and bulk both are connected. With this , they obtain power consumption of 500nA .

Rishika Sinha[10] obtained attenuation of 20dB for 50/60Hz with power consumption of 11.34nW at supply of ±0.95V and gm of 1.069 to 2.114 nA/V.

Ashish Kumar Mal and his friends [11] explain designing of folded cascade differential amplifier using potential distribution method. They found that design specification can be obtained in shorter time. They obtain voltage each node of the circuit and put this value current to get w/l ratio of each transistors.

Tripurari Sharan and his friend [12] shown the equation of drain current equation in subthreshold region with bulk driven. They have added Vsb term in the exponential part of drain current equation.

Chintala Yehoshuva and his friends[13] designed OTA for 0.5 V power supply and obtain minimum cutoff frequency of 100Hz and maximum cutoff frequency of 1KHz. Also obtain power consumption of 480nW. Whole design was designed on 180 nm.

Haixi Li, Jinyong Zhang, and Lei Wang[14] obtained 47.2 dB of attenuation for 50 Hz with power consumption of 120 pW. They use two OTA and obtained above results.

III. THEORY

In biomedical system, it consists of electrode, P(preamplifier), notch filter and ADC. Electrode will get the signals from the body, then signal is preamplifier with the help of preamplifier, notch filter will filter out the unwanted signal and ADC will convert analog to digital signal which can be observed on oscilloscope.

3.1 CMOS OTA

The OTA is basically a voltage controlled current source (VCCS) device who produces output current on the application of differential input voltage.

Its tunability is depended on transconductance which in turn depend on bias current and input voltage. Hence tunability is controlled by bandwidth of *gm*, which depends on the bias current. The term “cascade topology” refers to the cascade of a CS (common-source) stage and a CG (common-gate) stage which provides various valuable properties.

The expression for the output current of an OTA is given by
$IO = gm\ (V+ - V-)$
And the transconductance is given as
$gm = Ibias/2V_t$
where V_t: Thermal voltage = 26 mV at room temperature.
Ibias:Bias current.
The transconductance *gm* of the OTA is directly proportional to bias current Ibias. Characteristics of an ideal OTA are briefed as follows,
I/p impedance (*Zin*) = ∞
O/p Impedance (*Z0)* = ∞
Inverting i/p current *Io*-= Non-inverting i/p current *IO*+
Bandwidth = ∞

The circuitry of a folded cascades OTA is shown in Fig. 3.1.In folded cascade OTA the differential input stage provides the gain of the operational amplifier. because NMOS differential pair has greater mobility as compared to PMOS and provides a larger value of transconductance and gain, this pair is chosen. folding down of p-channel cascade active loads of a differential pair and changing the MOSFETs to *n*-channels satisfies folded cascade term. for large gain, high bandwidth performance and good PSRR compared to the two stage op-amp, the folded cascade is opted.

3.2 Notch Design

Above OTA is used to design notch filter. It is a band reject filter use to eliminate the power line frequency component in the signal. It is place before ADC block. Figure 3.2 shows the notch filter. This circuit diagram consists of six OTA, six capacitor, bias current and seven input voltage is applied depend upon the output to be plotted. Table 3.1 shown the settings to get the required output.

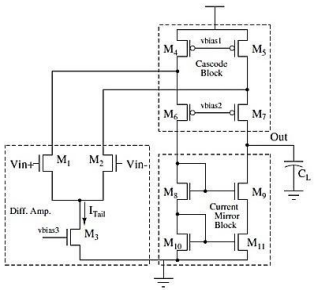

Fig 3.1 Circuit Diagram of a Typical Folded Cascode OTA

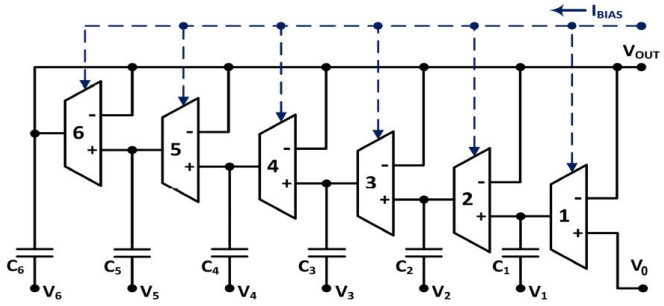

Fig 3.2 block diagram of notch filter[4]

This circuit diagram consist of six OTA,six capacitor,bias current and seven input voltage is applied depend upon the output to be plotted. Table 3.1 shown the settings to get the required output.

Table 3.1 Setting to be done for required output

V0	V1	V2	V3	V4	V5	V6	Output Response
0	0	0	0	0	0	Vin	Low pass
Vin	0	0	0	0	0	0	High pass
0	0	0	Vin	0	0	0	Band Pass
Vin	0	0	0	0	0	Vin	Band reject

In general, the expression for Vout for nth order, in terms of al the inputs(V0,V1.....V6) is

$$V_{OUT} = \frac{s^n V_0 + a_{n-1}s^{n-1}V_1 + a_{n-2}s^{n-2}V_2 + \ldots + a_0 s^0 V_n}{s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + a_0 s^0}$$

Where

$$a_k = \prod_{i=1}^{n-k} \frac{g_i}{C_i}; \quad k = 0, 1, 2, \ldots, (n-1)$$

As it can be observed from the expression that by selecting the number of OTA stages and input nodes, any filter can be realize. So to realize notch filter, the input nodes V0 and V6 are applied whereas other nodes are kept grounded. The following expression is obtained from said settings:

$$\frac{V_{OUT}}{V_{IN}} = \frac{s^6 + a_0 s^0}{s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0 s^0}$$

IV. DESIGN

4.1 CMOS OTA

4.1.1 Specification

Table 4.1 Specification for CMOS OTA

Parameter	Values
VDD	±150 mV
Technology	22 nm
Bias Current	50 pA
Trans-conductance(gm)	<18 pA/V

On the basis of specification mention in the table 4.1, the CMOS OTA is designed. This OTA is designed using potential distribution method [see appendix B for table].

4.1.2 W/L ratio

The voltage obtained on each node from potential distribution method will be use to design CMOS OTA i.e. width and length of transistor will be calculate. Table 4.2 shows the width and length of all the transistor for CMOS OTA [see appendix B for w/l ratio calculation].

Table 4.2 W/L ratio

Transistor	Width/Length
M1,2	55.5 nm/1 µm
M3	28 nm/100 µm
M4, M5	17 nm/10 µm
M6, M7	17 nm/10 µm
M8, M9	20.5 nm/10 µm
M10, M11	24.5 nm/10 µm

4.1.3 Schematic

Whole circuit(figure 4.1) is designed in tanner tool. The circuit consist of current source of 50 pA,four PMOS transistor,eight NMOS transistor and ±150 mV supply.

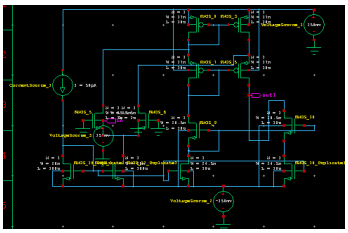

Figure 4.1 Schematic of CMOS OTA

4.2 NOTCH FILTER

4.2.1 Specification

Table 4.3 Specification for Notch filter

Parameter	Values
Notch frequency	50 Hz,60 Hz
Attenuation	>-30 dB
Power Consumption	<18 pW

The notch filter is designed for the above (table 4.3) specification. This notch filter is working for both the notch filter and attaining better attenuation for the mention notch frequency while consuming less power as mention in the table 4.3.

4.2.2 Extra component

Depending upon the output to be plotted, RC network is connected to the capacitor as inputs which in turn are connected at the output of each OTA. Table 4.4 shows the list of components connected to the notch filter for corresponding notch frequency.

Table 4.4 Component list

Notch Frequency=60 Hz		Notch Frequency=50 Hz	
Components	**Value**	**Components**	**Value**
Rseries	510 MΩ	Rseries	612 MΩ
Rperpendicular	255 MΩ	Rperpendicular	306 MΩ
Cseries	5.2pF	Cseries	5.2pF
Cperpendicular	10.4pF	Cperpendicular	10.4pF
C1-C5	10 pF		
C6	100 pF		

4.2.3 Schematic

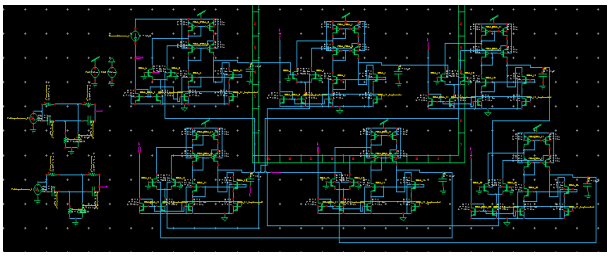

Fig 4.2 Schematic of notch filter

Figure 4.2 shown designed on tanner tool. Each OTA is receiving bias current of 50 pA. Circuit is also showing two RC circuit which is applied to the V0 and V6 input to realize as a notch filter.

V. RESULTS & COMPARISION

5.1 Results

5.1.1 Trans-conductance of OTA

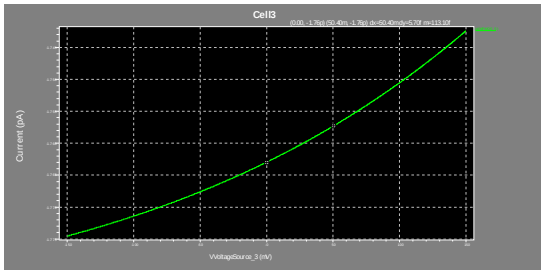

Fig 5.1 graph between input voltage and output current

The trans-conductance is obtained by plotting graph between voltage applied at the body of one input transistor while keeping body of another transistor ground and output current.

Simulation (figure 5.1) of this circuit shows trans-conductance(gm) of 0.114 pA/V which is the required value for gm.

5.1.2 Attenuation and Phase shift

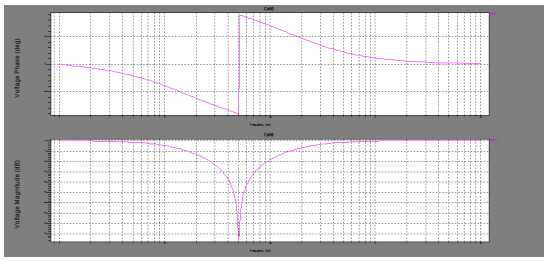

Fig 5.2 Amplitude and Phase responses of filter with notch at ACpower-line frequency of 50 Hz

As can be seen from Figure 5.2, at the notch frequency, an attenuation of about 57.73 dB along with phase reversals was observed

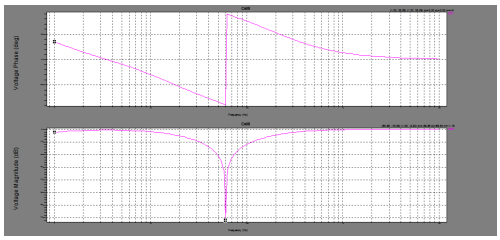

Fig 5.3 Amplitude and Phase responses of filter with notch at AC power-line frequency of 60 Hz

attenuation of same is observed (figure 5.3) as it was observed for 52.45Hz.

5.1.2 Power Consumption

The power consume by whole circuit is 10 pW which is again the required value by any biomedical system.

5.2 Comparison

Parameter/ References	[6]	[13]	[14]	[10]	[4]	This work
Technology (nm)	180	180	180	22nm	32nm	**22nm**
Power Supply(V)	1.8	0.5	0.5	±0.95	±0.5	**±0.5**
Gm(pA/V)	-	1000	1445	1069 to 2114	65.4	**0.114**
Power Consumption(W)	-	280n	120p	11.36p	18p	**10p**
Bias Current(A)	-	-	120p	1-2n	100p	**50p**
Attenuation (dB)	55.4-50 Hz	75-50/60 Hz	47.2-50 Hz	20-50/60 Hz	17-50/60 Hz	**52.45-60Hz 57.73-50Hz**

VI. CONCLUSION

Design of notch filter have been done using CMOS OTA on 22nm technology. All the transistor kept in subthreshold region which in turn consuming low current. Input transistor is bulk driven means input voltage is applied at body of transistor.

Potential distribution method is used to calculate the all the node voltage which helps in calculation w/l ratio for each transistor.

Supply of ±150mV is applied to the whole circuit consuming 10pW of power from bias current of 50pA. 47.8dB of attenuation is obtained for 50Hz notch frequency and 70 dB of attenuation for 60Hz notch frequency. CMOS OTA have trans-conductance of 0.114pA/V which make this design better candidate for biomedical system.

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