64 Bit Vedic Multiplier With High Fault Coverage

Renuka Talekar[1], Mayuri Chawla[2], Parinay Lavatre[3]
[1, 2, 3] Dept of VLSI
[1, 2, 3] Jhulelal Institute of Technology,Nagpur, India

Abstract- *The 64 bit Vedic multiplier using Urdhava Tiryakbhyam method is proposed. The ALU is the heart of any processor or the any complex system .To increase the speed of any system, it is required to increase the speed of ALU, but with low power consumption and for that portable life is required .Vedic multiplier gives faster processing speed in terms of array multiplier. VLSI designing techniques are the source to reengineering any digital electronics circuitry. In this paper a low power 64 bit ALU is designed in VHDL. Low power consumption is achieved with Vedic multiplier and energy recovery adder .As multiplier and adder are the most important functioning part of ALU .The speed of ALU is mainly depend on functioning of adder and multiplier. The idea to design Low power ALU is adopted from Vedic Mathematics. for this purpose Urdhva Tiryakbhyam Sutra is used from Vedic mathematics, due to that the complexity of circuit will reduce and power also get reduced.*

Keywords- Vedic multiplier,Urdhva Tiryakbhyam method, Vedic Mathematics ,64 bit multiplier ,Vedic Mathematics.

I. INTRODUCTION

Augmentation is a critical basic capacity in math activities. Augmentation based tasks, for example, Increase and Accumulate(MAC) and internal item are among a portion of the habitually utilized calculation Intensive Math Functions(CIAF) presently actualized in numerous Digital Signal Processing (DSP) applications, for example, convolution, Fast Fourier Transform(FFT), separating and in chip in its number juggling and rationale unit. Augmentation can be executed utilizing a few calculations, for example, exhibit, Booth, altered Booth calculations. Cluster multiplier is outstanding because of its standard structure. Multiplier circuit depends on include and move calculation. Each fractional item is created by the augmentation of the multiplicand with one multiplier bit. The halfway item are moved by their bit requests and afterward included. Stall Multipliers is an effective calculation for marked number duplication, which treats both positive and negative numbers consistently. This technique that will decrease the quantity of multiplicand products. For a given scope of numbers to be represented, a higher portrayal radix prompts less digits. The incomplete whole adders can likewise be reworked in a tree like mold, diminishing both the basic way and the quantity of snake cells required. The introduced structure is known as the Wallace tree multiplier The tree multiplier acknowledges considerable equipment investment funds for bigger multipliers. The spread deferral is decreased also. Indeed, it can be demonstrated that the spread deferral through the tree is equivalent to O (log3/2 (N)). While significantly quicker than the convey spare structure for extensive multiplier word lengths, the Wallace multiplier has the impediment of being change unpredictable, which confounds the assignment of a proficient format plan. Augmentation is a vital major capacity in number juggling activities. Augmentation based activities, for example, Multiply and Accumulate and internal item are among a portion of the much of the time utilized Computation-Intensive Arithmetic Functions as of now actualized in numerous Digital Signal Processing applications, for example, convolution, Fast Fourier Transform, separating and in microchips in its number juggling and rationale unit .

II. VEDIC MULTIPLIER

Vedic multipliers depend on Vedic Sutras. In Sanskrit word 'Veda' remains for 'information'. Vedic science is accepted to be reproduced from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918. The Vedic arithmetic has been separated into sixteen distinct Sutras which can be connected to any branch of science like polynomial math, trigonometry, geometry and so on. Its techniques diminish the intricate figurings into more straightforward ones since they depend on strategies like working of human personality accordingly making them less demanding. It has been seen that being rational and symmetrical, they devour lesser power and procure bring down chip region Vedic Mathematics manages Sixteen Sutras .These sutras are given underneath one after another in order with their concise significance. Every one of these sutras have tremendous examination. Discussion of all of them is beyond the scope of this paper. Only one Sutra number 14 "**Urdhva Tiryakbhyam**" has been discussed.

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero
2. Chalana-Kalanabyham– Differences and Similarities
3. Ekadhikina Purvena– By one more than the previous one
4. Ekanyunena Purvena– By one less than the previous one

5. Gunakasamuchyah– The factors of the sum is equal to the sum of the factors
6. Gunitasamuchyah– The product of the sum is equal to the sum of the product
7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10
8. Paraavartya Yojayet– Transpose and adjust
9. Puranapuranabyham– By the completion or non completion.
10. Sankalana-vyavakalanabhyam– By addition and by subtraction
11. Shesanyankena Charamena– The remainders by the last digit
12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero
13. Sopaantyadvayamantyam– The ultimate and twice the penultimate
14. Urdhva Tiryakbyham– Vertically and crosswise.
15. Vyashtisamanstih– Part and Whole
16. Yaavadunam– Whatever the extent to fits deficiency

III. URDHVA TRIYAKBYHAM SUTRA

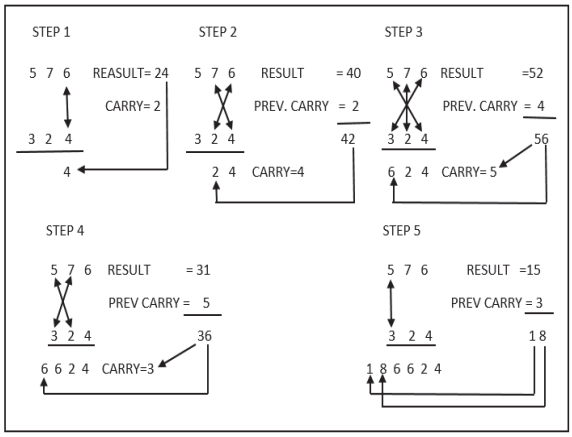

FIG.1 : VEDIC MULTIPLIER STEPS 3X3

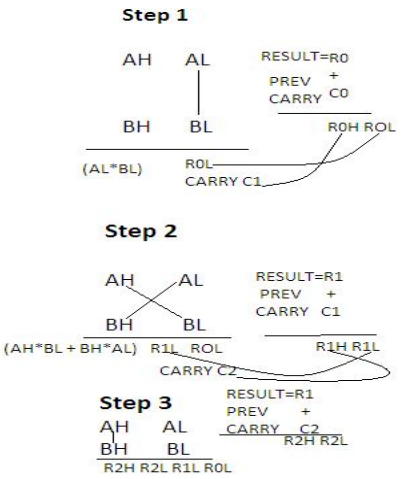

FIG.2 : VEDIC MULTIPLIER STEPS 2X2

The sutras in Vedic mathematics help to do almost all types of numeric calculations in easy and fast manner. This sutrais typically used for the multiplication purpose, applicable to all types of multiplication. Any bit binary number can bemultiplied quickly by using this sutra. The meaning of this sutra is vertically and crosswise. Given below summarize thegeneral process of the working of the Urdhva triykbyham sutra. For that we have consider here two number A and Bhaving digits AH and AL for A number and BH and BL for number. The result is in the form R0,R1,R2 and each timecarry is added in to each product i.e.C0,C1,C2. So there will no carry propagation occur in the result due to which delaywill be minimized. By using this sutra the carry will not propagated up to the higher level each time it will added to the product term, so time required to propagate carry up to higher level will be minimized. By designing this 2bit multiplier we have to design the 64 bit multiplier. Following block diagram shows the diagram for 64bit Vedic multiplier in the following fig shows the block diagram, RTL view and technology schematic and output waveform of 64bit Vedic multiplier.

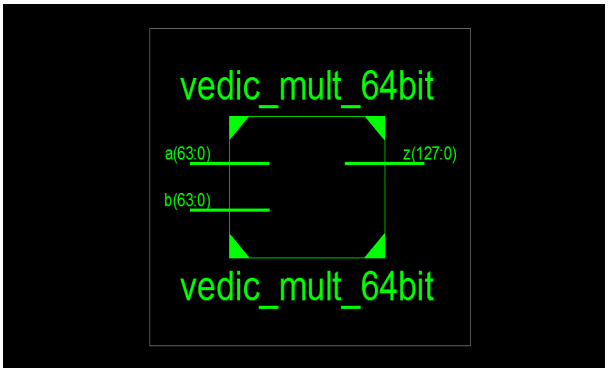

FIG.3 : RTL VIEW OF 64BIT VEDIC MULTIPLIER

FIG.4 : OUTPUT WAVEFORM OF 64 BIT VEDIC MULTIPLIER

IV. CONCLUSIONS

Vedic multiplier is essential part of any arithmetic and logical unit. Multiplier increases the speed of processor which reduces delay. The design of 64 bit multiplier using urdhava Tiryakbyham method is studied and successfully design. The future work of these project is to design for fault detection technique.

REFERENCES

[1] P. Gujamagadi, P. Sankolli, P. Kumar V, Raghavendra B, Namita Palecha, Dr. Suma MS "Design of Vedic Multiplier for High Fault Coverage and Comparative Analysis with Conventional Multipliers" IEEE Conference Proceeding, 2015.

[2] Garima Rawat, Khyati Rathore., "Design and Analysis of ALU: Vedic Mathematics Approach", International Conference on Computing, Communication and Automation (ICCCA2015).

[3] S.P.Pohokar, R.S.Sisal "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics" IEEE Conference 2015.

[4] G.Ganesh Kumar, V.Charishma "Design of high speed vedic multiplier using vedic mathematics techniques" International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012 .

[5] Jagadguru Swami Sri Bharath, Krsna Tirathji, "Vedic Mathematics or Sixteen Simple Sutras From The Vedas", Motilal Banarsidas, Varanasi 1986.