2–4 And4–16 Mixed-Logic Line Decoders Using Adiabatic Circuit

Neha Kapse[1], Mayuri Chawla[2], Nakul Nagpal[3]
[1, 2, 3] Dept of VlSI
[1, 2, 3] Jhulelal Institute of Technology, Nagpur, India

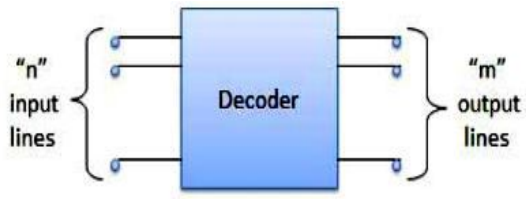
Abstract- *In day today world, as the technology is developing so rapidly the designing of the systems are becoming more and more compact. In some systems even if the circuits are not compact; still there is a need of less power consumption. In a microprocessor/ microcontroller based systems, the most commonly used block is the instruction set decoder. Hence; it will be not wrong if we say the instruction set decoder consumes more power. Thus optimizing the power of this block will be helpful to reduce the overall power consumption of the system. Thus proposed plan for this paper is the use of adiabatic technique to reduce power consumption of instruction decoder. In this paper, we have proposed the design of 2:4 decoder with the use of adiabatic logic to reduce the power of the decoder and thus will help in power reduction of overall system.*

Keywords- PTL, DPL, DVL

I. INTRODUCTION

Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. Decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. Applications of decoders are wide; they include data de-multiplexing, memory address decoding, seven segment display etc. A decoder is a simple circuit that converts a code into a set of signals. It is named as decoder because it changes the big coded data into different simple combinations which can be used to drive any signal, but we will begin our study of encoders and decoders because they are simpler to design. Active instructions occur only within a sub-set of all instructions.

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a particular code. The N inputs can be a 0 or a 1, there are 2N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH.



A common type of decoder is the line decoder which takes an n-digit binary number and decodes it into 2n data lines. The simplest is the 1-to-2 line decoder

II. LITERATURE REVIEW

Since last few decades the main challenges were Area, cost, and performance. But these days power is an important factor instead of cost, performance and area. The device which consumes very less power irrespective of speed such as heart pacemaker, RFID etc. works on the principle of adiabatic logic. The aim of reduction in power consumption is application specific. The authors have tried to decrease the power by combining the adiabatic and reversible technique [1]. The power consumed in traditional CMOS design can be given as,

$$P=CL.VDD^2. f$$

Here the power (P) is proportional to switching frequency (f), capacitance (CL), and square of supply voltage (VDD). Power consumption can be reduced by minimizing power supply, capacitance and switching frequency of operation. But as soon as these parameters reduce, it may deteriorate the performance of the circuit. Design using adiabatic principle helps in reducing power consumption at the

cost of reduced performance. A method based on adiabatic technique uses an ac power supply rather than dc for energy recovery. Theoretically adiabatic circuits consume zero power, it shows energy loss due to nonzero resistance in the switches. There are so many papers which describe different types of adiabatic technique such as ECRL, 2PASCL, PFAL etc. by which we can reduce power consumption of the circuit [2]. These techniques consume less power as compare to other CMOS circuits.

III. METHDOLOGY

A) DECODER

Proposed 2-to-4 decoder with enable input is constructed with AND gates, it becomes more economical to generate the decoder output. A 2-to-4 decoder is enable when E=1. The truth table of a 2-to-4 decoder is given in Table I and the general block diagram is shown in figure 2. The Boolean gate-based implementation of 2-to-4 decoder required four AND gates and two NOT logic gates

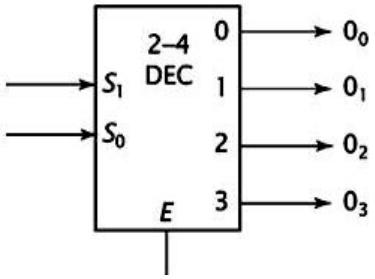


Fig1. General block diagram of 2-to-4 decoder

B) 2:4 LINE DECODER

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM) [7]–[9]. This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design.

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

TABLE I :TRUTH TABLE OF THE 2–4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

TABLE II : TRUTH TABLE OF THE INVERTING 2–4 DECODER

A 2–4 line decoder generates the 4 minterms *D*0−3 of 2 input variables *A* and *B*. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minterms *I*0−3, thus the selected output is set to 0 and the rest are set to

1, as shown in Table II. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gate Fig. 1(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 1(b), both yielding 20 transistors

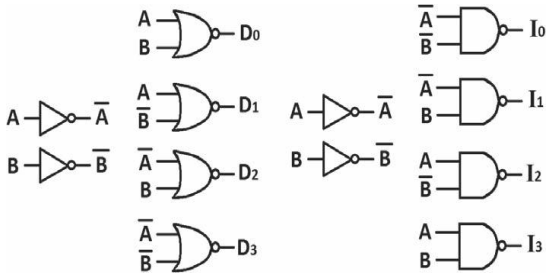


Fig 2. . 20-transistor 2–4 line decoders implemented with CMOS logic.

(a)Noninverting NOR-based decoder. (b) Inverting NAND-based decoder

C) Mixed Logic Line

Transmission gate logic (TGL) can efficiently implement AND/OR gates [5], thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and (b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL [3], and those that use both nMOS and pMOS pass transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and (d), respectively. They are full swinging but non-restoring, as well.

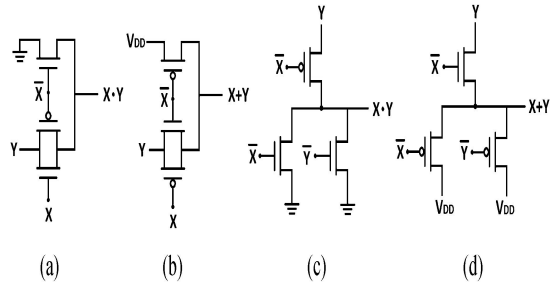


Fig 3. Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate.

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, i.e. the fact that they do not have balanced input loads. As shown in Fig. 3, we labelled the 2 gate inputs *X* and *Y*. In TGL gates, input *X* controls the gate terminals of all 3 transistors, while input *Y* propagates to the output node through the transmission gate. In DVL gates, input *X* controls 2 transistor gate terminals, while input *Y* controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to *X* and *Y* as the control signal and propagate signal of the gate, respectively.

Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (*A_B*) or implication (*A_ + B*) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (*A + B*) function, either choice is equally efficient. Finally, when implementing the NAND (*A_ + B_*) or NOR (*A_B_*) function, either choice result to a complementary propagate signal, perforce.

D) ADIABATIC CIRCUITS

The term "adiabatic" refers to the thermodynamic process that exchanges no energy with environment, and therefore there is no occurrence of power or energy dissipation. During the switching process, adiabatic technology reduces the power or energy dissipation and reuses some part of the energy by recycling it from the load capacitance.

Adiabatic circuits are basically low power circuits which use to conserve the energy by returning back its output energy to input, so that the same energy can be used for next operation.

Fig. 4 and Fig. 5 shows the Charging and Discharging in conventional CMOS circuit and Adiabatic System.

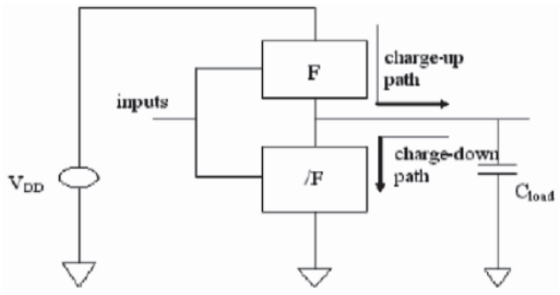


Fig 4. Charging and Discharging in Conventional system

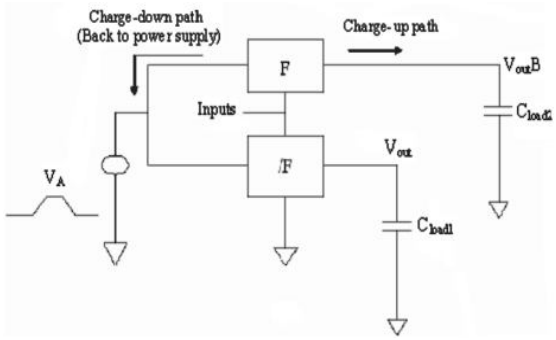


Fig 5. Charging and Discharging in Adiabatic system

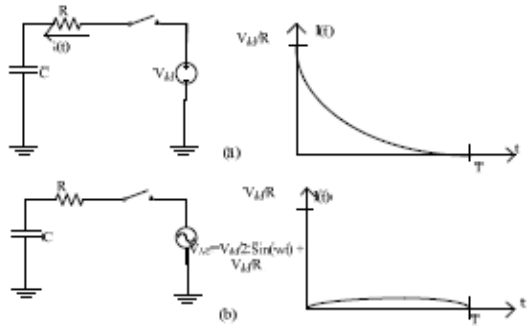


Fig. 6. (a) Switching of CMOS (b) Switching of Adiabatic Logic

Adiabatic circuits aims to conserve the charges by following essential rules

1) Avoiding turning on of transistor whenever there is a potential difference across the drain and source (VDS>0).
2) Avoiding turning off of Transistor whenever there is a flow of current through drain and source. (IDS~=0).
3) The current should not pass through diode.

Adiabatic Logic Types

During literature survey, we found different types of adiabatic circuits. They can be grouped into two fundamental kinds:

- Fully Adiabatic Circuit
- Partially energy recovery Adiabatic Circuit (Quasi)

Partially Adiabatic families include the following

- Efficient Charge Recovery Logic
- 2N-2N2P Adiabatic Logic
- Positive Feedback Adiabatic Logic
- NMOS Energy Recovery Logic
- Clocked Adiabatic Logic
- True Single-Phase Adiabatic Logic

IV. APPLICATION

- Decoders are greatly used in applications where the particular output or group of outputs to be activated only on the occurrence of a specific combination of input levels. Very often these input levels are provided by the outputs of a register or counter.
- When the counter or register continuously pulse the decoder inputs, the outputs will be activated sequentially. And these outputs can be used as sequencing signals or timing signals to switch the devices at particular times.
- Speed synchronization of multiple motors in industries
- War field flying robot with a night vision flying camera
- Robotic vehicle with the metal detector
- RF based home automation system
- Automatic health monitoring systems

V. CONCLUSION

The NEW design with respect to adiabatic technique reduce the power dissipation. Adiabatic design is an energy efficient way of design for low power circuits.

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