To Design Efficient 32-Bits Carry Select Adder By Using Brent Kung Adder

Priya S. Darne1, Prof. Y A. Sadawarte2
[1, 2] Dept of Electronics Engineering
[1, 2] Sevagram, Wardha –442102, INDIA

Abstract- *In this paper, delay and power efficient design for 32-bits carry select adder has been proposed. In digital technology, there is a large demand for high-speed technique. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic function. Carry Select Adder (CSLA) proposed architecture by using Brent Kung adder instant of Ripple Carry Select Adder .Ripple Carry Select Adder (RCS) gives complicated design and required long time for execution where Brent Kung Adder gives fast result, Carry select adder understand both the terms. And for fast execution, Carry select adder replaces RCA with Brent Kung and achieves to reduce delay and power of adder.*

Keywords- carry select adder, Brent Kung, power, delay.

I. INTRODUCTION

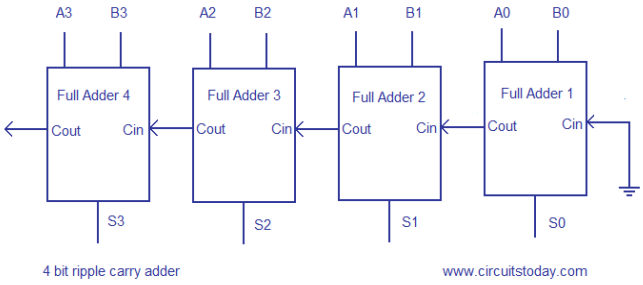
We are currently in the midst of a major period of transformation, the likes of which has never been seen before. Digital technology is permeating every aspect of our lives, industry and wider society, creating new and innovative forms of value and transformation the way we do almost everything. Adder is the important element of the arithmetic unit. Adder is considered one of the most essential units in digital circuits design. An example of the adder that is widely discussed is RCA, which is among the most straight forward implementation. RCA is a commonly used adder because it is simple to implement and an efficient adder in terms of area and power consumption. Although RCA has these advantages, it is very slow which then aspects the overall adder performance.

The high-speed and accuracy of a processor or system depends on the adder performance. To increase portability of system and battery life, delay and power are the ensuring the success of concern. Even in servers and personal computer, power efficient is a vital design parameter. In now days scenario, Design of power-efficient high-speed logic system in VLSI design techniques. In digital adders, the speed of addition is limited time required by the carry to generate thought the adder. In present scenario, where computations need to be perform using low power circuit that must operate at

high speed which is achievable with lesser delay that's why these paper describes comparative performance of 4-bit RCA and 4-bit BK design using TANNER EDA tool. Finally delay, power for the design adder presented and compare.

II. RIPPLE CARRY SELECT ADDER

A ripple carry adder is a login circuit in which the carryout of each full adder parameter is the carry in of the following next most significant full adder. It is called a ripple carry adder because each and every carry bit gets wind up into the next stage of adder.



Drawbacks of Ripple Carry Adder:

- In fig 1, the first sum bit should wait up unit carry is given; the second sum bit should wait up until previous carry is propagated and so on. Finally the output sum should wait up unit all previous carries are generated, so its result delays.
- In regular carry select adder there is a combination of multiplexer and double ripple carry adder due to which area increase and circuit becomes complicated. Ripple carry adder gives slow execution.

III. BRENT KUNG ADDER

In the type of structure of any adder greatly affects the speed of the circuit. The logarithm structure is considered to be one of the fastest structures and the Brent Kung

structure, use this logarithmic concept. Brent Kung is a low power adder and it is most effective technique which is used for implementing to reduced low power and low delay. For high performance and low power 32 bits carry select adder is implemented by using Brent Kung adder. Power and delay of all these adder architectures are calculated at different input voltages. Instead of using dual ripple carry adders, Brent Kung is used to design carry select adder. The results analysis shows that Modified 32-bits CSA is better than all the other adder architectures.

Advantages of Brent Kung adder

- Adder is portable and required less processing time. So Brent Kung adder is used for fast result.
- It is flexible, save power and low cost.
- There are three steps from where A to B signals is sending. As shown in fig 2: 4-bit Brent Kung adder.

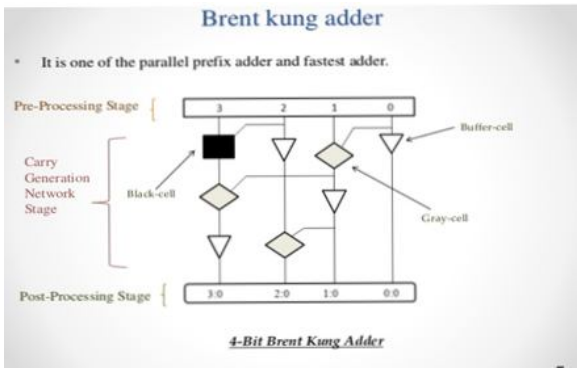


Fig 2: 4-bit Brent Kung adder

IV. LITERATURE REVIEW

Pallavi Saxena in paper entitled "Design of Low Power and High Speed Carry Select Adder Using Brent Kung Adder.

In this paper, Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA, Regular Square Root (SQRT) BK CSA and Modified SQRT BK CSA are designed. Power and delay of all these adder architectures are calculated at different input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of power but with small speed penalty.

L. Mugilvannan and S. Ramasamy "Low-Power and Area-Efficient Carry Select Adder Using Modified BEC-1 Converter"

Carry select adder is fastest adder used to perform arithmetic function. In this paper, carry select adder introduce the design of simple and efficient transistor. And this modification is design to save power and area in carry select adder but delay will be not control. There are two square root carry select adder is used one with modified BEC-1 converter and another with ordinary BEC-1 converter. And 16 bit square root carry select adder modified BEC-1 converter with is compare and developed with significant square root carry select adder ordinary BEC-1 converter.

When carry select adder design for large number of bit there is a possibility of large area but BEC-1 logic have ability to reduce area. Ripple carry adder gives low power and lead to increase in area, so carry select adder prefer to use Binary to Excess-1 Converter (BEC) instant of RCA. The basic idea of this work is to use transistor level modified Binary to Excess-1 Converter (BEC) instead of Ordinary BEC (gate level) with Cin = 1 in the CSLA to achieve lower area and power consumption. The main advantage of this transistor level modified BEC-1 comes from the lesser number of MOS transistor than the Ordinary BEC-1. For simple and efficient output in VLSI hardware implementation, carry select adder architecture is design with the modified Binary to Excess-1 Converter (BEC) instant of ordinary Binary to Excess-1 Converter (BEC) to achieve low power and area.

Basant Kumar Mohanty and Sujit Kumar Patel in paper entitled "Area–Delay– Power Efficient Carry Select Adder".

Mobile is a mini computer in VLSI hardware, which is modified and converted to smart mobile which is equally smart as computer. Now technologies become wireless and send data from one place to another place without data cables. In VLSI, system should be low power, high speed, less area. Some device like smart mobile device, wireless receivers and biomedical instrument need all these efficient parameter, which is provided by VLSI system. VLSI is a wireless system; where most of the wireless technology is been develop under VLSI system. In this paper, carry select adder study the data dependent parameter and also identify logic operation. The

logic operations which are present in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC) are analysed under carry select adder. We have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA. In the proposed scheme, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to Cin = 0 and 1) and fixed Cin bits are used for logic optimization of CS and generation units. An efficient CSLA design is obtained using optimized logic units.

V. RESULT

In regular carry select adder, there is a combination of multiplexer and double ripple carry adder due to which there is a increment of area. Carry select adder is one of the fastest adder and it understand both the terms, so by modifying carry select adder by replacing double ripple carry adder with Brent Kung adder. It designs a architecture which gives low power and high speed.

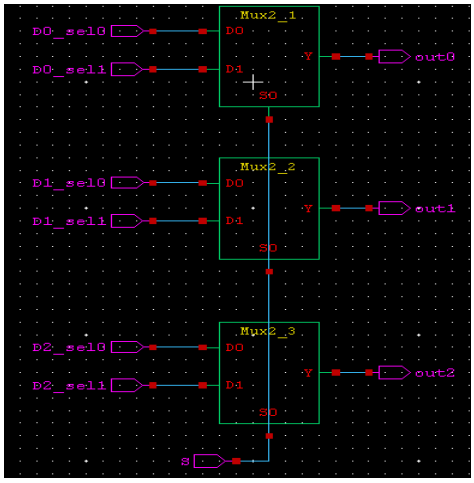


Fig: Multiplexer

Here there are basic diagram of multiplexer, 4-bits ripple carry adder and 4-bits Brent Kung adder, which are basic step of this architecture. By using this, I design 32 bits carry select adder with Brent Kung.

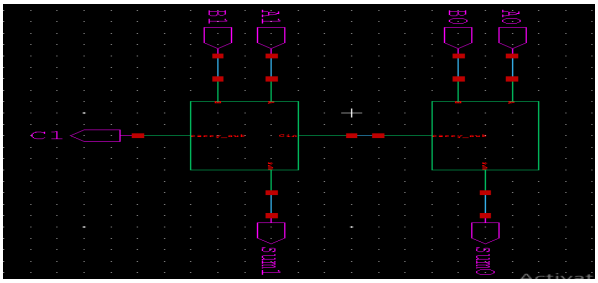


Fig: 4 bits Ripple carry adder

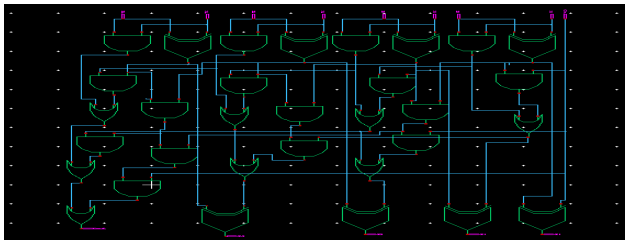


Fig: 4bits Brent Kung adder

VI. CONCLUSION

In this work, combination of multiplexer, Brent Kung adder, and ripple carry adder with 32 bit carry select adder form an advance design; which not only give high speed but also work on low power. Carry select adder proposed architecture with the help of Brent Kung adder which is consider being one of the fastest adder. The motive of this work is to give fastest technology to this transforming world. With changing world, techniques also need to be more advance and fast. These can be more modified by increasing number of N bits.

VII. ACKNOWLEDGEMENT

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