Minimization of Thd Using Unified Power Quality Conditioner for Medical Applications

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Abstract- *The Unified Power Quality Conditioner (UPQC) is used to mitigate power quality disturbances that arises in power distribution system. It compensates voltage or current harmonics and other disturbances that may arise due to nonlinear load and provides reliable power to the load. The UPQC is a combination of both series and shunt filter connected back to back by a DC link. The fundamental component appears as DC and is filtered out using low pass filter and the harmonics which appears as an alternating waveform is then converted to 3 phase line harmonics are cancelled. This is done by the harmonics suppression block in series filter.*

The other part of the series control block provides constant voltage supply during voltage sag or swell. The output reference voltage waveform Vref is then fed to back to obtain gate signal for series filter.

Keywords- power quality; UPQC.

I. INTRODUCTION

The power quality becomes a very important issue due to rapid growth in use of nonlinear loads. The recent advancements in power electronic equipment attract the users due to saving of electricity bills, user friendly, good performance and safety. The power quality is simply a sinusoidal voltage and currents waveforms exactly in phase with constant frequency. If there are any deficiencies in voltage or current waveform then there exists a problem on power quality. The various power quality problems are voltage sag, swell, harmonics, transients, interruptions, notches etc. voltage sag and harmonics are dominant and severe impact on the power system. The loss of production due to voltage sag is very high in the recent years. The harmonics are severe impact on sensitive equipment, motors, transformers, cables etc. the source need to supply harmonic component in addition with fundamental component, this makes the production cost high. The source voltage gets distorted due to nonlinear load connected at the point of common coupling which can affect the other linear loads connected to the source because the linear load draws nonlinear current due to non-uniform voltage.

There are many solutions available to improve power quality like DVR, D-STATCOM, series APF, Shunt APF, UPQC etc. Here UPQC is a series and shunt active power filters (APF) devices through common dc link which can solve both voltage and current related problems. The design and modelling of UPQC is explained in later sections. MATLAB/SIMULINK software is used to design and analyse the performance of UPQC with PI controller.

Here , We arrange our study as follows: Section II covers the UPQC configuration. In Section III, UPQC control blocks are discussed in brief and Section IV describes the UPQC implementation. Section V , the results of our simulated model is presented.

II. DESIGN OF UPQC

A conventional UPQC topology consists of integration of two active power filters are connected back to back to common dc link bus .A simple block diagram of a typical UPQC is shown in Fig. 1.

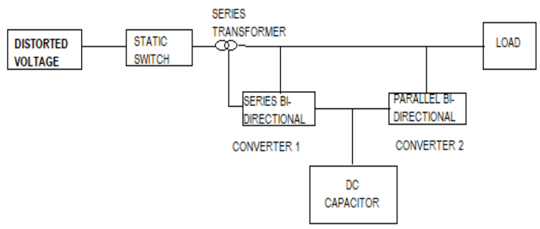

Fig 1 UPQC Design

It can be configured either with voltage-source converters or current source converters in single phase, three-phase three wire, or 3P4W configurations. The UPQC with the voltage-source converter (VSC) is most common because of its smaller size and low cost. Despite these previously mentioned advantages, the VSI topology has slow control of the converter (LC filter) output voltage and no short-circuit/overcurrent protection.

When the active rectifier inside the UPQC is used as a power factor corrector, dc bus voltage oscillations appear which makes the control of the series filter output voltage more difficult. The CSI-based UPQC has advantages of excellent current control capability, easy protection, and high reliability over VSI-based UPQC . The main drawback of the CSI-based UPQC has been so far the lack of proper switching devices and large dc-side filter.

A configuration of UPQC using two current-source converters connected back to back through a large dc-link reactor is shown in Fig. 2.

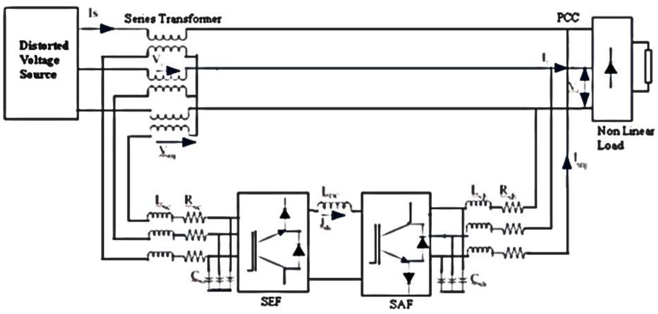

Fig.2.UPQC topology using current-source converter

The performance of the UPQC mainly depends on how accurately and quickly the reference signals are derived.

After efficient extraction of the distorted signal, a suitable dc-link current regulator is used to derive the actual reference signals.

A dc current regulator will serve as power-loss compensation in the filter circuits, which will take place through the activation of a shunt unit. This regulator will maintain dc-link current constant for stable operation of the filter.

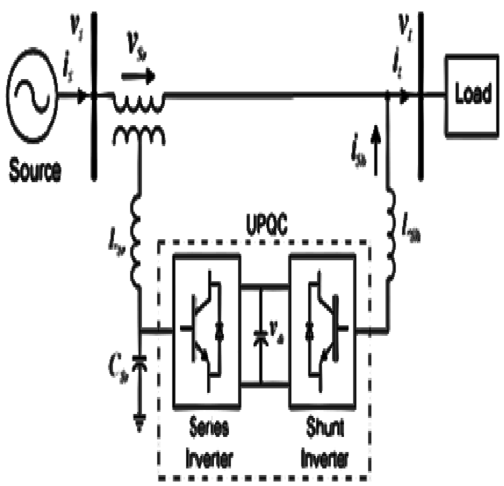

Fig 3. UPQC topology with voltage source inverters.

In the conventional PI controller, the error between the actual dc-link current and a reference value, which is generally slightly greater than the peak of the dc-link value, is fed to the PI controller. The output of the PI controller is added suitably for the generation of a reference template.

III. CONTROL BLOCKS OF UPQC

UPQC is a combination of series and shunt compensating devices connected through a capacitor which is used for energy storing device. The value of capacitance is based on the peak voltage ripple and rated filter current. The design and operation series and shunt APF are discussed. The regulation of voltage source can be done by series APF but some of the current harmonics are missing and this can affect the source voltage this can be avoided by shunt APF. The basic circuit of UPQC is shown.

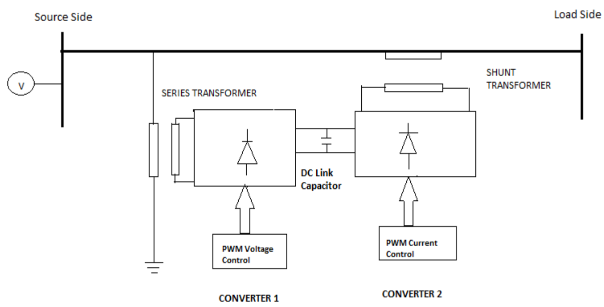

Fig 4 Structure of UPQC.

Series APF is a series element which can act as a controlled voltage source. It injects voltage of negative harmonics through injection transformer. The basic circuit circuit of series APF is shown. The capacitor is energy storage with self-supporting i.e. with reactive power exchange. If we use a fixed dc source then there exists only a real power exchange through voltage source inverter. The design of controller for generating pulses explained.

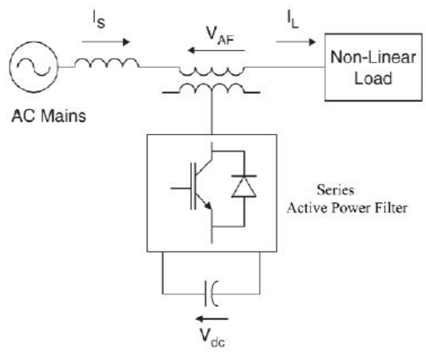

Fig.5 Series APF

Shunt active power filter is a shunt connecting device which can be acts as controlled current source. It injects negative current harmonics to solve current related problems. The purpose of capacitor is same as series APF. The basic circuit of shunt APF and its basic function is explained in fig 2.3. The controller for generating pulses is explained in section 2.3. The functions of shunt APF are dc link voltage regulation, improvement of power factor by controlling reactive power.

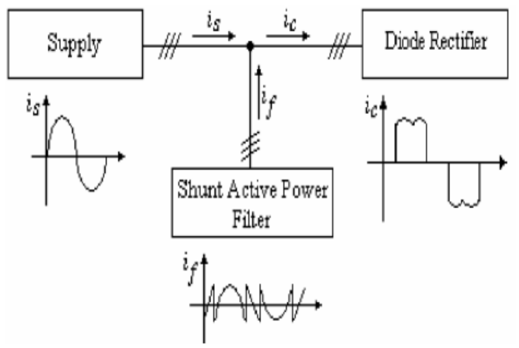

Fig 6 Shunt APF

CIRCUIT DIAGRAM

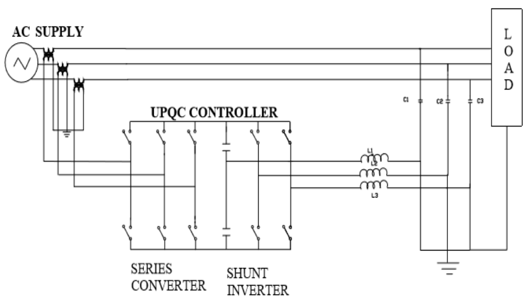

Fig 7 Circuit Diagram

IV. SIMULATION OF UPQC

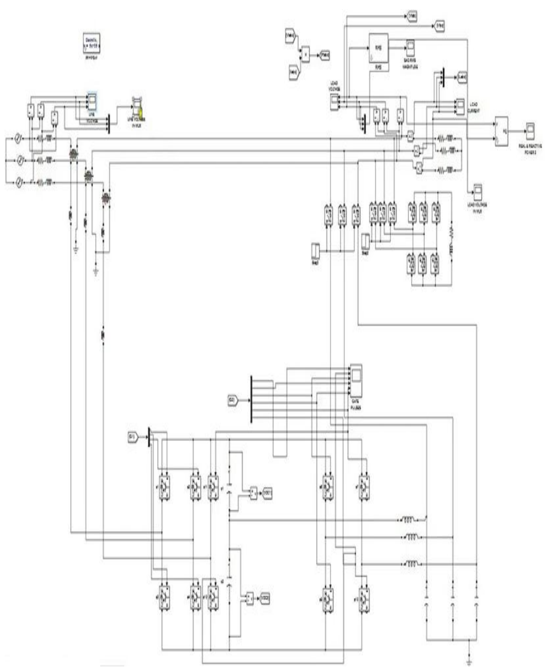

Fig.7 Simulation of UPQC

The input 3 phase voltage connected to the series and shunt converters , input side measures the line voltage and line voltage in MUX. The output shows the voltage sag and swell magnitude along with the load voltage**.**

SIMULATION RESULTS

Fig.8 Line Voltage

Figure 3.2 shows the simulated output of the line voltage .The line voltage shows input voltages in the each phases. Thus the figure shows input of 300V on every phases.

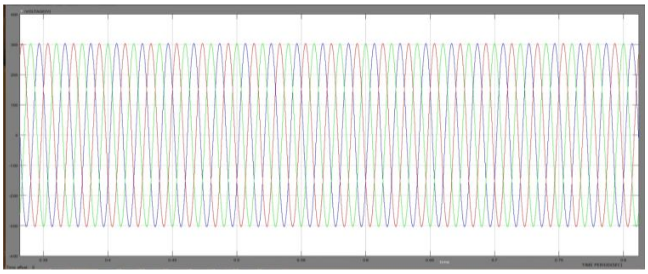

Fig.9 Line voltage in mux

Figure 3.3 shows the simulated output of the line voltage in multiplexer. The MUX is the multiplexer which shows all the 3phase voltages in the single MUX.

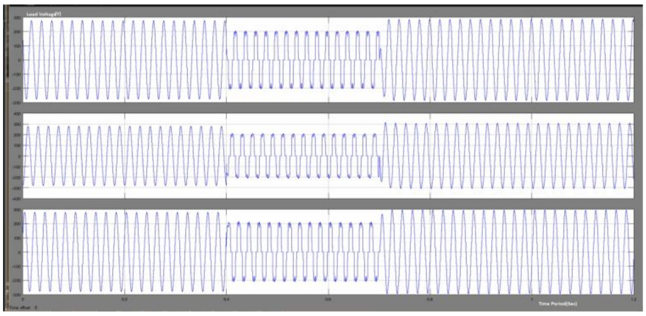

Fig.10 Load Voltage

Figure 3.4 shows the simulated output of the load voltage.Here the load voltage shown at the output side for the step 0.4 to 0.7. It shows that the harmonics are introduced at the point of 0.4 and is rectified at the point of 0.7 using UPQC.

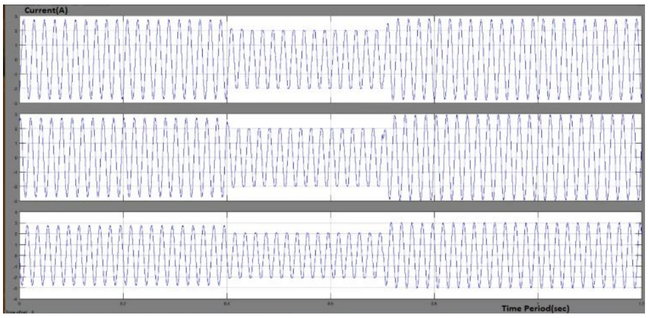

Fig.11 Load Current

Figure 3.5 shows the load current shown the output side for the step 0.4 to 0.7. It shows that the harmonics are introduced at the point of 0.4 and is rectified at the point of 0.7 using UPQC.

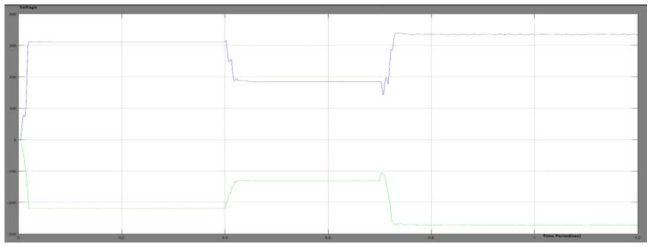

Fig.12 Real and Reactive Power

Figure 12 shows the simulated output of the real and reactive power. The sag and the swell of voltages that the drop in voltage and rise in voltage when the disturbance is produced by the power electronic load.

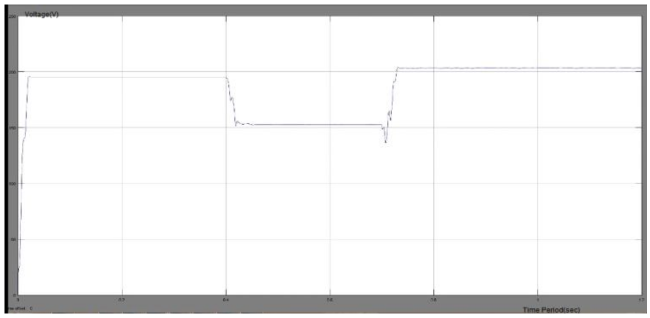

Fig.13 Sag RMS Magnitude

Figure 13 shows the simulated output of the Sag RMS Magnitude. It shows the sag that the drop in voltage when the disturbance is produced by the power electronic load.

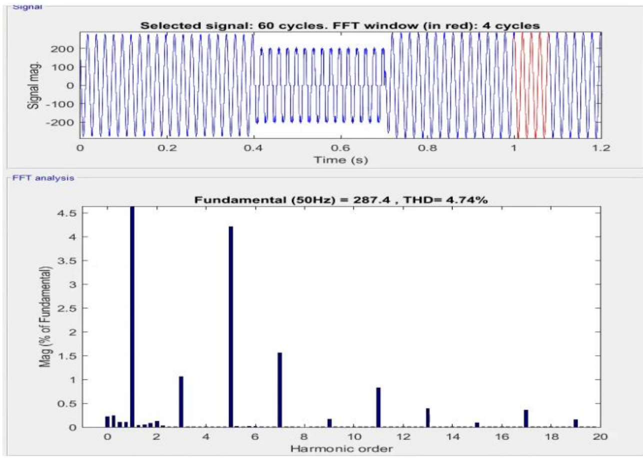

Fig.14 THD Reduction

Figure 14 shows the simulated output of the THD Reduction. Here the harmonic reduction upto 4.74% have been shown for the four cycles.The harmonic reduction in each of the phases can be done using FFT analysis.

IV. HARDWARE IMPLEMENTATION

The Figure 15 shows the hardware circuit diagram of UPQC model. It explains that the UPQC cicuit connected to the microcontroller circuit along with driver circuit inorder convert the microamps into milliamps, since the UPQC built for milliamps.

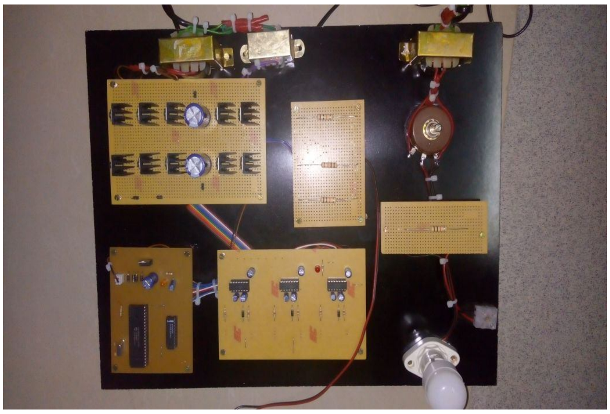

Fig 12 Hardware of UPQC arrangement

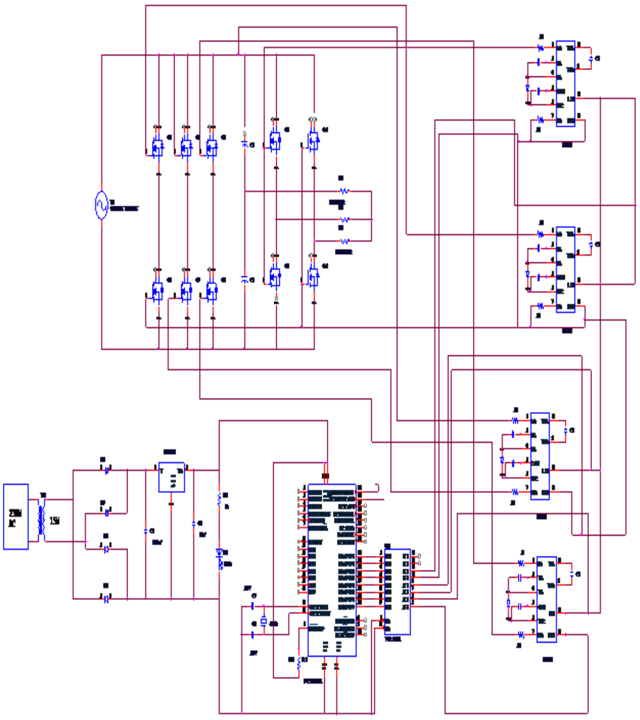

Figure 13 Hardware Circuit Diagram

The Figure 13 shows the hardware circuit diagram of UPQC model. It explains that the UPQC circuit connected to the microcontroller circuit along with driver circuit in order convert the microamps into milliamps, since the UPQC built for milliamps.

The input 3 phase voltage connected to the series and shunt converters , input side measures the line voltage and line voltage in MUX. The voltage and current are sensed by the series and shunt converters which is called as UPQC, The filtered current and voltage are sent to the output side.

The output shows the voltage sag and swell magnitude along with the load voltage. It is also shown that the power electronic device connected between the load and the UPQC , here the step noise are given to show the harmonic produced in the load and the rectification done by the UPQC block for the harmonic reduction.

VI. RESULT

The figure shows the hardware implementation of UPQC for THD reduction. From the simulation output it is clear that the harmonics are are highly reduced upto 4.74% by replacing a leg by 2 capacitors.

VII. CONCLUSION AND FUTURE SCOPE

Thus the Total Harmonic Distortion level is highly reduced to some extent level nearly 3.96% . To validate this method simulated UPQC model is developed in the MATLAB software. It is seen that the changes in the voltage sag and the voltage swell has been shown in the simulated diagram. The PI controller enhances the dynamic control of the UPQC. It is observed that in future, all the variables like THD of load voltage and source current will be considered for various optimization techniques.

VIII. FUTURE ENHANCEMENT

UPQC can mitigate voltage sag. No additional energy storage device required for sag compensation, long duration sags and under voltages can also be compensated. Dynamic response will be fast.

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Also, it isolates the load current harmonics from flowing to the utility. Hybrid (combined Analog and Digital) control can be implemented, the control scheme is applicable for both single and three phase.

- UPQC for three phase four wire system can be preferred for future purpose by Hybrid control.
- Voltage Swell Compensation can be done inorder to improve the load voltage and also power factor can be improved.
- In this research, the basic inverter has been considered which has a switching frequency, voltage rating and power capacity limited by the rating of power switches. Combining many swiches can address one or more of the inverter limitations. Thus , the UPQC configuration employing multi-step and multi-level inveter topologies must be investigated.
- Performance comparison of available power quality detection and reference signal generation methods experimentally with the realization of minimum power dissipation methods for DVR and APF.

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