Design Of Three Level Single Phase Diode-Clamped Inverter

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Abstract- *Multilevel inverter has a capability to handled high power, high voltage with less total harmonic distortion (THD), reduced switching losses and good power quality. In recent years, they become more popular in high power high voltage application, with increase in the voltage levels harmonic content in the output voltage waveform will decrease. This paper deals with the "Design of three level single phase inverter" which uses diode clamped method of multilevel inverter as a control strategy. This method is one of the well known, most advantageous, much simpler and basic method of multilevel inverter. The efficiency of diode clamped method is more than the cascade H-bridge and flying capacitor type methods.*

Keywords- Multilevel inverter, Voltage control, Diode clamped method.

I. INTRODUCTION

The concept of multilevel inverter has been introduced by NABLE ELAL in 1975. At present multilevel inverters has drawn a great attention in industry, due to its high power and high voltage applications. Multilevel inverter starts with the three voltage levels. In case of the two level inverter we get two voltage levels i.e. if we are giving V_{dc} as an input voltage then it gives $+V_{dc}/2$ and $-V_{dc}/2$ as output voltage levels. Although this method of inverter gives ac voltage but it has few drawbacks as it creates harmonic distortion, high switching frequency and also have high dv/dt as compared to the multilevel inverters. Normally this method works but it creates problems particularly those where low distortion in the output voltage is required.

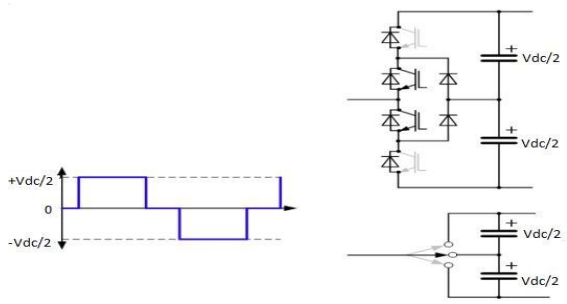

Fig.1 Three level inverter

The concept of three level inverter is the modification of two level inverter. In multilevel inverters instead of two voltage levels more than two voltage levels are combined together. In fig.1 shows the circuit diagram and output voltage waveform of three level inverter, we get three voltage levels and they are $+V_{dc}$, 0, $-V_{dc}$ respectively. The output voltage of multilevel inverter produces a staircase waveform, in other words multiple step voltage waveform which looks like a sinusoidal waveform. Smoothness of the waveform is proportional to the voltage levels, as we increase the voltage levels the waveform becomes more and more smoother. Multilevel inverter has drawback that by increasing the number of voltage levels, higher number of semiconductor switches required with separate gate driver circuit. Due to this it increases the size and complexity of the circuits.Fig.2 shows the hardware design blocks of the multilevel inverter design such as DC supply or battery, microcontroller, switching circuit, step up transformer, load etc.

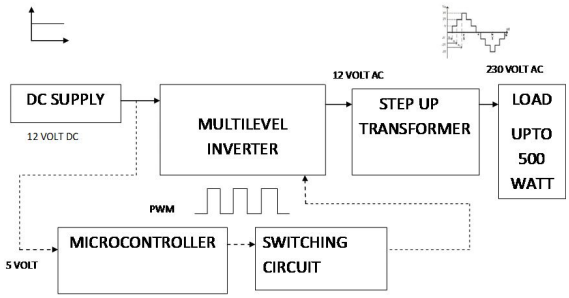

Fig.2 Block diagram of multilevel inverter design

II. TYPES OF THREE LEVEL INVERTER

Three level inverter topologies are :

1. Diode clamped multilevel inverter
2. Flying capacitor multilevel inverter
3. Cascade H-bridge type multilevel inverter

1. Diode clamped multilevel inverter

Diode clamped multilevel inverter has DC source, the series capacitors are used in this inverter is for to divide the DC bus voltage into a set of voltage levels.(n-1) number of capacitors are used to produce n levels of voltage.

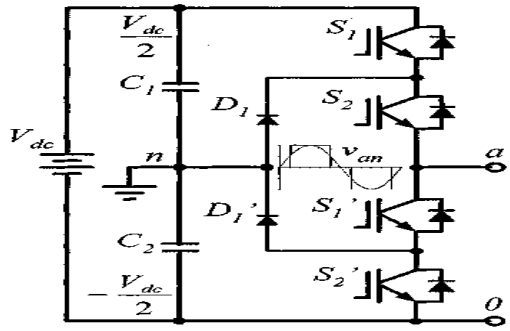

Fig.3 shows the circuit diagram of three level diode clamped inverter.

2. Flying capacitor multilevel inverter

Capacitors with ladder arrangement are used in this type of topology. The voltage on each capacitor is differing from that of the next capacitor. To generate n level inverter (n-1) capacitors are used.

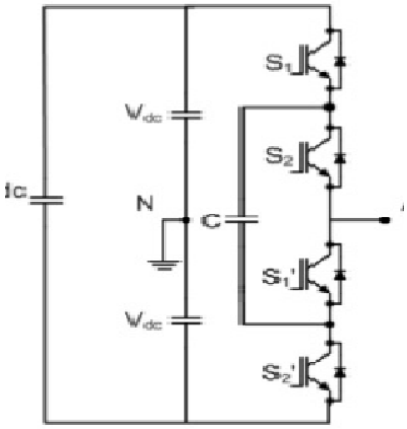

Fig.4 shows the Flying capacitor type 3 level inverter.

3. Cascade H-bridge multilevel inverter

This type of multilevel inverter has separately DC source. The main advantage of this inverter is that it avoided the extra clamping diodes or voltage balancing capacitors.

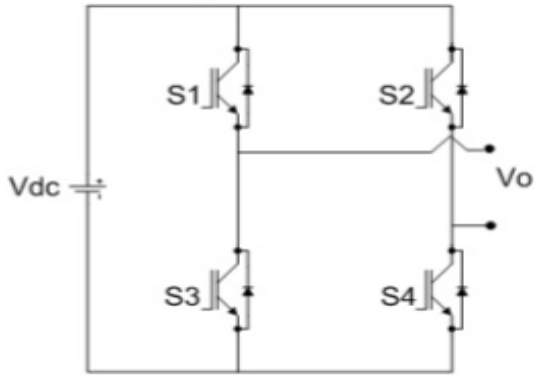

Fig.5 shows the circuit diagram of cascade H-bridge 3 level inverter.

III. DIODE CLAMPED INVERTER

In diode clamped circuit, the DC voltage is split in three levels by two series connected bulk capacitors, C_1 and C_2.The middle point of two capacitors n can be defined as neutral point. The output voltage V_{an} has three stages $+V_{dc}/2$, 0, $-V_{dc}/2$. For voltage $+V_{dc}/2$, switches S_1 and S_2 need to be turn on; for voltage level $-V_{dc}/2$ switches S_1' and S_2' need to be turn on; and for the 0 level, S_2 and S_1' need to be turn on. There are two diodes D_1 and D_1'are used for to clamp the switch voltage to half the level of DC bus voltage. When switches S1 and S2 turn on, the voltage across a and o is V_{dc} i.e., $V_{ao}=V_{dc}$. It is DC voltage. In this D_1' balances out voltage sharing between S_1' and S_2'.S_1' blocking voltage across C_1 and S_2' blocking voltage across C_2. The voltage across capacitor C_2 is the difference of V_{an} and V_{ao}, where V_{an} is ac voltage while V_{ao} is DC voltage. And the voltage across C2 is $V_{dc}/2$. If output voltage is removed out between a and o, then the circuit becomes a dc/dc converter, which has three outputs i.e. V_{dc}, $V_{dc}/2$, 0.

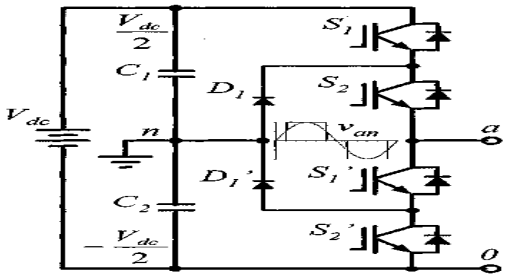

Fig.6 Three level diode clamped inverter

Output voltage	S_1	S_2	S_1'	S_2'
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Table Switching table of Three level inverter

Above figure shows the switching operation in which when switch S_1 and S_2 are operating then the output $V_{dc}/2$ is occurred while when switch S_1' and S_2' operated then $-V_{dc}/2$ occurred at output. When S_2 and S_1' operated then zero output is occurred.

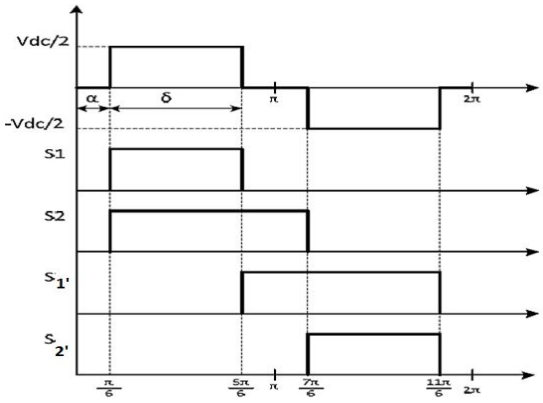

Fig.7 Output waveform of three level inverter

Above fig. shows the output waveforms of three level inverter. Where α is the firing angle at which the pulse get fired. While δ is the delay. The individual waveforms of switches are shown above.

Comparison of different multilevel inverter topologies :

Sr.no.	Topology	Diode clamped	Flying capacitor	Cascade H-bridge
1	Power semi conductor switches	2(n-1)	2(n-1)	2(n-1)
2	Clamping diode per phase	(n-1)(n-2)	0	0
3	DC bus capacitor	(n-1)	(n-1)	(n-1)/2
4	Balancing capacitor per phase	0	(n-2)(n-2)/2	0
5	Voltage unbalancing	Average	High	Very small
6	Applications	Motor drive system ,STATCOM	Motor drive system, STATCOM	Motor drive system, PV fuel cell, Battery system

IV. ADVANTAGES

The advantages for the diode-clamped inverter are,

(1) A large number of levels 'n' yields a small harmonic distortion.
(2) All of the phases share a common dc bus.
(3) Reactive power flow can be controlled.
(4) High efficiency for fundamental switching frequency.
(5) Relatively simple control methods.

V. DISADVANTAGES

The disadvantages are,

(1) Different voltage ratings for clamping diodes are required.
(2) Real power flow is difficult because of the capacitors imbalance.
(3) Need high voltage rating diodes to block the reverse voltages.
(4) The number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels. Extra clamping diodes required are 12nn per phase.

VI. APPLICATIONS

(1) An interface between High voltage DC transmission line and AC transmission line.
(2) High power medium voltage variable speed drives.
(3) Static VAR compensation.

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