CMOS ASIC Design And Implementation of Phase Locked Loop Using Cadence EDA Tool

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Abstract- *Phase Locked Loop is the heart of the many modern electronics as well communication system. Hence there is necessity of a PLL which must operate in the GHz frequency range. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. This project deals with the performance analysis of Phase Frequency Detector approaches with Charge Pump. The Phase Frequency Detector (PFD) is an important building block of phase locked loop (PLL). The phase frequency detector, charge pump and loop filter are designed and simulated using Cadence tool in GPDK 180nm technology. Virtuoso Analog Design Environment tool of Cadence have used to design and simulate schematic.*

Keywords- Charge pump, Loop filter, Phase frequency detector, Voltage control oscillator.

I. INTRODUCTION

The concept of Phase Locked Loop (PLL) first emerged in the early 1930's. But the technology was not developed as it now, the cost factor for developing this technology was very high. Since the advancement in the field of integrated circuits, PLL has become one of the main building blocks in the electronics technology. A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency of an input signal. In addition to stabilizing a particular communications channel (keeping it set to a particular frequency), a PLL can be used to generate a signal, modulate or demodulate a signal, reconstitute a signal with less noise, or multiply or divide a frequency. PLLs are frequently used in wireless communication, particularly where signals are carried using frequency modulation (FM) or phase modulation (PM). PLLs can also be used in amplitude modulation (AM). PLLs are more commonly used for digital data transmission, but can also be designed for analog information. Phase-locked loop devices are more commonly manufactured as integrated circuits (ICs) although discrete circuits are used for microwave.

II. SYSTEM DESCRIPTION

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock and data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL.A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

III. SOFTWARE REQUIREMENT

3.1 SOFTWARE USED

The proposed PLL is designed and simulated using Cadence EDA suite-180nm technology.

3.2 CADENCE EDA SUITE

Cadence Design Systems Inc. is an American electronic design automation (EDA) software and engineering services company, founded in 1988 by the merger of SDA Systems and ECAD, Inc. The company produces software for designing integrated circuits also known as chips, Systems On Chip (or SoCs) and printed circuit boards.

Cadence's product offerings are targeted at various types of design and verification tasks which include:

1. Virtuoso Platform-Cadence Virtuoso Design Environment- For schematic entry.
   - Tools for designing full-custom integrated circuits; includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, custom layout, physical verification, extraction and back-annotation. Used mainly for analog, mixed-signal, RF and standard-cell designs, but also memory and FPGA designs.

2. Encounter Platform– Cadence Encounter- For physical design of digital and mixed signal circuits.
   - Tools for creation of digital integrated circuits. This includes floor planning, synthesis, test, and place and route. Typically a digital design starts from Verilog net lists.

3. Incisive Platform – Cadence IES - For digital and mixed signal verification.

4. Tools for simulation and functional verification of RTL including Verilog, VHDL and System C based models. Includes formal verification, formal equivalence checking, hardware acceleration, and emulation.

5. Verification - Cadence Assura - DRC, LVS & Parasitic extraction of analog mixed signal designs.

Cadence Spectre - Simulation, analysis & parameter estimation of schematic and physical designs.

- Design IP: Cadence provides design IP targeting areas including memory(DRAM), covering DDR1, DDR2, DDR3, DDR4, LPDDR2, LPDDR3,LPDDR4, and Wide I/O; storage (non-volatile memory), covering NVME express and NAND Flash controller and PHY; and high-performance interface protocols such as PCI Express Gen3, 40/100G Ethernet, USB 2 and USB 3.
- Verification IP (VIP) Cadence provides the broadest set of Commercial VIP available with over 30 protocols in its VIP Portfolio. They include AMBA, PCI Express, USB, SATA, OCP, SAS, MIPI and many others. Cadence VIP also provides the unique Compliance Management System (CMS) to automate protocol compliance verification.

6. Allegro Platform – Cadence Allegro - PCB design solution.
   - Tools for co-design of integrated circuits, packages, and PCBs.
   - OR CAD/PSpice - Tools for smaller design teams and individual PCB designers.

3.3 180nm TECHNOLOGY

The 180 nanometer (180 nm) process refers to the level of semiconductor process technology that was reached in the 1999-2000 timeframe by most leading semiconductor companies, like Intel, Texas Instruments, IBM, and TSMC. The origin of the 180 nm value is historical, as it reflects a trend of 70% scaling every 2–3 years. This was the first technology using a gate length shorter than that of light used for lithography (which has a minimum of 193 nm).Some more recent microprocessors and microcontrollers (e.g. PIC) are using this technology because it is typically low cost and does not require upgrading of existing components. Processors using 180nm manufacturing technology are as follows.

- Intel Coppermine E
- AMD Athlon Thunderbird
- Intel Celeron (Willamette)
- Motorola PowerPC 7445 and 7455 (Apollo 6)

IV. PHASE FREQUENCY DETECTOR

In a PLL, unlike many other feedback systems, the variable of interest changes dimension around the loop: it is converted from phase to voltage (or current) by the phase detector, processed by the LPF as such, and converted back to phase by the VCO. In the lock condition, the input and output frequencies are exactly equal, regardless of the magnitude of the loop gain (although the phase error may not be zero). This is an extremely important property because many applications are intolerant or even small (systematic) differences between the input and output frequencies. The PD compares the phase of the output signal with the phase of the reference signal and develops an output signal that is approximately proportional to the phase-error Φe. The output voltage of the PD is proportional to the phase-difference between the reference signal and the output signal. In locked condition, all the signals in the loop have reached steady state and whose output DC value is proportional to $\Delta\varphi$.

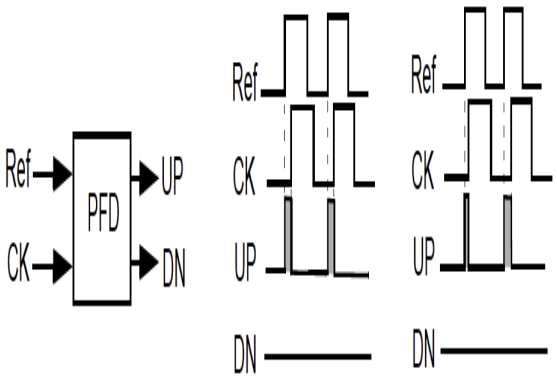

Figure 1 Schematic of charge pump

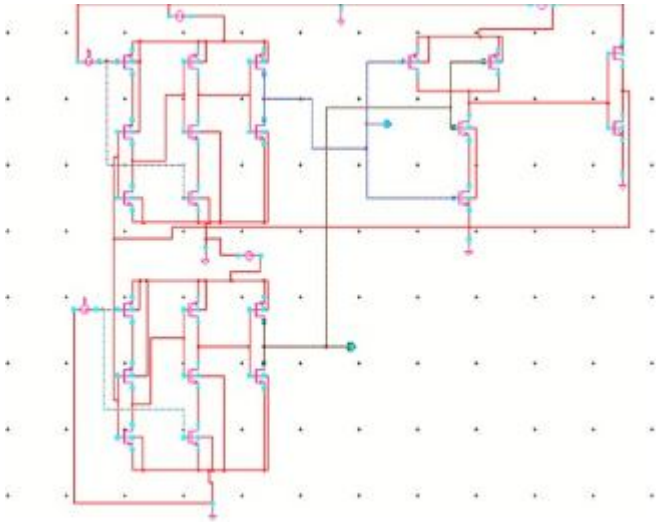

Figure 2 Schematic of phase frequency detector

V. CHARGE PUMP

Charge pump is the next block to the phase frequency detector. A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. The output of the PFD should be combined into a single output to drive the loop filter. The charge pump with the help of leakage current, delay offset and the mismatch in the PFD are analyzed in a quantitative manner. The basic charge pumps usually have UP and DOWN switches. These switches are made up of PMOS and NMOS. When charge is dumped into the loop filter, the gain boosting charge pump helps in mismatching of the current which generally occurs due to the difference between sources and drain voltages of the PMOS and NMOS. However it requires more transistors as compared with the conventional charge pump. Due to the current mismatch which is one of the common problems in conventional charge pump, the phase noise of overall PLL is dominated. A high performance charge pump circuit is used for eliminating this problem of current mismatch. The charge pump helps in minimizing the mismatch enclosed by the charging and discharging currents.

TABLE I TRUTH TABLE OF CHARGE PUMP

UP SIGNAL	DOWN SIGNAL	MODE OF OPERATION
1	0	Charging
0	1	Discharging
0	0	Vout constant
1	1	Vout constant

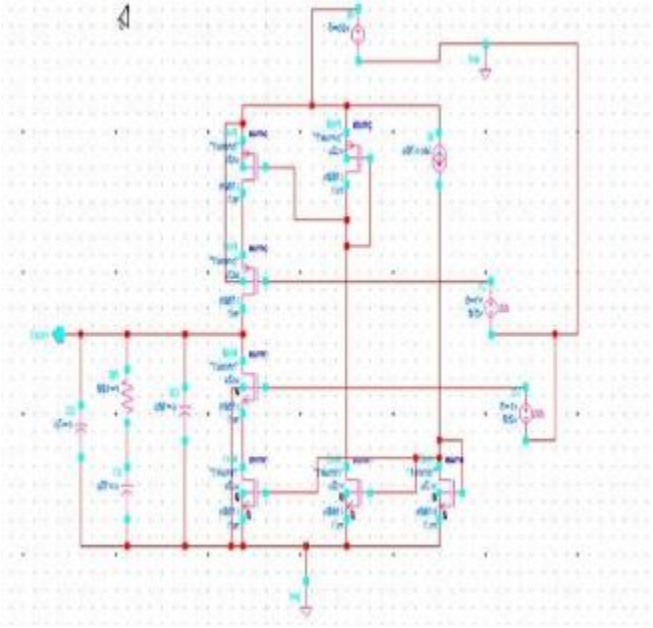

Figure 3 Schematic of charge pump

VI. LOOP FILTER

It is importunate to symbolize that the output converted from phase frequency detector and charge pump is comprised of high dc frequency components with a considerable amount of ac components. Hence loop filter has been introduced for filtering those ac components. The loop filter is a passive type low pass filter. For maintaining the stability loop filter is used as a vital component. Ideally the low pass filter helps in maintaining a constant voltage which is provided to the input of VCO.A low pass filter is a filter that passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frquencies higher than the cutoff frequency. The exact frequency response of the filter depends on the filter design.

Filters are frequently added after the charge pump to reduce the ripple. The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. Here the RC low-pass filter is used. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO. A high speed low power consumption positive edge triggered Delayed (D) flip flop was designed for increasing the speed of counter in Phase locked loop, using 180 nm CMOS technology.A simple passive RC Low Pass Filter or LPF, can be easily made by connecting together in series a single Resistor with a single Capacitor as shown below. In this type of filter arrangement the input signal (Vin) is applied to the series combination (both the Resistor and Capacitor together) but the output signal (Vout) is taken across the capacitor only. The reactance of a capacitor varies inversely with frequency, while the value of the resistor remains constant as the frequency changes. At low frequencies the capacitive reactance, (Xc<) of the capacitor will be very large compared to the resistive value of the resistor, R. This means that the voltage potential, Vc across the capacitor will be much larger than the voltage drop, Vr developed across the resistor. At high frequencies the reverse is true with Vc being small and Vr being large due to the change in the capacitive reactance value.

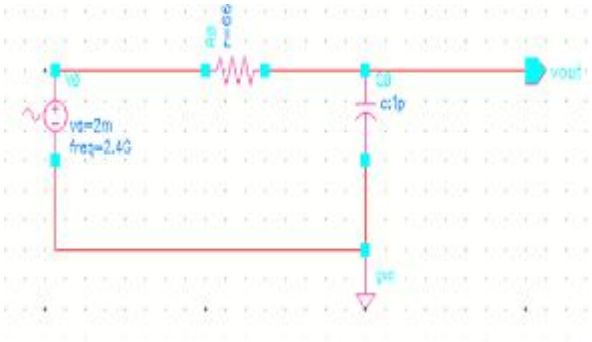

Figure 4 Schematic of low pass filter

VII. RESULTS AND WAVEFORMS

The blocks of PLL is implemented using Cadence Virtuoso and simulated. Simulation results of the Phase Frequency Detector, Charge pump, Loop Filter circuit are given below.

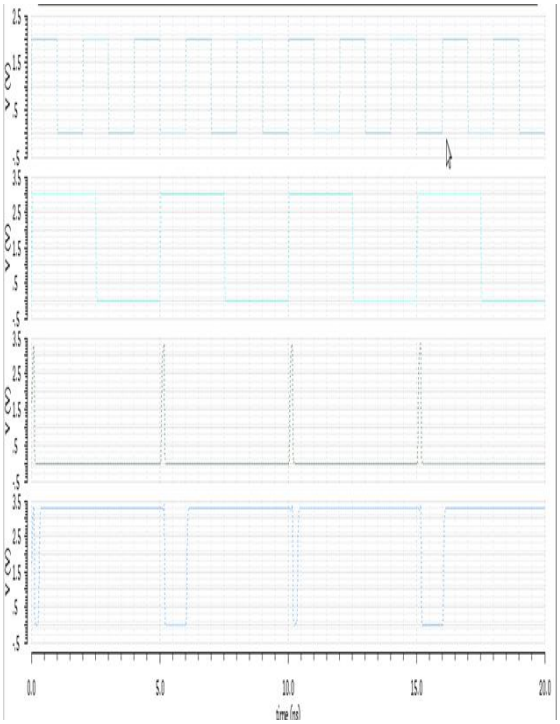

Figure 5 Output waveform of phase frequency detector

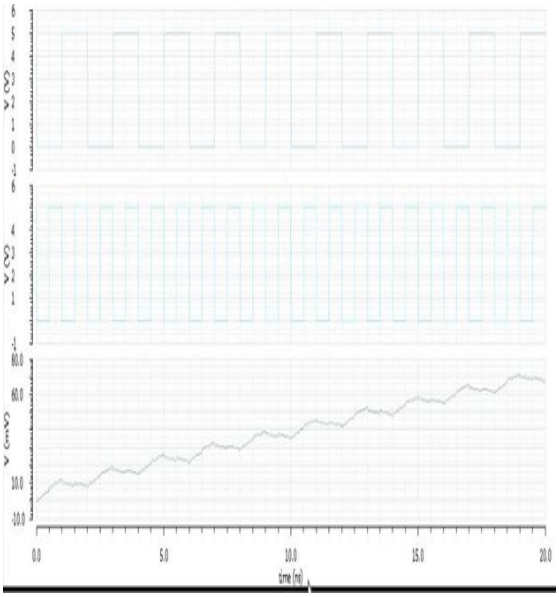

Figure 6 Output waveform of charge pump

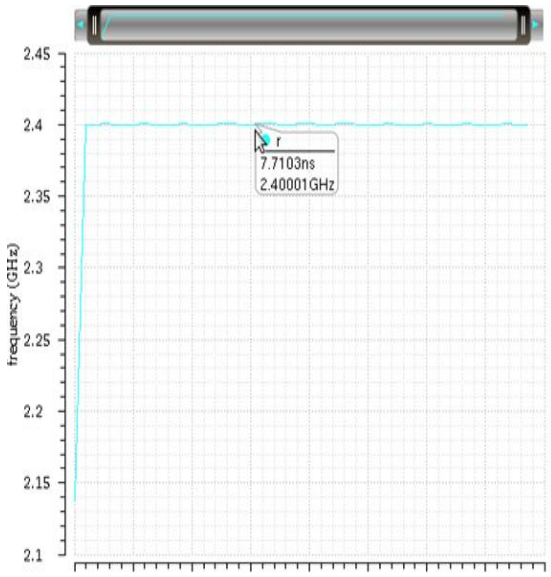

Figure 7 Output waveform of low pass filter

VIII. CONCLUSION

Minimization of power consumption is essential for high performance VLSI systems. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved. The power consumption of PFD is 4.5µW, Charge pump is 5.05mW and loop filter is 3.1µW.

REFERENCES

[1] B.P.Panda, P.K.Rout, D.P.Acharya, and G.Panda, (2011), "Analysis and Design of 1GHz PLL for Fast Phase and Frequency Acquisition"Proc. of *International Conference on Electronic System,* India, pp 212-215.

[2] Darji Urvi M.,(2012) "Design, Analysis and implementation of DPLL using 0.18µm CMOS Technology", Gujarat Technological University.

[3] George Tom Varghese, (2007-2009), "Phase Locked Loop Design as a Frequency Multiplier", Thesis Department of Electronics and Communication Engineering, National Institute of Technology Rourkela, India.

[4] G.Jovanovi´c, M. Stojcev,(2007), "A Method for Improvement Stability of a CMOS Voltage Controlled Ring Oscillators", *ICEST* , Proceedings of Papers, Vol. 2, pp. 715-718, Ohrid.

[5] H. Z. Lei, (2004), "High Frequency Phase-Locked Loop Design and Simulation", Thesis (B.S.), California Polytechnic State University, Microfiche. San Luis Obispo, Calif: MPI Microfilm Service.

[6] Kashyap K. Patel and Nilesh D. Patel.(2013), " Phase Frequency Detector and Charge Pump For DPLL Using 0.18µm CMOS Technology" *International Journal of Emerging Technology and Advanced Engineering* , ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3 Issue1, Page No. 55-58.

[7] Kruti P. Thakore, Harikrishna C. Parmar and Dr.N.M. Devashrayee, (2011), "High Speed PFD with Charge Pump and Loop Filter for Low Jitter and Low Power PLL", *IJECT*, Vol. 2, Issue 2.

[8] Rahajandraibe, A.W., L. Zaid, V.C. de Beaupre and J. Roche, (2007) "Lowgain-wide-range 2.4-GHz phase locked loop"*14th IEEE International Conference on Electronics, Circuits and Systems.*