

# A Fault Tolerance Technique For Combinational And Sequential Circuits Using Triple Modular Redundancy Technique

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**Abstract-** Reliability is one of the most critical factors that have to be considered during the designing phase of any IC. In critical applications like Medical equipment & Military applications this reliability factor plays a very critical role in determining the acceptance of product. Insertion of special modules in the main design for reliability enhancement will give considerable amount of area & power penalty. So, a novel approach to this problem is to find ways for reusing the already available components in digital system in efficient way to implement recoverable methodologies. Triple Modular Redundancy (TMR) has traditionally used for protecting digital logic from the SEUs (single event upset) by triplicating the critical components of the system to give fault tolerance to system. TMR technique provides recovery for all internal faults. Hence, proposed design will be more efficient & reliable to use in critical applications, than any other design present till today.

## I. INTRODUCTION

Reliability with respect to soft errors has become a critical issue in digital circuits. In the past few decades, CMOS technology has reached high scaling advancement. This advancement is consistent with Moore's law, which states that the number of transistors that can be placed in a chip doubles every 18 months. As CMOS technology is reaching the nanometer scale, quantum mechanical effects cause many challenges for additional scaling of CMOS devices. Soft errors are transient errors that can cause digital circuits to operate incorrectly. Soft errors are mainly caused by cosmic-ray neutrons or alpha particles in device packaging. If these particles strike sensitive areas of the circuit, they may result in transient glitches at primary outputs. In previous generations of packaging technology.

The effect of soft errors caused by alpha particles can be almost neglected. Hardware redundancy methods are based on adding redundant hardware to maximize the masking of errors. Triple Modular Redundancy (TMR) is one of the most well-known hardware redundancy techniques. TMR consists

of three functionally identical copies of the original circuit that feed a 2-out-of-3 majority voter. TMR suffers from high overhead in terms of area and power (more than 200%). In this technique, a module is used to select the correct result, based on the history index of correct computation (HICC). Instead of using merely majority voting to transmit results, the HICC module uses the history indices of redundant units to transmit the correct computation. The most reliable unit is the unit with the highest history index. A generalized modular redundancy scheme is proposed for enhancing the fault tolerance of combinational circuits. In this technique, only the output combinations of the circuit with a high probability of occurrence are protected. This limited protection reduces area overhead compared to TMR. In synthesis-based techniques, a combinational circuit is restructured to maximize the masking properties of a circuit. Logical masking is the main masking property to be maximized. In the logical masking of errors is increased by taking advantage of conditions already present in the circuit, such as observability don't-care terms. Observability don't-care terms are input conditions that will make the output of a circuit not observable. Two techniques are used to improve reliability: don't care-based re-synthesis, and local rewriting. In the first method, high-impact nodes are identified. A node has high impact if many observable faults flow through it. High-impact nodes are used to select areas of the circuit for restructuring, in which a vulnerable node is replicated by adding a single gate. Local rewriting is also used to optimize small sub-circuits to obtain overall area improvements. In two algorithms are proposed to improve input error resilience. They focus on input error due to propagated failures from previous blocks. Both algorithms determine 0–1 assignments for the most critical don't-care terms.

## II. LITERATURE SURVEY

To overcome the drawbacks of QL and QT[3], a hybrid design using QT in QL is proposed to enhance the gates that generate the primary outputs in a QL circuit. In a QLQT implementation of the benchmark C17, for example,

the two NAND gates at the last logic layer are implemented using QT. This provides a significant advantage over QL. However, a critical error at the third last layer that would be corrected in QL, may not be necessarily corrected in a QLQT circuit; this is caused by the fan-outs of the subcritical errors induced at the second last layer onto the last QT structures. However, these errors may not cause an erroneous output due to: 1) the errors may propagate to two transistors that are not in parallel in QT; and 2) the errors may be corrected by other signals due to their subcritical nature.

**III. EXISTING SYSTEM**

Designing reliable systems, while eschewing the high overheads of conventional fault tolerance techniques, is a critical challenge in the deeply scaled CMOS and post CMOS era. To address this challenge, we leverage the intrinsic resilience of application domains such as multimedia, recognition, mining, search, and analytics where acceptable outputs are produced despite occasional approximate computations. In this section, we first provide an overview of stochastic checkers and discuss the key issues involved in their design. We then propose strategies to improve the accuracy of stochastic checkers in order to achieve high fault coverage and low false positives. We also outline progressive checking policies that significantly lower the fault detection latency of stochastic checkers. Fig. 2 shows the block diagram of a circuit with a stochastic checker. A stochastic circuit implementing the same function as the original (binary) circuit, along with the necessary BTS and STB converter logic, is placed alongside the original circuit. Since the latency of the original circuit and the stochastic checker may differ, the checker samples the original circuit’s inputs and outputs. Once the stochastic checker completes evaluation, the binary and stochastic outputs are compared

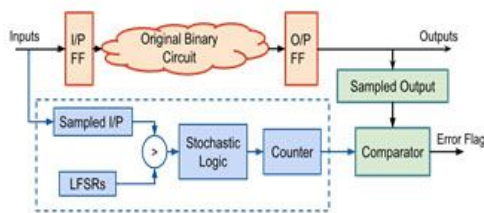


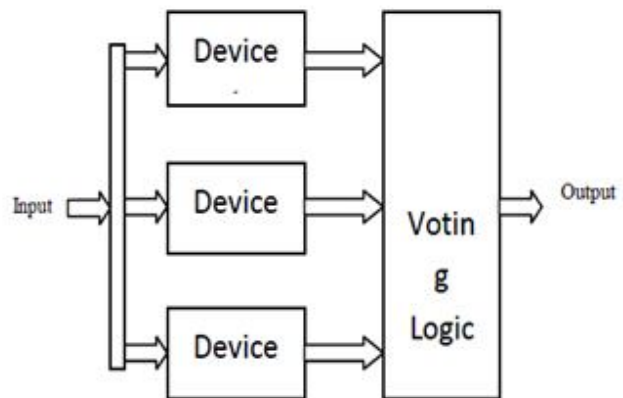
Fig. 2. Stochastic checkers: overview.

to determine whether there is an error. We next discuss how the comparison of the binary and stochastic outputs is performed. Since stochastic circuits are intrinsically approximate, there is a small error in the output of the stochastic circuit. Therefore, an exact (equal-to) comparison of the checker’s output with the original circuit output will frequently declare an error even when the original circuit

output is correct (we refer to this phenomenon as a false positive). Fault tolerance techniques, is a critical challenge in the deeply scaled CMOS technology. The stochastic checkers (checkers designed using stochastic logic) as a approach to performing error checking in an approximate manner. Stochastic checkers are inherently inaccurate and require long duration for computation.

**IV. PROPOSED SYSTEM**

An alternative way to have a fault less system is Fault Tolerant System, Triple Modular Redundancy (TMR) is used for making a fault tolerant system for Multiplexer, DFF, and Binary to gray code converter. FPGA platform used in Altera Cyclone kit and Altera Quartus II software is for functional and timing simulation. This model not only detects the faulty processor but also repair the faulty bits in the faulty processor. Fault detection are done over the air means at the same time. By using this TMR model, the faulty processor is detected as well as the



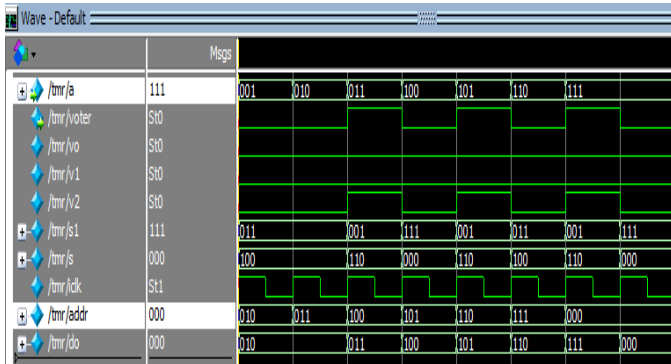
administrator will be able to know that fault lie in which bit of which processor.

**FIGURE A BLOCK DIAGRAM OF TMR**

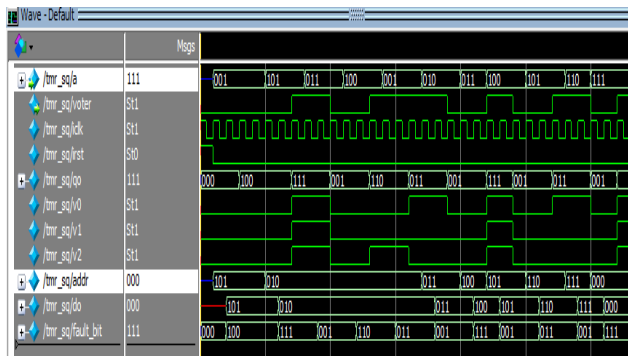
Inside and generate a different output. This inconsistency will be caught and corrected by voting logic. Thus the voted output is always a correct value under the assumption of single error. Thus, the voted output is always a correct value under the assumption of single error. When the TMR concept is applied to a processor (system), all output signal of the CPU are voted; therefore no error should exist at output of voters. Any error that occurs represent that one of the CPUs has an error inside. If that error is not corrected by some way; it may result in more errors and finally become unrecoverable.

In the design of fault-tolerant systems, the designer must consider the possible occurrence of several different kinds of faults such as transient faults, intermittent faults, permanent, logical faults, and indeterminate faults. Transient faults, often caused by external disturbances, exist for a finite length of time and are nonrecurring. Intermittent faults occur periodically and typically result from unstable device operation. Permanent faults are perpetual and can be caused by physical damage or design errors.

**V. RESULTS**

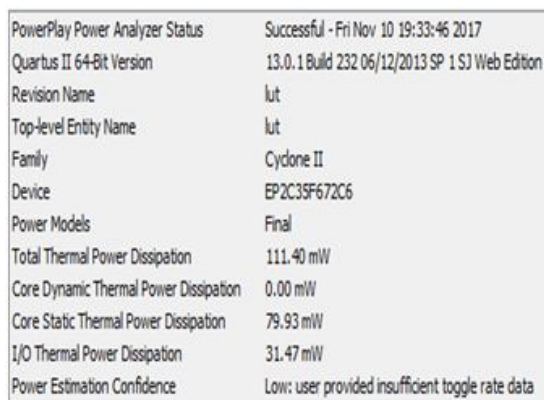


**FIGURE a. TMR COMBINATIONAL LOGIC**

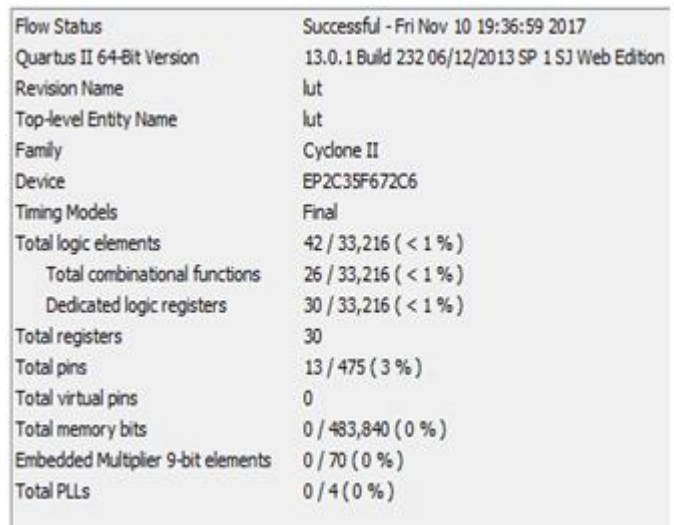


**FIGURE b. TMR SEQUENTIAL LOGIC**

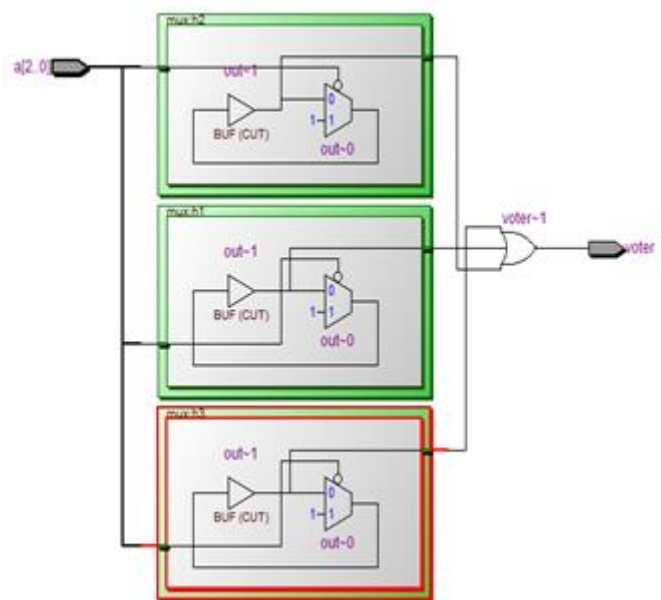
**VII.SYNTHESIS REPORT**



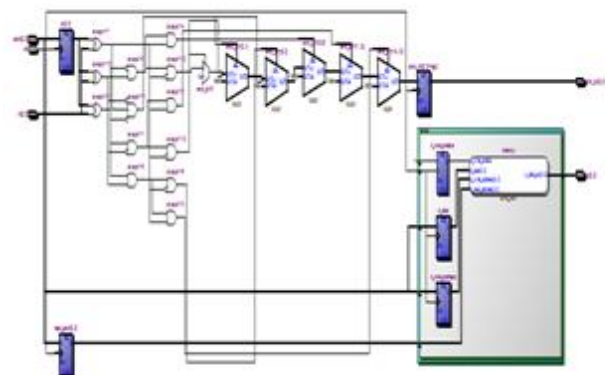
**FIGURE A. AREA REPORT**



**FIGURE B. POWER REPORT**



**FIGURE C. RTL VIEW FAULT TOLERANT**



**FIGURE D. TMR FOR COMBINATIONAL LOGIC**

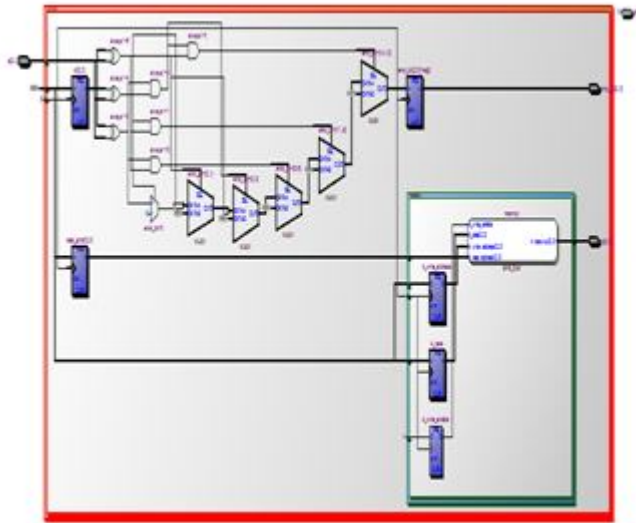


FIGURE E. TMR FOR SEQUENTIAL LOGIC

### VIII. CONCLUSION

TMR-based ALU fault tolerance technique for combinational circuits has been discussed in literature papers. This proposed technique can be applied DFF, Multiplexer, code converter to achieve a given circuit reliability or enhance the reliability of a circuit under a given area constraint. This system evaluates the processor and checks for the faulty bits in the processor. By evaluating the faults in the processor prevents the whole system from collapsing. With the help of TMR administrator will come to know which of the processor is diverting from regular program and they will able to take the appropriate action based on the results. This system detects the faults in the systems.

### REFERENCES

- [1] Kashif Sagheer Siddiqui, Mirza Altamash Baig,, “FRAM based TMR (Triple Modular Redundancy) for Fault Tolerance implementation”, Proceedings of The Sixth IEEE International Conference on Computer and Information Technology (CIT'06), 2005
- [2] Wei Chen, Rui Gong, Fang Liu, Kui Dai, Zhiying Wang, “Improving the Fault Tolerance of a Computer System with Space-Time Triple Modular Redundancy”, Proceedings International Conference on Dependable Systems and Networks, pp. 389-98, 23-26 June 2006
- [3] Mark Hunger and Sybille Hellebrand, “The Impact of Manufacturing Defects on the Fault Tolerance of TMR-Systems”, 25th International Symposium on Defect and Fault Tolerance in VLSI Systems, (2010)

- [4] Chris Winstead, Yi Luo, Eduardo Monzon, and Abiezer Tejada, “An error correction method for binary and multiple-valued logic”, 41st IEEE International Symposium on Multiple-Valued Logic, 2011.
- [5] Jun Yao, Ryoji Watanabe, Kazuhiro Yoshimura, Takashi Nakada, Hajime Shimada, and Yasuhiko Nakashima, “An Efficient and Reliable 1.5-way Processor by Fusion of Space and Time Redundancies”, IEEE TRANSACTION, 2011.
- [6] Jakob Lechner, “Designing Robust GALS Circuits with Triple Modular Redundancy”, Ninth European Dependable Computing Conference, 2012.