A Review on Different Style of D Flip-Flop

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Abstract- *Flip-flop is a fundamental building block of memory, according to necessity we can use different flip flops, usually D flip-flop is used. Here different style of D flip-flop implementations of is discussed, that is used to reduce the area. The flip flop or latch in the circuit that has two fixed states and can be used to store state data. The D flip flop is the edge trigger device. A positive edge trigger and the negative edge trigger flip flop of low area. Dual-edge triggered Flip-Flop designed at CMOS technology. In DETFF identical data throughput can be reached with half of the clock frequency as related to single edge triggered Flip-Flop. In this paper we discussed SCDFF, DEPFF and SEDNIFF respectively. Therefore the proposed DETFF design is suitable for small area applications.*

Keywords- High Speed, small area, Static D F/F. dual- edge triggered F/F, DETFF & SETFF.

I. INTRODUCTION

The present improvement in computing science has set a goal of working with small area consumption for VLSI designer. Flip-Flops are valuable timing component in digital circuits have a good contact on circuit area and speed. The performance of the Flip-Flop is an important element to determine the performance of the whole synchronous circuit, particularly in deeper pipelined design. For improving the performance one innovating approach is to increase the clock frequency. However, using high clock frequency has many disadvantages. Power consumption of the clock system increases dramatically and clock uncertainties take significant part of the clock cycle at high frequencies. Moreover the non-ideal clock distribution results in degradation of the clock waveforms this is dissipated due to clocking network, and the Flip-Flops. An alternate clocking access is placed on the use of storage component which are able to catch data on both rising and falling edges of the clock. Such storage components are described as Dual-Edge Triggered Flip-Flops (DETFFs). In this scheme, equivalent data throughput can be reached at half of the clock frequency as correlated to single edge triggered Flip-Flops. In the other way we can say that double edge clocking can be usage to save half of the area in the clock transportation system.

However it decreases the area of the designed circuit. Reduction in clock frequency is another alternative to reduce the area, with half of the clock frequency as compared to SETFF.

The paper is organized as follows-

II. FLIP FLOP STRUCTURES

In some of the designs DETFF approach is preferred to reduce area. Different SETFF, data is cache by both edges of the clock. design of DETFF is shown in Fig 1. In fig. positive edge triggered D flip flop and negative edge triggered D flip flop linked by multiplexer.

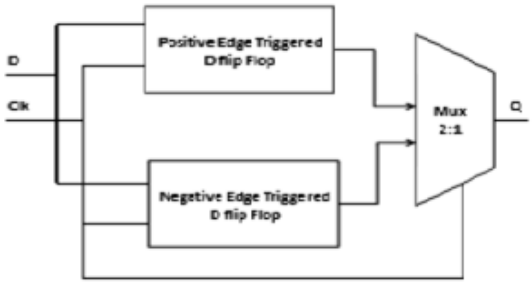

Fig.1 dual edge triggered flip flop

Both positive edge triggered D flip flop and negative edge triggered D flip flop are used to sample the D input at alternate clock edges, and the appropriate sample is selected for the Q output by a clocked multiplexer (MUX). As shown in Fig 1.

III. CONVENTIONAL DUAL-EDGE TRIGGERED FLIP-FLOPS

In 2005 M.W. Phyu proposed a static output-controlled discharge Flip–Flop (SCDFF). SCDFF is realizing by Cross-coupled inverters to carry the data at the o/p Q. However, race problem is there in the cross-coupled inverters, which not only degrades the speed of charging and discharging, but also reduce the area.

In 2010 Yan-yun Dai et.al, proposed a dynamic explicit-pulsed double-edge triggered Flip–Flop (DEPFF) ,

Which is a pulse-triggered Flip–Flop. To pre charge the internal node an always ON PMOS transistor is used in DEPFF pulse generator circuit, but it results in a short-circuit current in the scenario when the discharge path is also ON.
In 2012 Xue-Xiang Wu et.al, projected a static specific - pulsed dual edge triggered F/F with latch node built-in (SEDNIFF). In the SEDNIFF, a pulse generator generates narrow pulses in the circuit at both rising and falling edges of the clock.

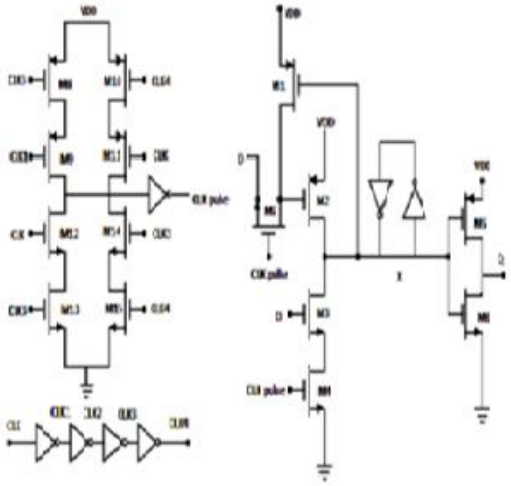

Fig.2 SEDNIFF Circuit

In the SEDNIFF the charge paths, VDD to clock-pulse are OFF when the discharge paths, clock-pulse to ground are ON, to reduction in area, Because no. of clock transistors present in the clock generator. As shown in Fig 2.

IV. PROPOSED DUAL-EDGE TRIGGERED FLIP-FLOP.

In the proposed DETFF, positive latch and negative latch are connected in parallel. In These latches are develop using one transportation gate and two inverters connected back to back and o/p of both the latches are connected to 2:1multiplexer as i/p. Multiplexer is develop using one PMOS and one NMOS connected in series and gates are connected together. Output of multiplexer is connected to the inverter for strengthening the output. Back to back connected inverters hold the data when transmission gate is OFF and at the same time multiplexer sends the latched data to the inverter to get the correct D at the output.

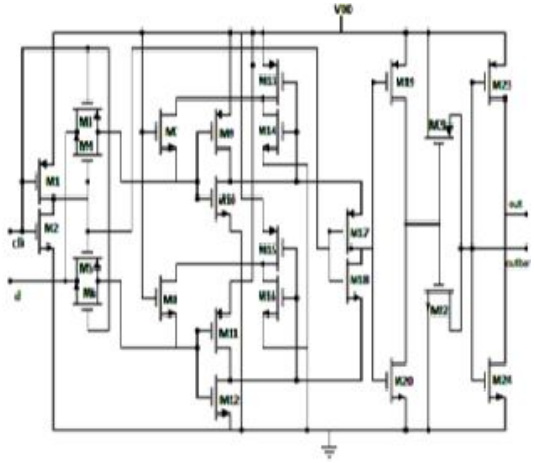

Fig.3 DETFF circuit.

The DETFF work. When the clock is low M3, M4 and M18 are ON and M5, M6 and M17 are OFF. the data hold by negative latch is transparent to Q. When clock is high M5, M6 and M17 are ON and M3, M4 and M18 are OFF. If input D remains the same, Q also remains same. if D is changed before the clock then D will be hold by positive latch and the same value will be send to the output when clock changes from Low to high and similarly for the transition of clock from high to low. As shown in Fig 3. SET D FLIP- FLOP develop common sixteen- transistor SET D flip-flop run either rising edge or falling edge of the clock. The right operation of the flip-flop, the input value is maintain stable before setup time and after hold time of the triggering edge of the clock. Sixteen-transistor SET D flip flop [1, 6]. Master and slave branch are differentiate by vertical line. PMOS transistor is usage for feedback path and the point to a more compact design then the NMOS transistor. The high noise surroundings, transistors may be replaced with transportation gate. As shown in Fig 4.

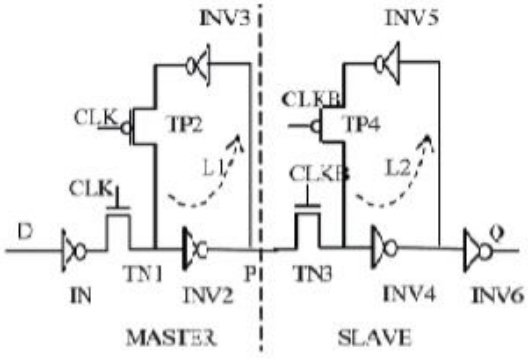

Fig.4 conventional SET D-FF

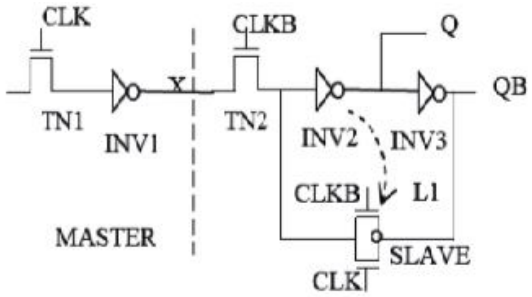

Fig.5 10T SET D-FF

The layout of ten-transistor negative edge triggered SET D F/F. These designs the feedback circuit of the master region is removed and slave section, feedback loop subsist of transportation gate. When the state of clock is at 'HIGH', master latch in active mode and inverse the data is saved to a middle node X. When the clock is goes to 'LOW' logic level, the slave latch consisting of transistor TN2 and regenerative feedback loop L1 becomes functional and produces data at the output Q and QB. The D F.F can maintain its logic state even when the clock is removed or stopped, this property of the flip flop shows its static nature. The aspect ratios of the transistors involved in the SET D flip-flop. The aspect ratios of the transistors involved in regenerative feedback are made weak to provide weak feedback. When we compare the SET D flip flop of conventional type we found that the new developed 10-transistor SET D flip flop is required less number of flip flop. As shown in Fig 5. The circuit evolves into dynamic in nature if the transportation gate is removing in the feedback loop. The primary aim of this paper is to revise the ten-transistor arrangement is reduce the overall space such that the design evolves into agreeable for the less area use. To progress with this, the architecture is first converted by changeable the substrate contact. Substrate of all PMOS transistors are affiliated to the ground and substrate of all NMOS transistors are affiliated to the supply voltage (Vdd). In this type of substrate connection, bulk voltage is less than the source voltage (VB < VS). the result of all devices get an amount of forward bias equal to Vdd. Substrate of all NMOS and PMOS transistors are linked to ground. This type of substrate contact overcomes the complication of the architecture. All the NMOS transistors are reverse bias position and all PMOS are forward bias position. Sub Threshold Ground Body (STGB) design is minor more responsive towards supply and ground noise than Low Voltage Swipe Body (LVSB) design. The substrate of the MOSFET is affiliated to the source and the VSB of the MOS transistor is continually at zero it is called as No Body Bias (NBB) condition. In NBB connection, the MOSFET transistor is continually fixed.

V. CONCLUSION

Structure of Different style of D Flip-flop were studied. Dual-Edge Triggered Flip-Flops, Conventional Dual-Edge Triggered Flip-Flops, conventional SET D-FF and 10T SET D-FF. These can be used according to the requirement such a low power, small area and high speed. The use of multi bit flip-flops can achieve area reduction. Power reduction reduces the chip area. Its application is mostly oriented in area and delay. The future scope of flip flop is to reduce the area. Dual-edge triggered Flip-Flop (DETFF) is very well suited for small area applications.

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