Implementation of Convolution Encoder & Various Decoding Algorithm

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Abstract- *Convolution encoding with Viterbi decoding is a good forward error correction technique suitable for channels affected by noise degradation. Fangled Viterbi decoders are variants of Viterbi decoder (VD) which decodes quicker and takes less memory with no error detection capability. Modified fangled takes it a step further by gaining one bit error correction and detection capability at the cost of doubling the computational complexity and processing time.*

Keywords- Convolution Encoder, Forward Error Correction, Bit Error Rate, Viterbi Decoding.

I. INTRODUCTION

Convolution coding is a bit-level encoding technique. Convolution codes are used in applications that require good performance with low implementation cost. Using convolution codes a continuous sequence of information bits is mapped into a continuous sequence of encoder output bits. The encoded bits depend not only on current k input bits but also on past input bits. This mapping is highly systematic so that decoding is possible. As compared with the block codes, convolution codes have a larger coding gain.

We are implementing convolution encoder using different decoding algorithm like Viterbi algorithm, Sequential decoding & feedback decoding. Here we have used Viterbi decoding algorithm we are simulating these algorithm in MATLAB & XILINX. In order to check the error probability, efficiency, simplicity, speed, accuracy & Performance.

Also implementing FPGA i.e Flied Programmable Gate Array using XILINX. Implementation of Viterbi decoder on FPGA for performance improvement which is more demanding task.

II. SYSTEM OVERVIEW

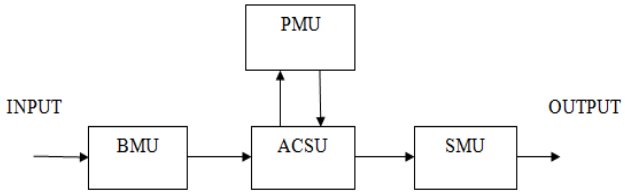

Figure 1. Block diagram of viterbi decoder

The basic units of viterbi decoder are branch metrics, Add compare select and Survivor management unit. Figure 1 shows the general structure of a Viterbi decoder. It consist of three blocks: the branch metric unit (BMU), which computes metric the add–compare–select unit (ACSU), which selects the survivor paths for each trellis state, also finds the minimum path metric of the survivor paths and the survivor management unit (SMU), that is responsible for selecting the output based on the minimum path metric.

Branch Metric Generation Unit – The BMU is the simplest block in the Viterbi decoder design. However, the operation of BMU is crucial as it is the first stage of the Viterbi algorithm and the consequent decoding process depends on all the information it provides. In a hard-decision Viterbi decoder, the BMU design is straightforward since the BMs are the Hamming distances between the received code words and expected branches. For a soft-decision Viterbi decoder, the received code words are quantised into different levels according to the signal strength then the BMU maps the levels of code words into BMs according to their likelihood.

Add Compare Select Unit - The add compare select unit also known by the path metric unit (PMU) calculates new path metric values and decision values. Because each state can be achieved from two states from the earlier stage, there are two possible path metrics coming to the current state. The ACS unit, as shown in figure2.10, adds for each of the two incoming branches the corresponding states path metric, resulting in two new path metrics. The path with the better metric is chosen and stored as the new path metric for current state, while generating a decision bit.

III. SYSTEM OVERVIEW

The flowchart shows the overall operation of system in accordance with software.

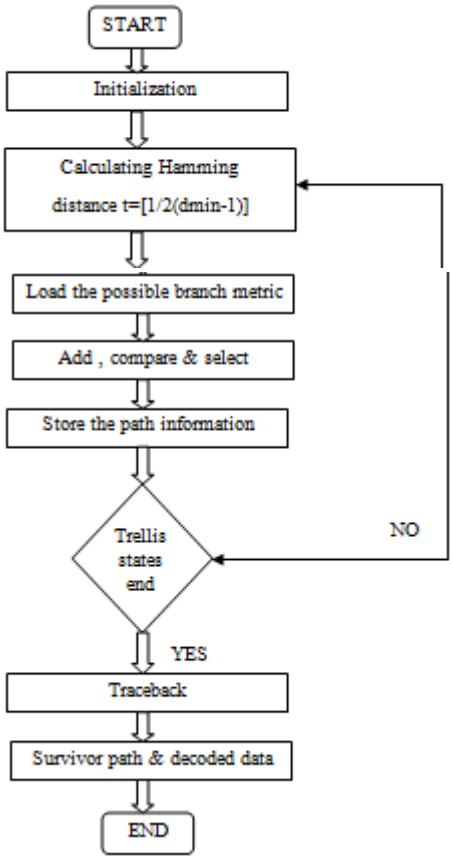

Fig 2: Flowchart of Matlab process.

IV. SYSTEM OVERVIEW

Software Description

A. MATLAB

The name MATLAB stands for matrix laboratory. MATLAB was originally written to provide easy access to matrix software developed by the LINPACK and EISPACK projects, which together represent the state-of-the-art in software for matrix computation. MATLAB has evolved over a period of years with input from many users. MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation.

B. XILINX

Xilinx ISE(Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the Model Sim logic simulator is used for system-level testing.

C. TURBO C

C Programming is an ANSI/ISO standard and powerful programming language for developing real time applications. C programming language was invented by Dennis Ritchie at the Bell Laboratories in 1972. It was invented for implementing UNIX operating system. C is most widely used programming language even today. All other programming languages were derived directly or indirectly from C programming concepts.

Harware Module Of Project

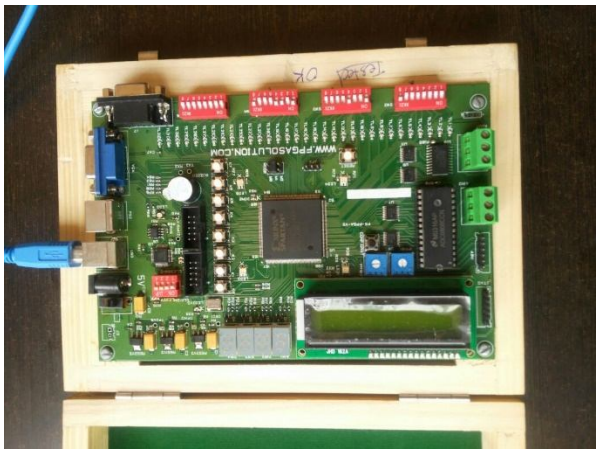

Figure 3. Hardware Module Of Project

Encoding Output: On MATLAB

```
Enter constraint length3

K =

     3

Enter generator vector-G1[ 1 0 0 ]
Enter generator vector-G2[ 1 1 1 ]
Enter generator vector-G3[ 1 0 1]
Enter input sequence[ 1 0 1 1 0 0]

code =

  Columns 1 through 15

     1     1     1     0     1     0     1     0     0     1     0     1     0     0     1

  Columns 16 through 18

     0     1     1
```

Figure 4.

Decoding Output: On MATLAB

```
Enter constraint length3

K =

     3

Enter generator vector-G1[ 1 0 0 ]
Enter generator vector-G2[ 1 1 1 ]
Enter generator vector-G3[ 1 0 1]
Enter input sequence[ 1 0 1 1 0 0]

code =

     1     1     1     0     1     0     1     0     0     1     0     1     0     0     1     0     1     1

Enter recieved code[ 1 1 1 0 1 0 1 0 1 1 0 1 0 0 1 0 1 1 ]
traceback length3

encoded_seq =

     1     0     1     1     0     0
```

Figure 5.

V. APPLICATIONS

- AM Receiver.
- PM Receiver.
- FM Receiver.
- TV Receiver.

VI. CONCULSION

As we have studied the design of a convolution encoder with a Viterbi decoder that can encode a bit stream of digital information and outputs a code word that has a capability to be transmitted to the destination and then decoded .The encoder was designed with constraint length 4 and rate 1/2.The Viterbi decoder design had been driven in such a way that it would calculate the decoding path with the minimum metric to be passed to the decoder output port.

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