Design and Simulation of Bias-Tee in S Band

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Abstract- *Bias Tee is RF circuit which is used to carry RF signal as well as DC signal together through the same cable . Design components are based on the value of the frequency. In this work Bias Tee is designed for 2.7 GHz to 3.1 GHz using ADS tool.*

Keywords- ADS, Impedance Match ,Isolation, S parameter

I. INTRODUCTION

A bias tee is a three-port network used for setting the DC bias point of some electronic components without disturbing other components. The bias tee is a diplexer. The low-frequency port is used to set the bias; the high-frequency port passes the radio-frequency signals but blocks the biasing levels; the combined port connects to the device, which sees both the bias and RF. It is called a tee because the 3 ports are often arranged in the shape of a T . Bias Tee using lumped component is shown in fig 1 . Conceptually, the bias tee can be viewed as an ideal capacitor that allows AC through but blocks the DC bias and an ideal inductor that blocks AC but allows DC. Although some bias tees can be made with a simple inductor and capacitor, wideband bias tees are considerably more complicated because practical components have parasitic elements.

Bias tees are designed for transmission-line environments. Typically, the characteristic impedance Z_0 will be 50 ohms or 75 ohms. The impedance of the capacitor (X_C) is chosen to be much less than Z_0, and the impedance of the inductor (X_L) is chosen to be much greater than Z_0:

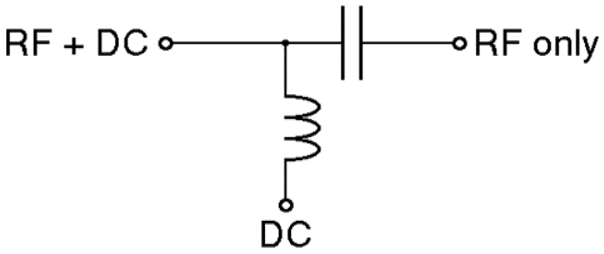

Figure 1. Basic Bias Tee Network

II. BIASING NETWORK

A basic bias network should have a DC block and an RF choke. DC block should have low impedance for shorting the operating frequencies. RF choke should have high impedance for preventing leakage of RF signals through the biasing network. It acts as DC short while blocking RF signals. An impedance of 500-1000Ω range is accepted for RF choke. For DC block an impedance range of .05-.001Ω is acceptable. Gate current is small as compared to drain current. For HEMT transistors dual power supply is required. Negative voltage for gate and positive voltage for drain is required.

Since we are using a depletion mode HEMT, a negative voltage is generally applied at the gate. The biasing network is realized using microstrip lines. At microwave frequencies, RF choke is realized using an impedance transformer which is terminated by an RF bypass capacitor. A DC block is a capacitor.

DC Analysis in ADS is shown in Figure 2

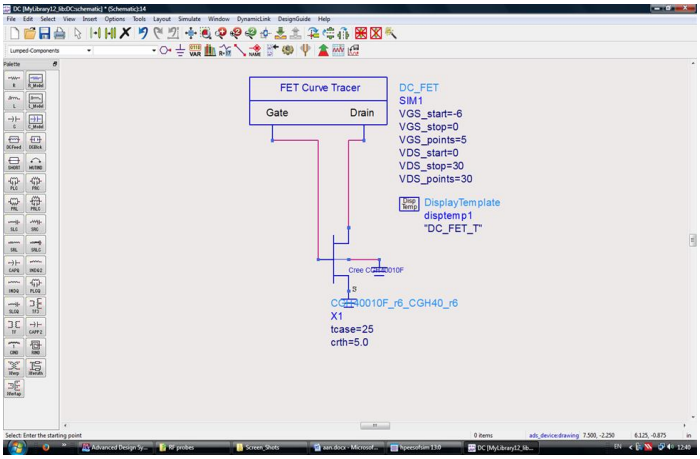

Figure 2. Finding analysis of device model using FET curve tracer DC

After Simulating FET Trace curves in ADS Drain current vs Drain Voltage graph is generated. At V_{gs} = -2 V and At V_{ds} = 28 V the Drain current is 0.785A.

Simulated Drain current vs Drain Voltage graph is shown in fig 3

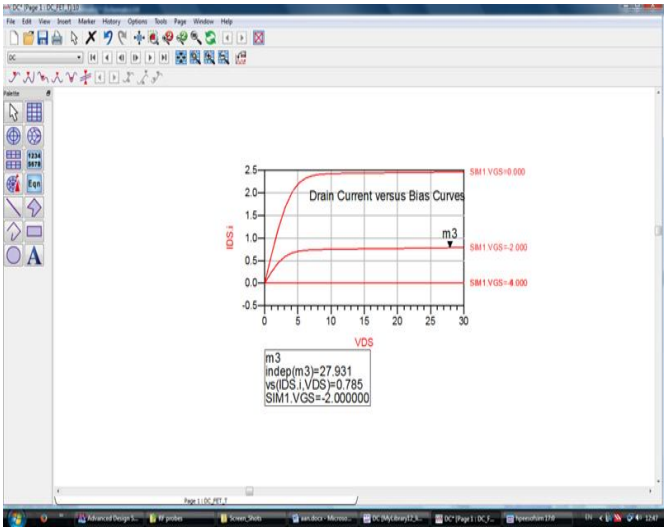

Figure 3.DC I-V characteristics of device model

After studying the I-V characteristics the bias point is set with V_{GS} = -2V and V_D = 28V. Bias-Tee network is designed in ADS Software using Micro strip Line and LTCC PT as Substrate. Designed Bias Tee Schematic is shown in figure 4.

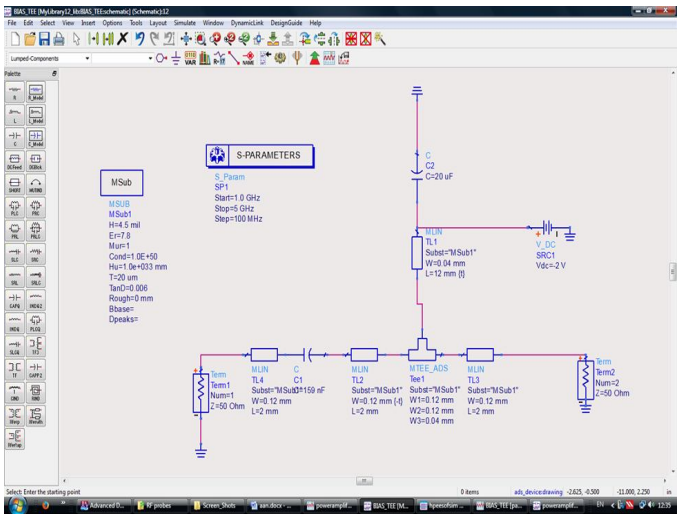

Figure 4. Designed Biasing Network

S parameter simulation for the designed bias network is done. The following Values of S parameter is obtained. RF input is given on the port1 and DC input is applied via TEE junction. RF Signal plus DC signal is obtained from Port2. Simulated graph is shown in Fig 5.

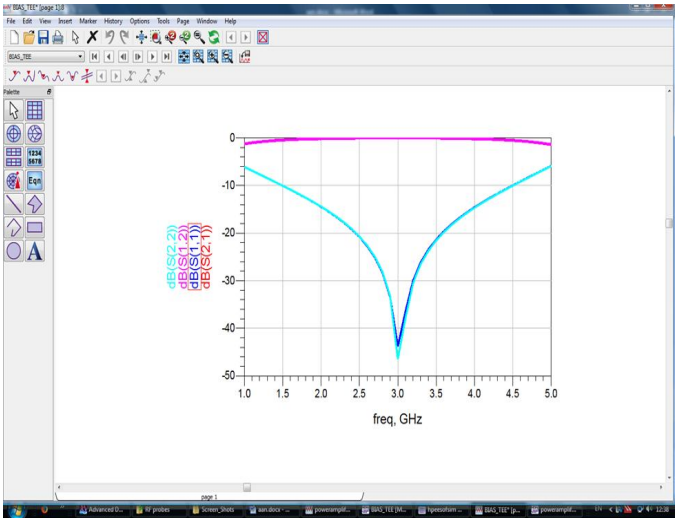

Figure 5. S parameter simulations of bias network

III. RESULT

S12 and S21 are overlapped and is nearly zero around the frequency band 2.7-3.1GHz. Port 1 is the RF port and port 2 is the output port. S_{21} equals 0dB implies complete RF signal that is applied reached the output port. So the insertion loss is zero. S_{11} and S_{22} is the isolation at the input and output ports. Isolation is around -45dB.

IV. CONCLUSION

The Bias Tee design is implemented using ADS . The Designed network can be used to bias HEMT. Bias Tee has been designed for the frequency range of 2.7 GHz to 3.1 GHz.

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