Implementation of Anti-Collision Algorithm Used In RFID Technology

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Abstract- *In RFID on bus anti-collision of data is minimized with help of carrier sense basis for the same first in first out using queue methodology for memories read and write of any information and data using some control logic is proposed. The whole proposed FIFO algorithm work fully dependent on the control circuitry and clock domain. It is often used to control the flow of data from source to destination by the transition of every clock. Basically algorithm differentiate by clock domain either Synchronous or Asynchronous. There are various methods to designing and synthesized algorithm but here fully focused on the memory which is used to store the data in domain of clock either synchronous and asynchronous or single and multiple clock cycles. This paper will present the design, synthesize and analyze a FIFO algorithm using Register file memory by older version of Synchronous. This work shows change the parameters like on-chip components (clock, signal, input and outputs etc), clock domain, type of resources, and how to minimize and optimize hierarchy of the device.The RTL description for the FIFO is written using VHDL language (hardware description language) and results of design simulation and synthesis in Xilinx ISE Design suit and Modelsim.*

Keywords- First in first Out (FIFO), VHDL, Power Optimization, Anti-Collision Algorithm, Radio Frequency Identification (RFID).

Summery of this Results

In this paper we discuss about the FIFO designing for Carrier sense anti-collision using RAM for storage and passing the data from source to destination, as well as we discuss the changes in parameters. The effect of using proposed algorithm, acting much efficient, high speed, less power consumption, and minimize the area of a on-chip components, in a FIFO memory. Firstly we fully concern on the basic architecture of register file and then after designing VHDL code of FIFO, and check test bench, with series of data input till better response is coming. After that checking parameters of that and compare the FIFO design with the other designs.

I. INTRODUCTION

A Synchronous FIFO describes the FIFO design where the data and information is stored in the memory and transition a data in a appropriate fashion using clock pulse. Both read and write operation handle by control circuit. In computer programming, FIFO (first-in, first-out) is an approach to han-dling program work requests from queues or stacks so that the oldest request is handled first. In hardware it is either an array of flops or Read/Write memory that store data given from one clock domain and on request supplies with the same data to other clock domain following the first in first out logic. Basically FIFO divided in two categories like Synchronous and Asynchronous. In synchronous FIFO, write operation to the FIFO buffer and read operation from a same FIFO buffer are occurring in same clock domain. But in asynchronous FIFO these two operation of write and read to and from respectively FIFO buffer in different clock domain. As clear that the clock domain is different in asynchronous FIFO. Write operation is occurred in one clock domain, and read operation is in another clock domain. In FIFO concept, there is a restrictions for writing any data and read data from FIFO memory. In other way we can say that we cant write and read data without fulfill some appropriate conditions, are called fifo full and fifo empty[2]. Here we considered these are two flags which shows status of FIFO condition. In designing time we fully concern on these two flags. If fifo full flag is asserted then the user does not write any data in FIFO buffer and for fifo empty, user does not read any data from FIFO buffer [4]. For assertion of these condition we design pointers to check these conditions. So these pointers are called write and read pointers or we can say, Firstly Read Pointer/Read Address Register. Secondly Write Pointer/Write Address Register.

1. FIFO Empty when read address register catches a write address register, the FIFO asserts the Empty signal [4].

2. FIFO FULL when write address register catches a read address register, the FIFO asserts the FULL signal [4]. FIFO are often used to safely pass data from one clock domain to

another asynchronous clock domain FIFO are used in designs to safely pass multi-bit data words from one clock domain to another. In Async FIFO, Data words are placed into a FIFO buffer memory array by control signals in one clock domain, and the data words are taken from another port of the same FIFO buffer memory array by control signals from a second clock domain. In Sync FIFO, FIFO where writes to, and reads from the FIFO buffer are conducted in the same clock domain.

II. PROPOSED FIFO ALGORITHM

FIFOs are controlled based on methods of control proven in processor systems. Every digital processor system works synchronized with a system-wide clock signal. This system timing continues to run even if no actions are being exe-cuted. Enable signals, also often called chip-select signals, start the synchronous execution of write and read operations in the various devices, such as memories and ports. The block diagram in Figure 1 shows all the signal lines of a synchronous FIFO. It requires a free-running clock from the writing system and another from the reading system. Writing is controlled by the WRITE ENABLE input synchronous with WRITE CLOCK. The FULL status line can be synchronized entirely with WRITE CLOCK by the free-running clock. In an analogous manner, data words are read out by a low level on the READ ENABLE input synchronous with READ CLOCK. Here, too, the free-running clock permits 100 percent synchronization of the EMPTY signal with READ CLOCK. Thus, synchronous FIFOs are integrated easily into common

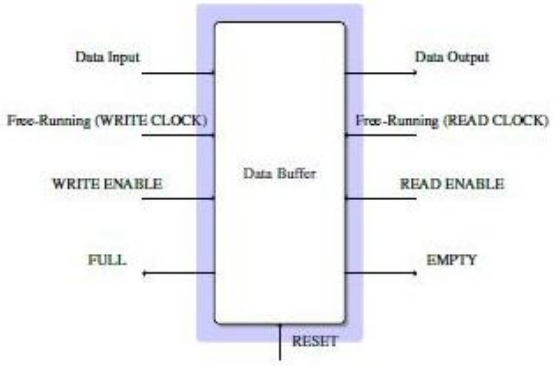

Fig. 1: Proposed FiFo Block Diagram

processor architectures, offering complete synchronism of the FULL and EMPTY status signals with the particular free-running clock. Figure 7, 8 and 9 shows the typical waveform in a synchronous FIFO. WRITE CLOCK and READ CLOCK are free running. The writing of new data into the FIFO is initialized by a low level on the WRITE ENABLE line. The data are written into the FIFO with the next rising edge of WRITE CLOCK. In analogous fashion, the READ ENABLE line controls the reading out of data synchronous with READ CLOCK. All status lines within the FIFO can be synchronized by the two free-running-clock signals. The FULL line only changes its level synchronously with WRITE CLOCK, even if the change is produced by the reading of a data word. Likewise, the EMPTY signal is synchronized with READ CLOCK. A synchronous FIFO is the only concurrent read/write FIFO in which the status signals are synchronized with the driving logic.

III. SIMULATION RESULTS AND ANALYSIS

In this section, after written the VHDL code of fifo using RAM files and create RTL diagrams of FIFO using RAM. After this, concern on output corresponding to given inputs in xilinx(software) simulator. In this simulator we observe test benches. In test bench we get waveform representation of the given parameters and response of the system according to given parameters. The FIFO architecture has six input ports, three output ports and each input port has four virtual channels with each VC having 8 bit input buffers. The data coming to each input port is stored in virtual channels temporarily.

The design is implemented in VHDL on structural Register Transfer Level (RTL) as shown in figure 5 and 6 and it is synthesized and simulated using Xilinx ISE Design Suite 9.2i. The router was prototyped in Vertex 5 Device. The operating frequency of this router is 440.490 MHz. Minimum input arrival time before clock and Maximum output required time after clock is estimated as 2.103ns shown in figure 2. The minimum clock period required is 2.270 ns.

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Timing Summary:
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Speed Grade: -3

   Minimum period: 2.270ns (Maximum Frequency: 440.490MHz)
   Minimum input arrival time before clock: 2.103ns
   Maximum output required time after clock: 4.007ns
   Maximum combinational path delay: No path found

Timing Detail:
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All values displayed in nanoseconds (ns)
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Fig. 2: Timing anlysis summery of proposed system

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	12	19,200	1%	
Number used as Flip Flops	12			
Number of Slice LUTs	31	19,200	1%	
Number used as logic	23	19,200	1%	
Number using O6 output only	23			
Number used as Memory	8	5,120	1%	
Number used as Dual Port RAM	8			
Number using O5 and O6	8			
Slice Logic Distribution				
Number of occupied Slices	9	4,800	1%	
Number of LUT Flip Flop pairs used	31			
Number with an unused Flip Flop	19	31	61%	
Number with an unused LUT	0	31	0%	
Number of fully used LUT-FF pairs	12	31	38%	
Number of unique control sets	4			
IO Utilization				
Number of bonded IOBs	25	220	11%	
Specific Feature Utilization				
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Total equivalent gate count for design	2,305			
Additional JTAG gate count for IOBs	1,200			

Fig. 3: Device utilazation Summery

A. RTL diagram of FIFO

In figure 5 paper i design synchronous FIFO using register file by VHDL code and simulate it, and parameter the effects.

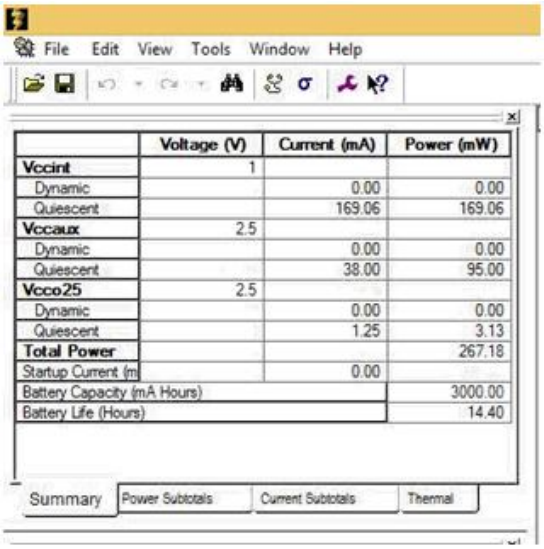
IV. MODELSIM SIMULATION RESULTS

A. Simulation for write data

Figure 7 shows tb waveform of the write data. The data is write in fifo memory. In this figure wdata=10011111 taking as a example for write data in fifo memory.

B. Simulation for read data

Figure 8 shows the output waveform. Here the read data is same as the write data in fifo memory. The time and user constraints are same for initial process. But in this waveform write data is read after some delay because of un-stability of output. The output take some time to give the response against



	Voltage (V)	Current (mA)	Power (mW)
Vccint	1		
Dynamic		0.00	0.00
Quiescent		169.06	169.06
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		38.00	95.00
Vcco25	2.5		
Dynamic		0.00	0.00
Quiescent		1.25	3.13
Total Power			267.18
Startup Current (m		0.00	
Battery Capacity (mA Hours)			3000.00
Battery Life (Hours)			14.40

Fig. 4: Thermal Analysis Summary

Fig. 5: RTL Schematic of Proposed FIFO Algorithm

Fig. 6: RTL of Read and Write Pointer

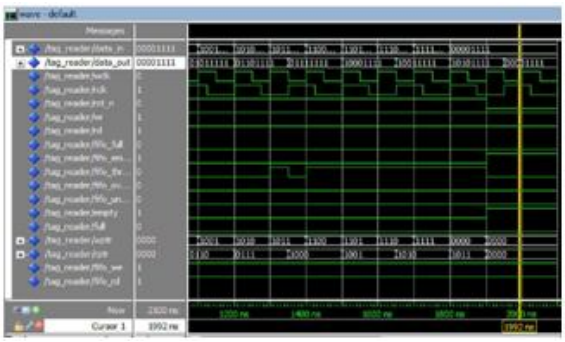


Fig. 7: Modelsim result for write data

write data in fifo memory. But we have a exact output from fifo buffer. Here these figure 7 and 8 shows test bench of write and read data. Let assume we pass a 8 bit data 10011111 passes from write data, then after some delay (because of unstability) the data read from the read data, which is clear in Test Bench. After that we concern on the flags that is empty and full.

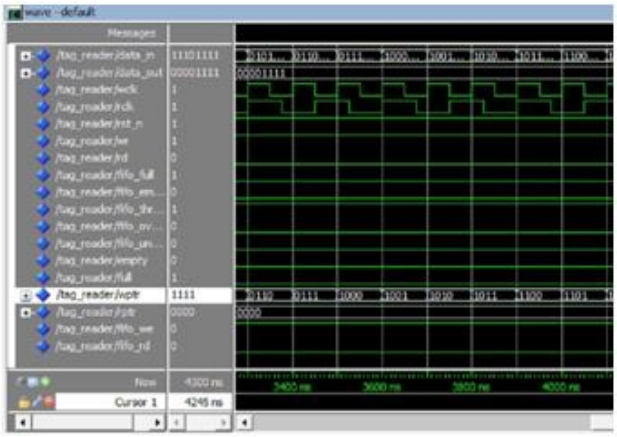


Fig. 8: Modelsim result for read data

C. Simulation for Flags

In figure 9 shows that at the time of reading operation the, EMPTY flag is 1, so the FIFO memory is able to read input data till empty flag is 0, and FULL flag is 0 which mean FIFO memory is not full, when read and write enable are both 1 and reset signal falls to 0. So after simulation part there is comparison between FIFO using RAM.

V. CONCLUSION

The hybrid feedback dependent protocol is developed for avoiding on bus collisions between RFID receiver in to verities of applications. This protocol adapts or switches between time driven and data driven schemes to reduce the power consumption and latency. The proposed protocol accurately analyzes the environment being monitored using only moder-ate resource consumption. The main feature of this research is that to investigate on bus anti-collision algorithm with hardware implementation it consumes low power 267.18 mw and provides high speed of operation upto 440.49 MHz, which will suitable for suitable for real time applications. In further work, an VLSI implementation of processor which incorporates all processing system with smart algorithm for avoiding receiving signal collisions will be considered.

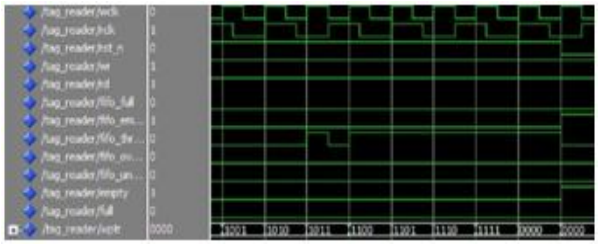


Fig. 9: Modelsim result for flags data

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