Review Paper on Binary Coded Decimal Adder

Surved Pratap Singh[1], Shweta Agarwal[2]
[1]Dept of Electronics and Comm.
[2]Assistance Professor, Dept of Electronics and Comm.
[1, 2] SRCEM Banmore, Morena, India

Abstract- *Adder is the most important component of any application such as digital signal processors (DSP), arithmetic logic unit (ALU), and number as well as logical operations. Therefore the speed of the microprocessor is depends on the performance of the adder. So the designer of integrated circuits are also try to make the digital adder more and more efficient. For developing high performance adder different techniques are adopted till date. The primary concern for designing engineering are minimum power consumes, lower area occupied by the devices, high performance in term of less time delay. Even adders are used by the other components for its operation such subtraction, multiplication etc.*

Keywords- ALU, DSP, Adder, IC , Half adder, Full adder, BCD

I. INTRODUCTION

Digital adders are primary circuits for arithmetic operations such as calculation of addresses, table indices and similar operations [1]. High speed addition and multiplication are fundamental requirements of high performance microprocessors. In microprocessors the arithmetic logic units (ALU) are assigned to for calculation purpose. The digital adder having less power consumption occupies less area and minimum delay is desirable for the high performance processors [2]. As we know that most of the devices which are developed for the portable and mobiles station and all these system works on battery. For long lasting batteries we need to design circuits with high performance. Total power dissipation in CMOS circuits has become a huge challenging in current semiconductor industry due to the leakage current and the leakage power [3].

In CMOS technology, power dissipation mainly contributed by static and dynamic power. The main components that affect power dissipation are capacitive load currents, short circuit currents and leakage currents. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive and it can lead to reliability and IC packaging problems. Power dissipation can be reduced by employing different techniques at different levels of abstraction of the IC design process (system, algorithmic, architecture etc.)[4].

II. TYPES OF ADDER

Digital Adder is a digital device capable of adding two digital n-bit binary numbers, where n depends on the circuit implementation. Digital adder adds two binary numbers A and B to produce a sum S and a carry C.

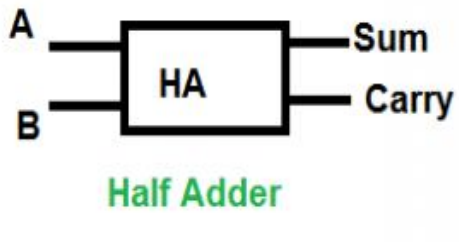


Fig. 1 Block diagram of Half Adder.

The block diagram of half adder is shown in fig. 1.The half adder can is the smallest unit to perform addition function. We can combine the half adder to design the full adder. The full adder is presented in fig. 2. In the fig. 2 we can see that while combining two half adders and put the OR gate to generate carry signal. When we need to process higher bit data we can employ the number of full adders. The full adder is also considered as 1 bit adder. In same manner when we want to add 4 bit data we use 4 one bit adders in series.

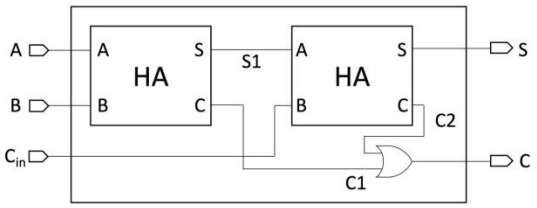


Fig. 2 Block diagram of Full adder using half adder.

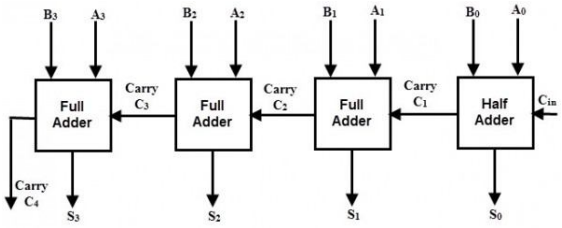
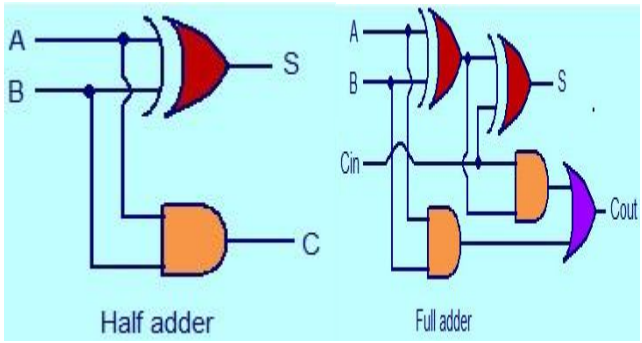


Fig. 3 Cascading of 4 full adders for 4 bit adder.

From the above figure 1 to figure 3 we have observed that we need to provide two inputs. To get back the sum and carry out as output we need to give two inputs and a Carry in. The internal structure of half adder is shown in figure 4. It uses only one XOR gate and a AND gate. It generates two outputs (A & B) – sum (S) and carry(C). Truth table is mention under table 1. Truth table is consisting two inputs these are "a" and "b" and two outputs "sum" and "carry". As we have seen in the table 1 is when both inputs i.e., A and B high than only carry will be high in other conditions it kept on low. But sum will be high when one of the inputs A or B is high.



(a) (b)

Fig. 4 Implementation of Half Adder (a) Half adder and (b) Full adder.

Table 1- Truth table of (a) Half adder and (b) Full adder.

A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a)

Cin	A	B	Sum(S)	Carry(Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b)

III. REVIEWED DIGITAL ADDERS

There are number of adder are available based on different methods. In this section we will review different adder with their efficiency. The primary motive of discussion to find out the adder having high performance and consume less power as well as occupies minimum area. To estimate the performance of device we need the keep three parameters into consideration these are area of semiconductor wafer required to design, speed at which it execute the operations, power which is consumed by core to perform the tasks. On the basis of this there are number of adders some them are Ripple Carry Adder (RCA), Carry-Lookahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder, Carry-Bypass Adder or Carry Skip Adder (CSK).

A. Ripple Carry Adder (RCA)

Full adder is the building block of the highly complicated adders. By using full adders in different combination high end adder are constructed. Such example is ripple carry adder for this full adder are putting in series combination. It accepts three binary inputs A, B and Cin called addend, augends and carry in respectively the two outputs are the sum and the carry-out(Cout).A RCA is built by connecting the full adder, So that the carry out from each full adder is the carry –out from each full-adder is the carry-in to the next stages, the sum and carry bits are generated sequentially starting from the LSB, the Speed of the RCA is determined by the carry propagating time. The one of the most attracting feature if the RCA is is low power requirement for its operations as well as it can be designed using less area [5].

B. Carry Lookahead Adder (CLA)

Carry lookahead-adder is designed to eliminate the ripple carry delay and to overcome the latency introduced by the rippling effect of the carry bits [1]. This method based on the carry generating and the carry propagating functions of the full adder. It plays a vital role in the digital calculation. For the purpose of the operation it adopted the principal of looking mainly for the LSB of the augends whereas addend if a higher order is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate [5].

C. Carry Save Adder (CSA)

The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers. The Carry save unit consists of number of full adders, each of which computes a distinct sum and carries bit based on the corresponding bits of the three inputs numbers. The total sum can then be calculated by altering the carry sequence left by one place and add a 0 to the front of the partial sum sequence and adding this array with RCA produces the result which is (n+1) bit values applied in the partial product line of array multiplier works at superior speed for the carry propagation in the array [5].

D. Carry Select Adder (CSLA)

CSLA is one of the advanced adders. It is one of the important adder is present in most of the complicated arithmetic logic unit. It can be developed by covering very limited area of wafer. Because of the less area the overall delay is reduced to great extent. The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. It uses independent ripple carry adders (for Cin=0 and Cin=1) to generate the resultant sum. The final sum and carry are selected by the multiplexers (mux). A carry-select adder speeds is superior then RCA in terms of operation speed and reducing the maximum carry path[5].

E. Carry Skip Adder (CSkA)

A special up carry chain is used in carry-skip adder. This special up carry chain is also called as skip chain. Carry skip adder is a fast adder compared to ripple carry adder. A CSkA is developed to boost up a wide adder bmy aiding the generation of a carry bit around a share of the entire adder. However the current requirement of industries is to develop a processor which use word length of 32 bits integrated in the desktop computers. These adders have different performance in terms of delay, area and power for same length of binary numbers. [5]

IV. CONCLUSION

After taking the different adder of various bits size we can conclude that the different capabilities. So these are used for number of objectives. But as per the requirement in term of area, power and the clock pluses we can state that the CLA is performed more efficiently. All the coding had been done in the verilog HDL language. The coded is placed in the Xilinx 13.2 ISE . The stimulation is done using Modelsim.

For the purpose of the simulation of CLA the Xilinux software is used. The CLA is tested for the different bit sizes. In every design circuit compulsory to check the design circuits works with required specification. In the following table we can observes the situation brief output.

Table 2 - Comparison of different parameters

Adders	No. of slices	No. of 4 i/p LUTs	Logic Level	Delay
4 bit CLA	6	12	4	7.863
8 bits CLA	11	21	9	12.895
16 bits CLA	18	32	16	19.848

V. BCD ADDER

A BCD adder is a circuit that adds two BCD digits and produces a sum and carry. Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight. Special bit patterns are sometimes used for a sign or for other indications (e.g., error or overflow).

BCD numbers use 10 digits, 0 to 9 which are represented in the binary form 0 0 0 0 to 1 0 0 1, i.e. each BCD digit is represented as a 4-bit binary number. When we write BCD number say 5 2 6, it can be represented as 0101 0010 0110. Here, we should note that BCD cannot be greater than 9. Following table indicates the BCD numbers [6].

Table 3- BCD and its equivalent decimal number

Binary coded decimal	Decimal Number
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
10001	9

The input “a” and “b” loaded in the A1 with carry in. In A1 block the addition of input data have been done in binary format. In CL block is responsible for correction of data. In A2 block If the value is greater than 9 then 6 is added in it. If the value is less than 9 then 0 is adder in it.

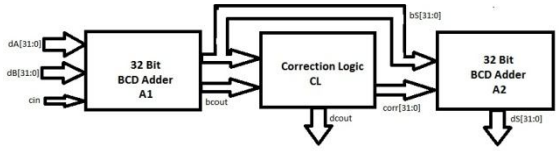


Fig. 5 Block diagram of BCD adder

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