Arithmetic And Logic Unit Using GDI Technique

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Abstract- *In order to meet the growing demand of low power VLSI systems, a low power Arithmetic and Logic Unit circuit is proposed by using GDI logic type of design which considerably increases the speed and decreases the power consumption. An ALU being the most important module of any system which involves computation requires efficiency. So the efficiency can be increased by adding buffer at every cell of GDI. The Full adder, Multiplexer in the ALU is designed in Cadence tool using both GDI and Cmos gate implementation which is one of the used in ALU are replaced by gate diffusion input cell. Finally, comparison is done between Efficiency; power consumed by a normal ALU and ALU implemented using GDI cell.*

I. INTRODUCTION

Power loss is an imperative thought in digital circuit configuration, otherwise called circuit synthesis. Some portion of the issue of vitality scattering is identified with innovative non idealistic of switches and materials. Larger amounts of combination and the utilization of new manufacture forms have significantly diminished the heat loss in the course of the most recent decades. The other piece of the issue emerges from Landauer's guideline for which there is no arrangement [1]. Landauer's rule expresses that logical calculations that are not reversible essentially create kT∗log2 Joules of heat energy for all of data that is lost, where k is Boltzmann's constant and T the total temperature at which calculation is performed.

Outline that does not bring about data loss is called reversible. It normally deals with heat produced because of the data loss. Bennett indicated zero power dissipation would be conceivable just if the system comprises of reversible gates. In this manner reversibility will turn into a fundamental property in future circuit outline. Quantum calculations are known to take care of some exponentially difficult issues in polynomial time. All quantum calculations are essentially reversible [2].

Along these lines examine on GDI logic is advantageous to the advancement of future quantum advances: reversible design techniques may offer ascent to strategies for quantum circuit development, bringing about considerably more intense PCs and calculations.

Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area. T. Esther Rani, M. Asha Rani, Dr. Rameshwar Rao, designed an area optimized low power arithmetic and logic unit in which Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [3]. Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm Using GDI Technique and Its Performance Comparison [4]. The billiard ball model is a model for reversible computations, which among others, was simulated with reversible cellular arrays. It happens that reversible logic naturally appears in many applications that initially do not seem to be connected to reversible logic at all, such as complex antenna simulations. But the essence of the simulation, a process of propagating a wave, is essentially a reversible transformation. We do not discuss the different technologies in detail, since some of their descriptions involve deep knowledge of physics, electronics, circuitry, quantum mechanics, optics, thermodynamics and other physical/engineering subject.

Let's assume we need to understand a 5 input 3 output work in a reversible strategy on a quantum computer, however the design requires 7 extra garbage outputs (that is consistent input sources), bringing about a 10-input 10-output reversible capacity. In the year 2002 the best quantum computer has 7 qubits, accordingly we won't have the capacity to actualize this design.

II. GATE DIFFUSION INPUT TECHNIQUE

A. Gate Diffusion Input logic style (GDI)

Morgenshtein et al. examined a rapid and multipurpose logic style for low power hardware configuration, known as Gate Diffusion Input (GDI), with lessened territory and power necessities, and capable of actualizing a wide assortment of logic functions [5].

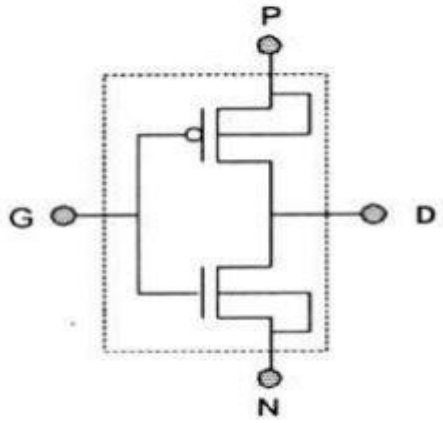

Figure 1: Basic GDI Cell

S.NO	N I/P	P I/P	G I/P	OUTPUT	FUNCTION
1.	0	B	A	A'B	F1
2.	B	1	A	A'+B	F2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

Table 1: Functions of GDI Cell

The GDI logic style approach permits usage of wide scope of multifaceted functionalities utilizing just two transistors. This strategy is hence fitting for plan of fast and low-control circuits utilizing decreased number of transistors contrasted with CMOS and existing PTL logic methods. The GDI logic style strategy utilizes a basic essential GDI cell which looks carefully like the fundamental CMOS inverter at first impression and helps one to remember the standard CMOS inverter, with the exception of present different wonderful contrasts which are recorded below.

1. The essential GDI cell contains 3 inputs: G (regular gate contribution of nMOS and pMOS), P (contribution to wellspring of pMOS), and N (contribution to wellspring of nMOS) while there are no three data sources
2. Bulks of both nMOS and pMOS are associated with N or P separately so with the motivation behind can be self-assertively one-sided which is interestingly with a CMOS inverter.
3. The essential GDI cell permits execution of logic capacities utilizing just two transistors which isn't conceivable with CMOS inverter. We can understand all essential logic gates and general gates likewise with this GDI cell; we can infer that the GDI logic style approach devours less silicon zone contrasted with other logic styles. In perspective of the way that, the zone is less, the estimation of hub capacitances will be less and hence GDI gates have quicker operation which introduces that GDI logic style is a power proficient technique for outline.

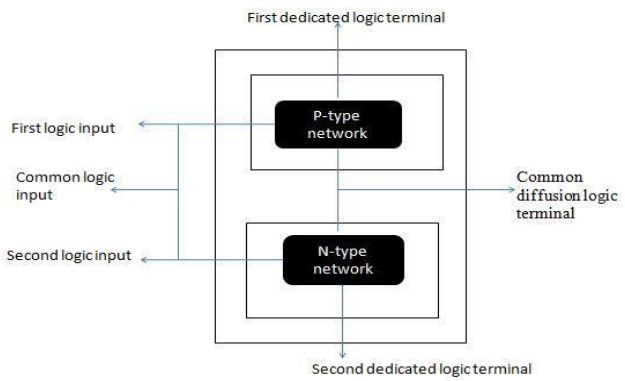

Figure 2: Block Diagram of GDI Cell

The fundamental GDI cell utilizes p-sort and n-type transistors which perhaps will be field impact transistors, CMOS transistors in creation of p-well, n-well, or twin-well process (while p-well and n-well CMOS transistors may be utilized just for a set number of logic circuit setups.), SOI transistors, SOS transistors and so on. There is a reality that the distinction between the source and deplete of the transistor is impossible with the GDI logic style, given that for any transistor the relative voltages between the transistor dissipation hubs changes relying on the logic information and output voltages which is conversely with the standard reciprocal CMOS arrangement in which the source or deplete is coupled to a consistent voltage [6]. Hence, for GDI logic style one of the two transistor dissipation hubs just not the gate is randomly chosen to work for the inward dispersion association, and the other to work for the external dispersion association. Various GDI cell topologies can be actualized in standard p-well or n-well CMOS innovation, because of obstruction of mass impacts under unequivocal information/output conditions, GDI logic style are subsequently ideally executed in either twin-well CMOS or silicon-on-separator (SOI) or silicon-on-sapphire (SOS) advances, which don't encounters these restrictions.

CMOS Implementation of full adder:

This CMOS implementation of Full Adder consists of 28 transistors, here we first generate carry Cout and then use it for finding the sum S.

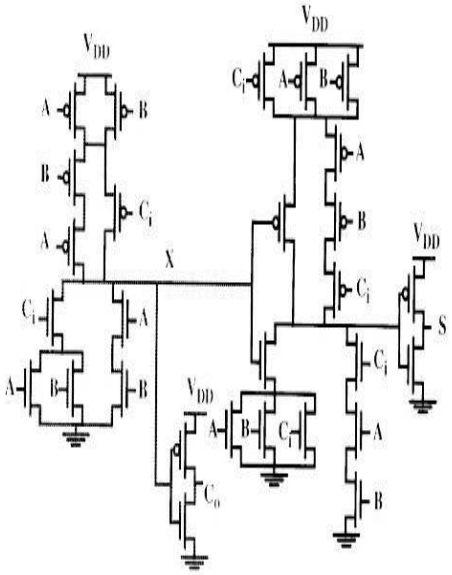

Figure 3: CMOS implementation using Full Adder

Full adder implementation using GDI technique:

This form of implementation has 10 transistors to find out carry and sum of given inputs which allows lesser power consumption than conventional CMOS full adder.

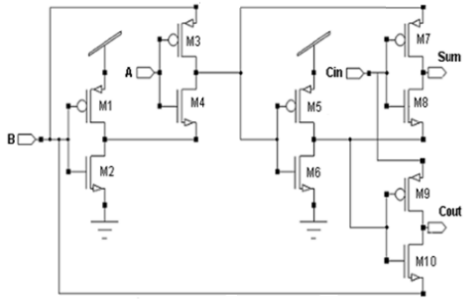

Figure 4: Full Adder Implementation using GDI

III. PROPOSED DESIGN OF 1-BIT ALU

The proposed design of 1-bit ALU can do 2 arithmetic and logic operations which can be selected using selection inputs fo, f1 and with input operands as A, B, Ci. The outputs of the processing unit are c_{out} and result .Where the output of NOT, OR, AND is given as input to the 4*1 multiplexer.

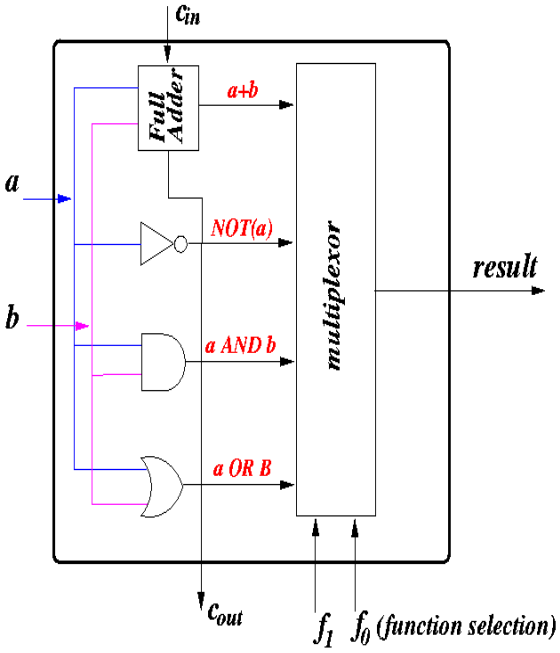

Figure 5: ALU sing CMOS

Truth table of ALU can be given as:

f0	f1	output
0	0	invert
0	1	and
1	0	or
1	1	add/sub

Table 2: Truth table of ALU

ALU using GDI:

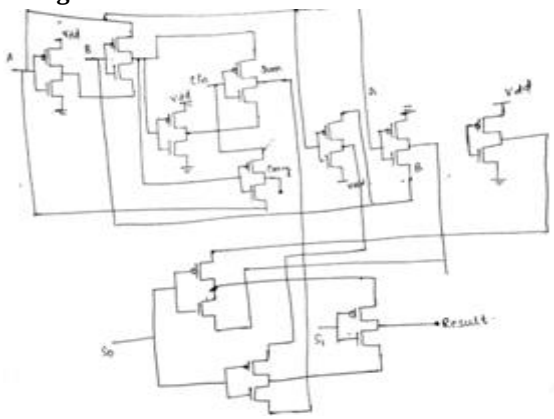

Figure 6: ALU using GDI

IV. SIMULATION RESULTS

B. *CMOS Implementations:*

For the sake of comparison and analysis of different implementation techniques, all the primitive gates and sequential circuits like full adder is implemented using CMOS implementation. In the following section schematic view, output waveform and power analysis using cadence software is presented and values are compared.

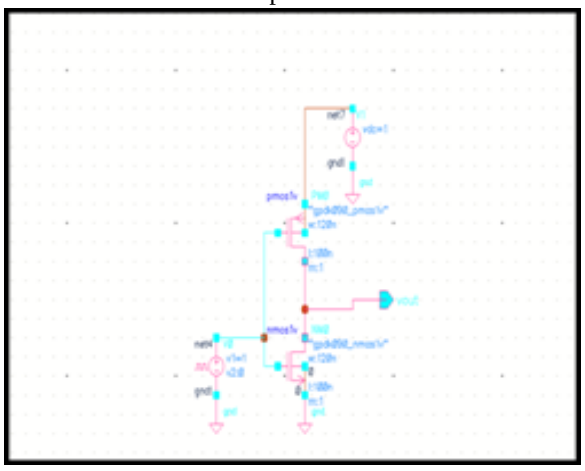

Figure 7: Circuit diagram of INVERTER using CMOS

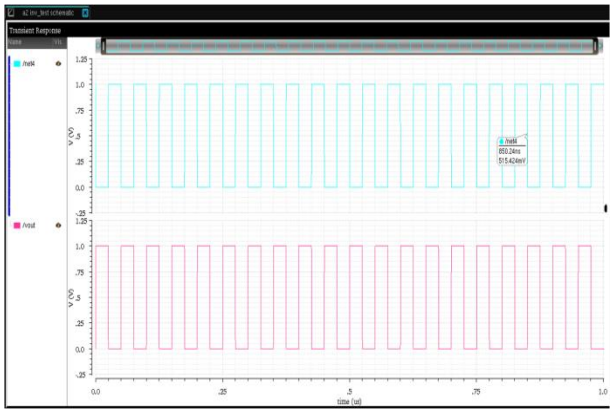

Figure 8: Output Waveform of INVERTER using CMOS

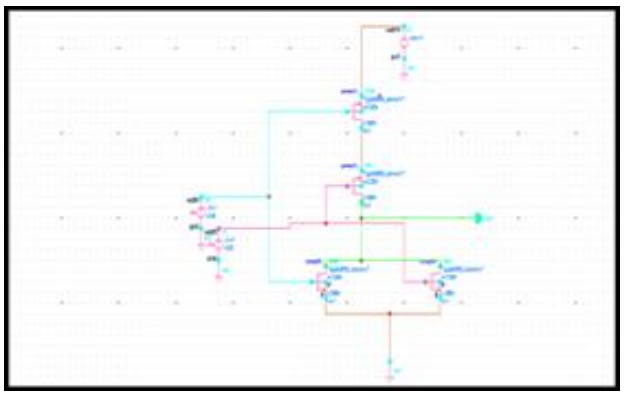

Figure 9: Circuit diagram of NAND using CMOS

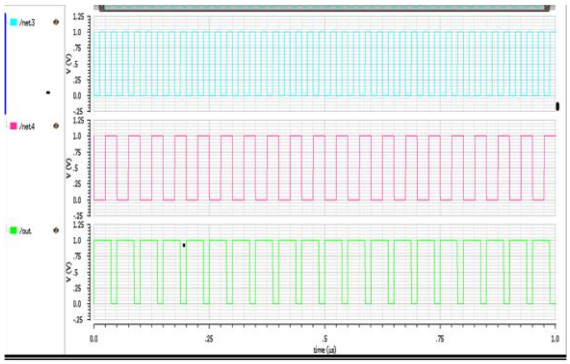

Figure 10: Output Waveform of NAND using CMOS

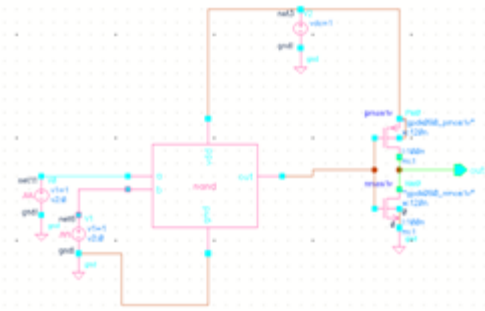

Figure 11: Circuit diagram of AND using CMOS

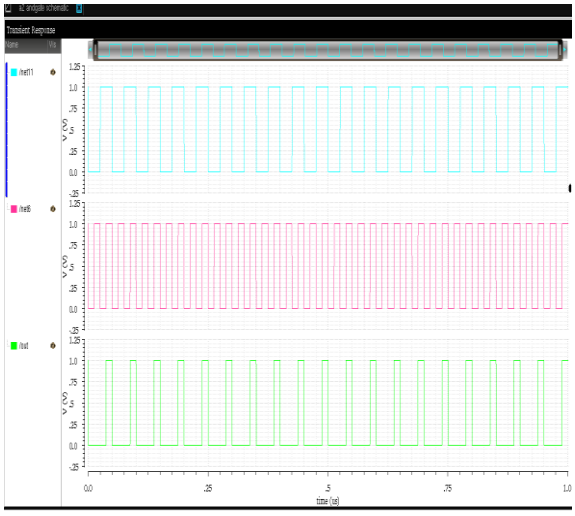

Figure 1 Output Waveform of AND using CMOS

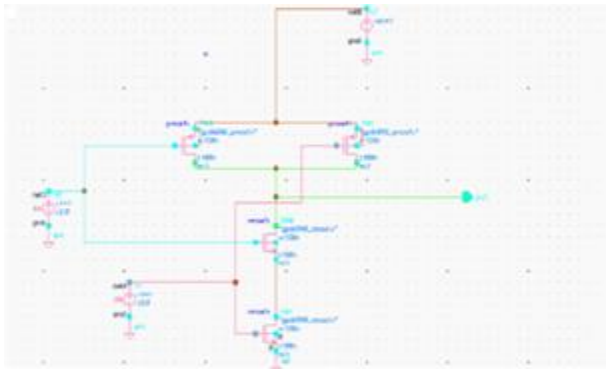

Figure 13: Circuit diagram of NOR using CMOS

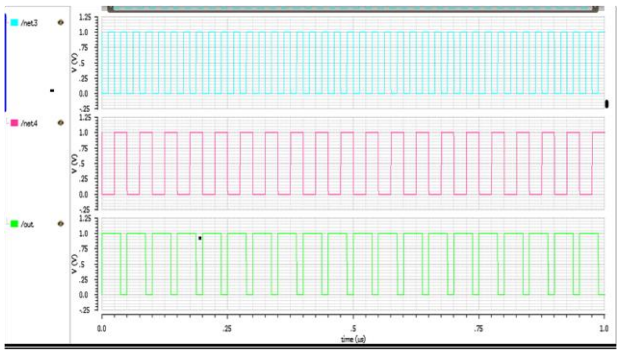

Figure 14: Output Waveform of NOR using CMOS

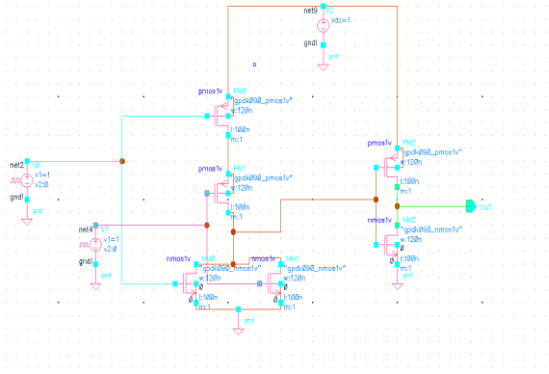

Figure 15: Circuit diagram of OR using CMOS

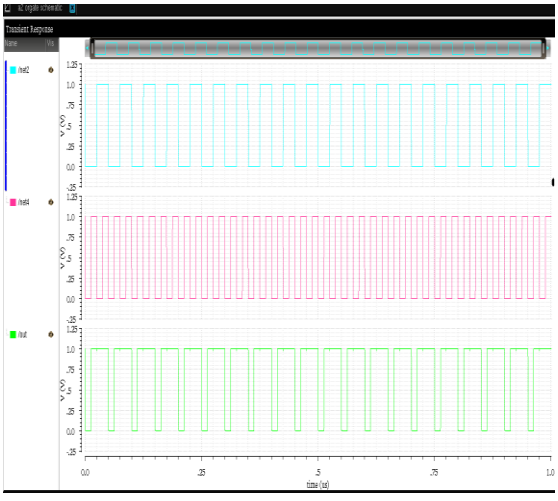

Figure 16: Output waveform of OR using CMOS

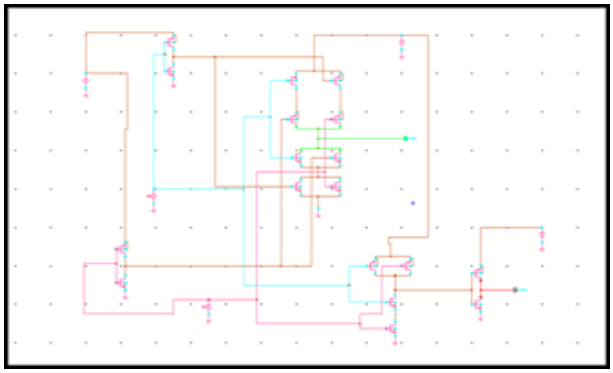

Figure 17: Circuit diagram of HALF ADDER using CMOS

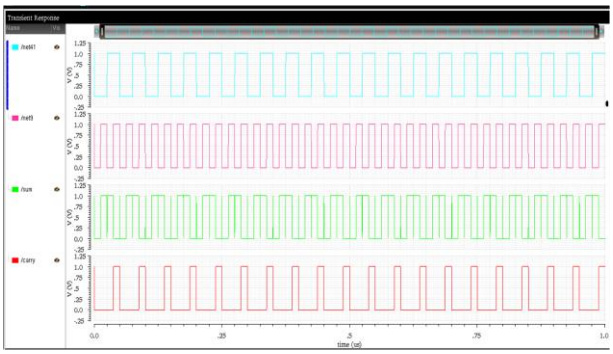

Figure 18: Output Waveform of HALF ADDER using CMOS

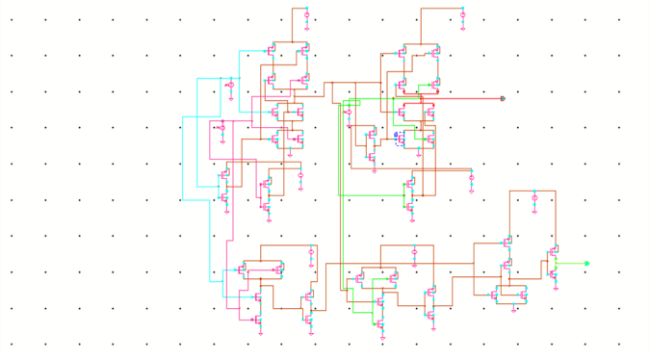

Figure 19: Circuit diagram of FULL ADDER using CMOS

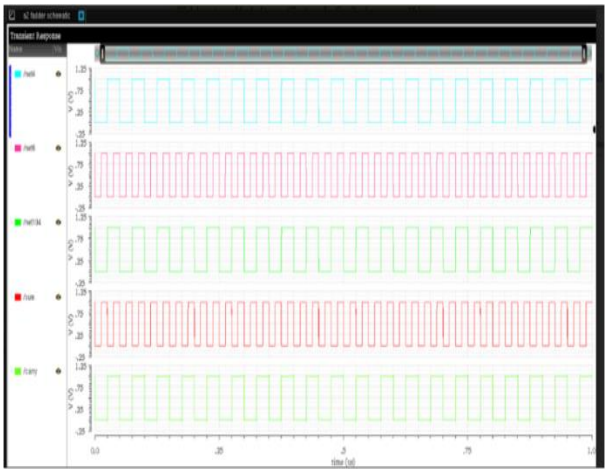

Figure 20: Output Waveform of FULL ADDER using CMOS

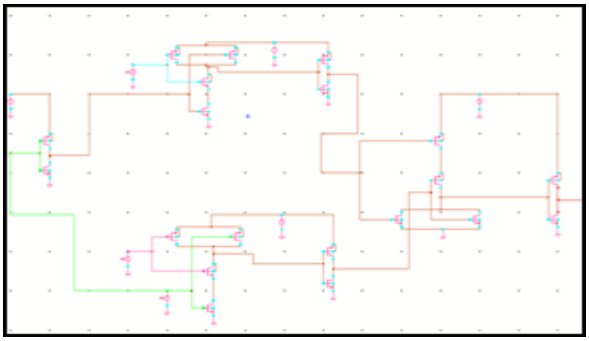

Figure 21: Circuit diagram of 2x1 MUX using CMOS

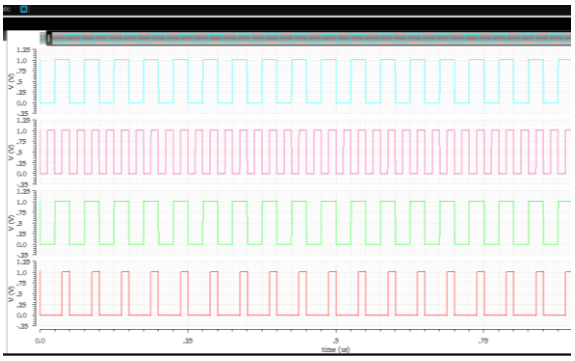

Figure 22: Output Waveform of 4x1 using CMOS

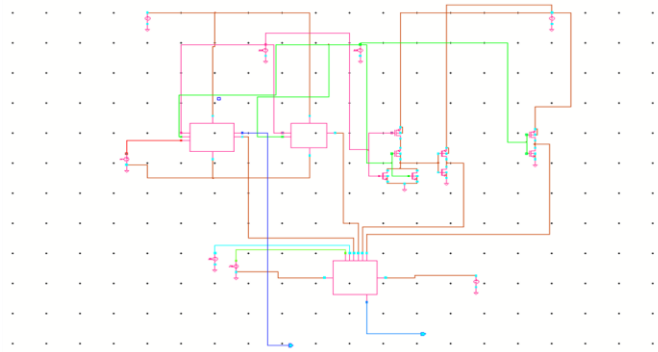

Figure 23: Circuit diagram of ALU using CMOS

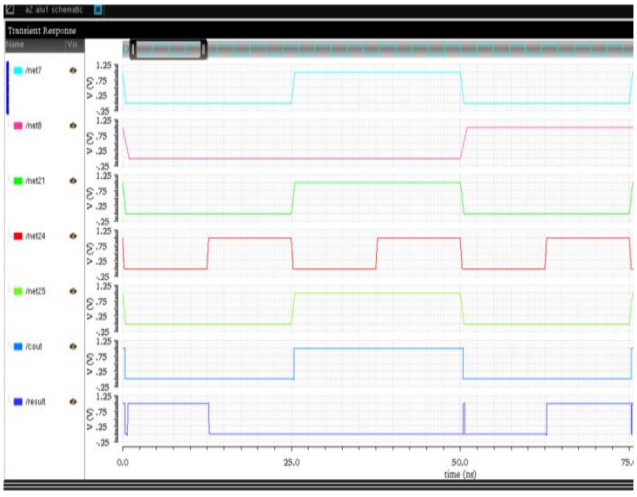

Figure 24: Output Waveform of ALU using CMOS

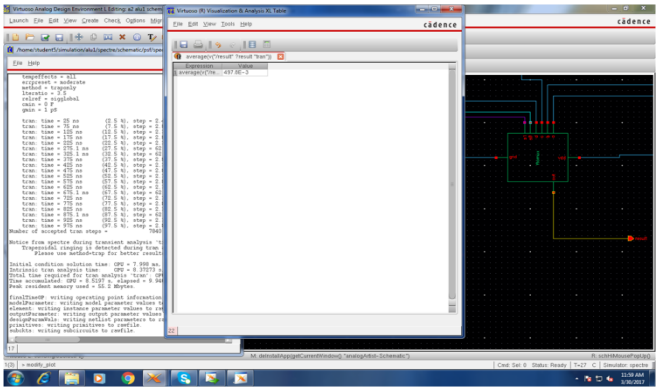

Figure 25: Power calculation of ALU using CMOS

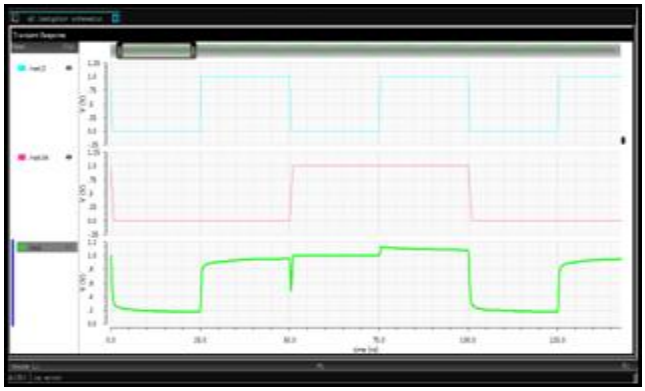

Figure 29: Output waveform of OR using GDI

C. *GDI Implementation:*

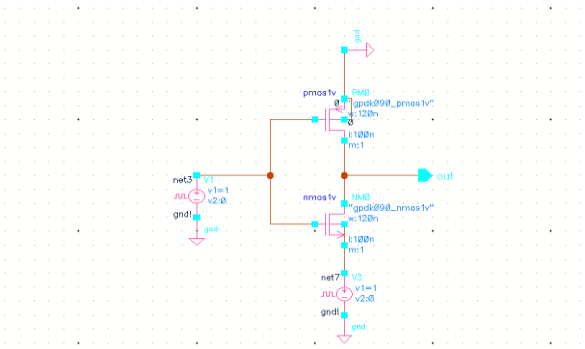

Figure 26: Circuit diagram of AND using GDI

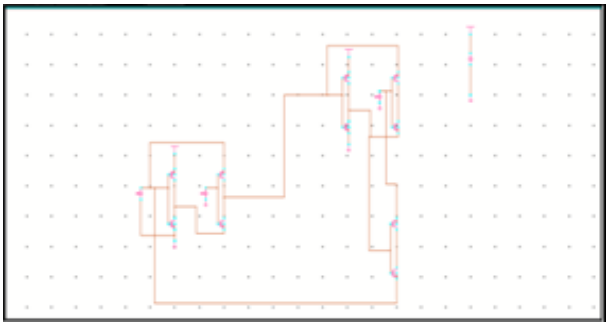

Figure 30: Circuit diagram of full adder using GDI

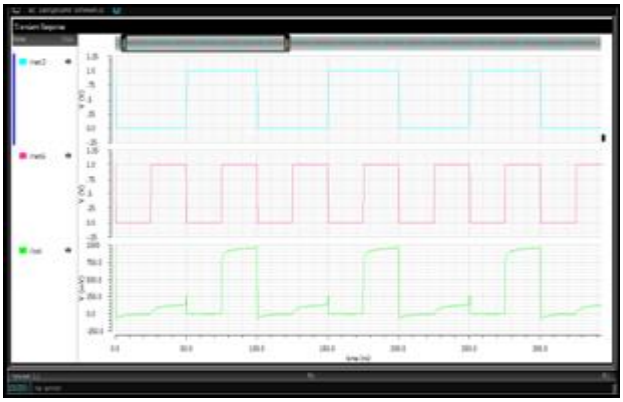

Figure 27: Output waveform of AND using GDI

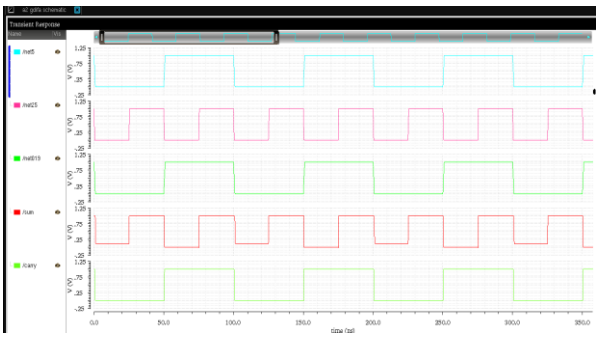

Figure 31: Output waveform of full adder using GDI

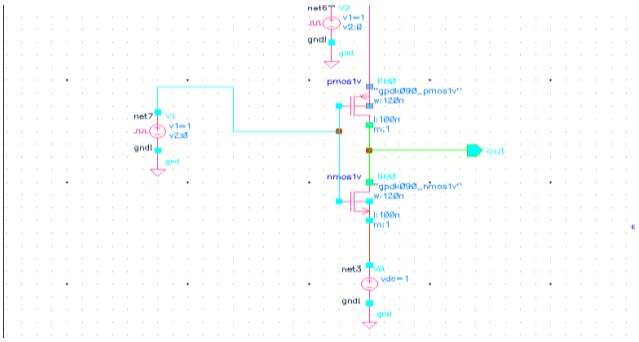

Figure 28: Circuit diagram of OR using GDI

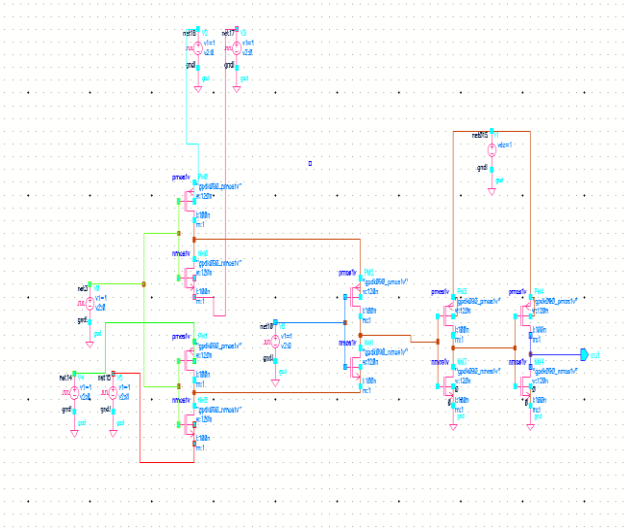

Figure 32: Multiplexer using GDI

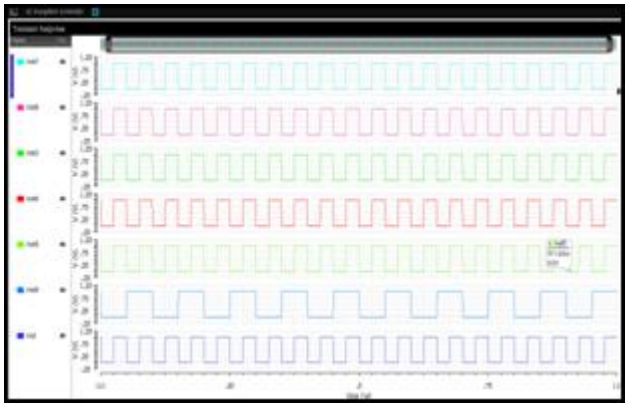

Figure 33: Output waveform of multiplexer

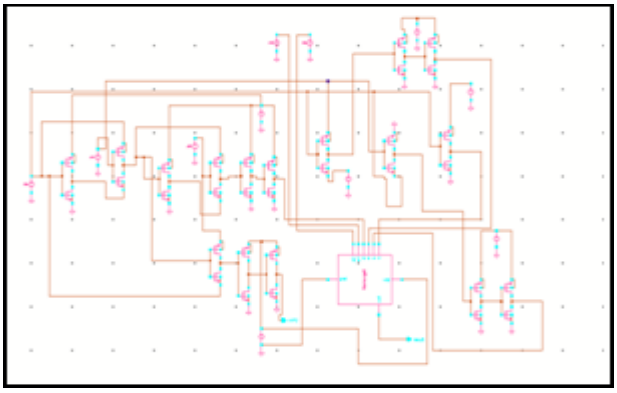

Figure 34: ALU using GDI

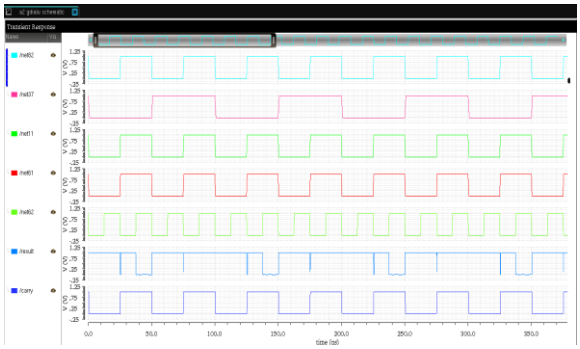

Figure 2Output waveform of ALU using GDI

V. CONCLUSION AND FUTURE SCOPE

Power is a primary design parameter that VLSI engineers need to bother when designing with the integrated circuits. This projected has presented the design methodologies of a compact low power n-bit ALU. We have proposed a design for compact n-bit ALU. I have proved the efficiency of the proposed design with simulation analysis. The required inputs, for the proposed circuit Selection is inputs and input operands. It has also been shown by comparative analysis that the proposed circuit has been constructed with the optimum 'number of gates', 'garbage outputs', 'quantum cost' 'power consumption'. Even though the timing delay of the proposed circuit is not as less as the tree-based designs, considering the optimization of all the parameters, the circuit outperforms the existing ones in terms of scalability and efficiency. Simulations of the proposed circuit have shown that it works correctly.

Since ALU is useful in many applications, like in almost all digital device which involves computations. The ALU can be used in many operations in the areas like microprocessor, communication systems, encryption devices, sorting networks, low power circuits etc. In these applications we can use this ALU efficiently, as it proved better in the power and delay performances than the other circuits.

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