Design of Wideband LNA for RF Receiver

Aniket P. Joshi
Department of Electronics and Telecommunication
RMCET, Ambav (Devrukh)

Abstract-*One of the challenging task and vital thing at the receiver is LNA design because received signal will always be weaker in amplitude and degraded by noise in wireless communications. It should provide low noise figure not only at one frequency but over range of frequencies of interest. Also requirements of minimum noise figure and maximum gain will always be design trade-offs and can't be met simultaneously. An optimization and fine tuning of component values is necessary to get the optimum results. For certain applications like astronomy, it's desirable to have wider bandwidth, low noise figure and good gain. Sometimes we need to sacrifice gain for bandwidth. High electron mobility transistor (HEMT) plays a crucial role and is extensively used in ultra low noise amplifiers. This paper emphasizes in the design of Wideband LNA to achieve desired specifications.*

Keywords-Bandwidth, HEMT, Impedance Matching, LNA, Noise Figure

I. INTRODUCTION

A low noise amplifier (LNA) is a device used in communication systems which amplifies very weak signals captured by the antenna. Almost in any communication system, the LNA is located very close to the receiving antenna; in fact, the first component after the antenna is the low noise amplifier.LNA should boost desired signal power while adding as little noise and distortion as possible [8]. An LNA is the combination of low noise, high gain and stability over the entire range of operating frequency. Impedance and noise matching over wide bandwidth is the most challenging task in wideband LNA design. Wireless communications are very lossy, so signals travelling from far away normally suffer from a lot of degradation. When these signals are received at the antenna, they are very weak, that is why the LNA is used very close to the antenna. Also losses in the feed line become less critical if LNA is located very close to the antenna.

The received signal is typically filtered, amplified by an LNA and translated to the base-band by mixing with a local-oscillator. After being demodulated, the signal is applied to an Analog-to-Digital Converter (ADC) which digitizes the analog signal. The digital signal is then processed in a Digital Signal Processing unit (DSP).

Noise figure is the most important parameter in radio telescope as the sensitivity depends on its value, the smaller it is, the higher is the sensitivity of the telescope [9].

II. TECHNICAL SPECIFICATIONS

Design Specifications:

- Bandwidth – 1 to 2GHz
- Operating frequency range -1 to 3 GHz
- Noise figure - 0.2 to 0.6dB (as it should be as low as possible)
- Gain > 20dB
- Input and output VSWR – Between 1 to 2

III. FLOWCHART

Fig.1 shows generalized flowchart of LNA design.

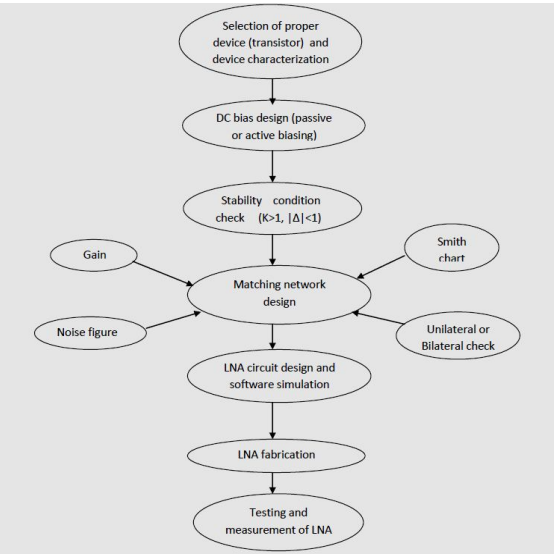

Fig.1 Generalized flowchart of LNA design

IV. DESIGN CONCEPT

First essential step while designing LNA is suitable component (active device) selection. We must keep in mind the trade-offs between various key parameters while designing. S-parameters and noise figure parameters are required to characterize the device [1]-[3]. Key design parameters to be considered for LNA are,

- Desired noise figure (in dB)
- Gain and gain flatness (in dB)

- Operating frequency and Bandwidth (in Hz)
- Input and output reflection coefficients (or VSWR)
- Selection of proper transistor (first important step)
- Amplifier's stability (K>1, |Δ|<1)
- Third order intercept point (TOIP) (in dBm)
- Good sensitivity is desirable
- Good linearity
- Good dynamic range (for astronomy applications).The spurious-free dynamic range refers to the output power range where no third-order products are observed [4].

Based on the amplifier's specifications and application we have to select an appropriate device. We should apply suitable DC bias for proper functioning of the transistor. Input and output matching networks can be designed by either transmission line sections or reactive components or combination of both. Fig.2 illustrates the basic block diagram of LNA [2].

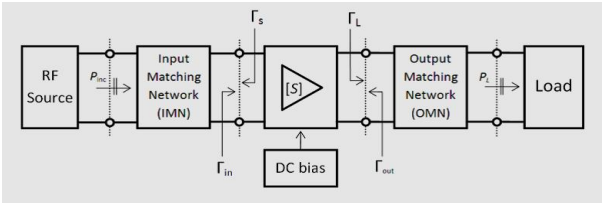

Fig. 2 Generalized block diagram of LNA design

A. Device Selection

Active device selection is the first essential step in LNA design. The designer should carefully review the transistor selection keeping the most important design tradeoffs in mind.Examination of the data sheet is a good starting point in the transistor evaluation for LNA design. We have selected ATF 35143 pHEMT which is a depletion mode device.

B. Stability Check and Enhancement

Stability of the circuit is nothing but it's resistance to oscillations. Stability is an indispensible part of LNA. Unconditional stability is the goal of the designer. It means that for any source and load impedance the circuit should not oscillate. Otherwise proper techniques are applied to make it stable for given frequency range. S-parameters play a significant role in stability analysis.

1) Analytical solution of stability criteria:

Two parameter test (K>1, |Δ|<1) where

$K = [1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2] / [2|S_{12}||S_{21}|]$

and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$

2) Graphical solution of stability criteria:

Single parameter test ($\mu>1$), $\mu_A>\mu_B$, Device A more stable [1]. Smith chart is used to plot input and output stability circles for conditional stability ($|\Gamma_{IN}|>1$ and $|\Gamma_{OUT}|>1$) where

$\Gamma_{IN} = S_{11} + [(S_{12} S_{21}\Gamma_L) / (1 - S_{22}\Gamma_L)]$ and

$\Gamma_{OUT} = S_{22} + [(S_{12} S_{21}\Gamma_S) / (1 - S_{11}\Gamma_s)]$

3) *Stability Enhancement:*

Different techniques are used to enhance the stability. Some of them are:

(a) Adding a series resistance:

A small resistance is added in series or shunt with the drain of the transistor.This will increase the noise figure of the amplifier.It's preferable not to use any noisy component like resistor.

(b) Use of source inductance (inductive degeneration):

Another method of improving stability is to add an inductor to the source leg. A source inductor acts like a noise less resistance. But this reduces gain by a small factor.The additional inductance between the source and ground provides lossless negative series feedback.An added benefit arising from the use of the source inductance is that the input conjugate match, Γ_{11}*, is moved closer to the optimal noise match, Γ_{opt} [7].

C. Biasing of the Device

DC biasing network is required to provide stable operating point for the device.Biasing circuit must be protected from the high frequency effects. For that purpose RFC and blocking capacitors are useful. We have used passive biasing due to it's simplicity and selected V_{DS}=2V, I_D=10mA with negative V_{GS}. So we require dual power supply. Our device is a depletion mode device.

$V_{GS} = V_P(1 - \sqrt{Id/Idss})$

So by controlling V_{GS} we can get control over I_D.

The gate voltage required to set the drain current, I_d, is dependent on the device pinch-off voltage, V_p, and saturated drain current, I_{dss}.

D. Gain Considerations

Gain of the amplifier is the ratio of output power to input power. For LNA design there are three power gain definitions appears in the literature.

- Transducer power gain (G_T)
- Operating power gain (G_P)
- Available power gain (G_A)

Out of these, transducer power gain is the most useful gain definition which accounts for both source and load mismatch.

E. Noise Figure Considerations

The lower the noise figure, the better the LNA as it means less noise is added by the LNA. In telecommunications, noise factor is the measurement of degradation of signal to noise ratio.

Noise figure (F) = 10 log $[(S/N)_{in}/ (S/N)_{out}]$

In generalized form, $F= F_{min}+ (R_n / G_s) |Y_s-Y_{opt}|^2$

For two stagecascade,

$F = F_1 + (F_2-1)/G_{A1}$ or $T_e= T_{e1} + (T_{e2}/G_{A1})$

So First stage N.F. and gain has a large influence on overall N.F. or noise temperature. So the key to low overall N.F. is to focus on first stage by reducing it's noise and increasing it's gain. Later stages have greatly reduced effect on the overall N.F. [1]-[2].

F. Impedance Matching

Input and output matching networkstransition the device to the outside world. Basic objective of matching network is not only to transfer maximum power but also to improve SNR [1].

To have a best compromise between gain and N.F., lossless matching networks (ideally) must be designed to transform the input and output impedance to source and load impedances required in the design specifications. Inter stage matching networks are required in case of cascading. The losses of the matching networks are related to the Q of the components and associated printed circuit board loss.

Input matching network at the input side should give minimum noise matching principle and output matching network is required for maximum gain matching principle and its flatness [5].

That is, $\Gamma_S= \Gamma_{opt}$ to get $F=F_{min}$for simultaneous i/p and noise matching and $\Gamma_L = \Gamma_{out}^*$ or $Z_L= Z_{out}^*$ for output matching.

IV. DESIGN AND SIMULATION

It is found that the selected ATF 35143 is unstable in the desired frequency range. We can verify this in AWR using stability circles. Usually at low frequency, FET is potentially unstable without the addition of Ls and some resistive element. As the source lead inductance is increased, the stability factor increases rapidly. Also we have added extra resistor at the drain side to get unconditional stability throughout the frequency range of interest. Fig. 3 shows unstable regions on the smith chart

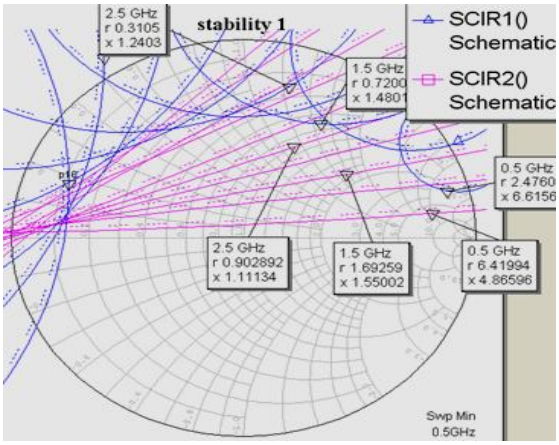

Fig. 3 Stability check for the device in AWR

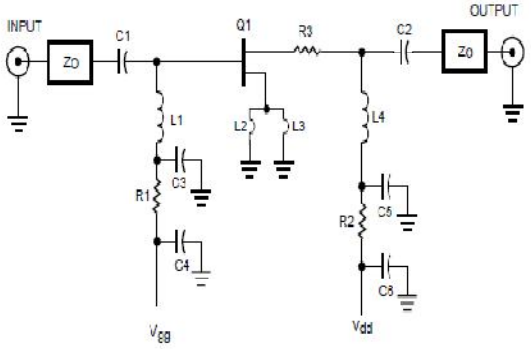

Fig. 4 Circuit diagram for single stage LNA

As shown in Fig.4, the amplifier uses a high-pass impedance matching network for input noise match and output conjugate match. The high pass network consists of a series capacitor and a shunt inductor.The L-section matching networks also double as a means of inserting gate and drain voltages for biasing. Additionally, the series capacitors C1 and C2 also function as DC blocking capacitors.L1 also doubles as a means of inserting gate voltage for biasing up the pHEMT. This requires a good bypass capacitor in the form of C3.

The Q of L1, L4 is also extremely important from the standpoint of circuit loss which directly relates to noise figure. Resistor R3 and capacitors C3, C5 provide in-band stability, while resistors R1 and R2 provide low frequency stability by providing a resistive termination. The resistive loading, R3, is one of the main contributors to stability along with the inductance in the ground path. C4, C6 performs low frequency bypassing. Also extra capacitor may be needed to minimize power supply noise from modulating the DC. Increasing L2, L3 reduces gain and improves input-IP3, but we have to look for microwave oscillation with excessive source inductance [6].

In the similar way we have designed two stage LNA by incorporating inter stage matching network between two transistors.The topology uses two amplifiers and it is an extension of single stage. It gives more gain and stability than single stage. Also we have observed the improvement in the input and output return loss bandwidth due to greater amount of flexibility in tuning for matching networks. Fig.5 and Fig.6 depicts two stage LNA simulated results.

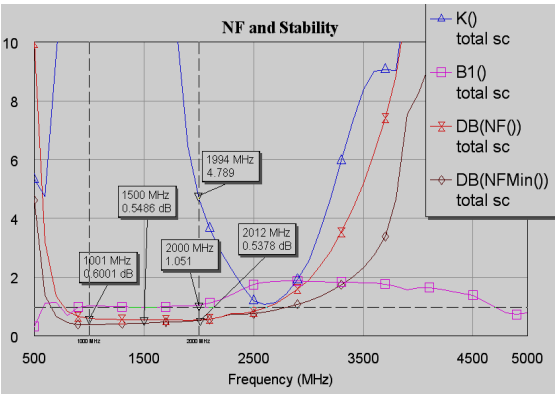

Fig. 5 Stability and noise figure of two stage LNA

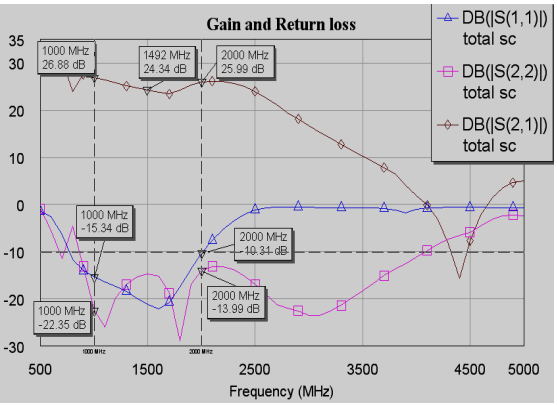

Fig. 6 Gain and return loss of two stage LNA

V. RESULTS FOR TWO STAGE LNA

Following table shows results for important parameters.

Parameter	Two stage LNA
Stability (K and β)	K>1 and β1>0 throughout 500Mhz to 5GHz
Noise Figure (in dB)	0.54 to 0.58 dB from 1 to 2 GHz
Gain (S_{21} in dB)	24 to 27 dB from 800Mhz to 2.5GHz
Return loss (S_{11} and S_{22} in dB)	S_{11}< -10dB from 750MHz to 2 GHz (BW > 1GHz) S_{22}< -10dB from 860MHz to 4 GHz (BW 3GHz)

Table 1: AWR software results for two stage LNA

VI. LAYOUT AND FABRICATION OF LNA

Layout is a critical part of high frequency circuit design and simulation. Layout is the view of the physical representation of a schematic. The first step in fabrication of the LNA is generating the layout from the schematic. For creating a layout of the design, all the wires are removed and the lumped components and devices are connected using the microstrip lines. If there is a node where three circuit paths are being combined, it has been replaced by a MTEE microstrip line. To make a connection between the two components on the circuit path, MLIN microstrip line has been used. To make a layout for any RF circuits the designer needs a real component foot prints. For this task, real components from Coilcraft, TOKO, ATC, Panasonic are chosen.

During the fabrication process, Plating Through Hole (PTH) requirement arises when grounding the source of the device. There is ground on one side of the substrate and circuit lies on the other, in between the two is a dielectric. We have used FR-4 as a commonly used dielectric material having thickness of 0.8 mm. Fig.7 represents layout of two stages along with real component footprints and PTH.

The components used in the circuit are 0603 or 0805 packaged SMD components which are very small having width and length of 1 or 2 mm. To reduce unwanted lead inductance and capacitance, a smaller package size with shorter leads is preferred. This also enables miniaturization of the physical circuit. Soldering such small components on the surface of PCB is very skilled job. In RF circuit even small variation in the width and length can cause significant changes in the results.

For testing purpose, it's desirable to place the PCB inside chassis or metal box in order to avoid external EMI. So mechanical design of chassis considering it's height, width and length is an essential requirement. We have used 4 hole SMA flange connectors for applying input and output power. Vector network analyzer, Noise figure analyzer and noise source is required for testing purpose.

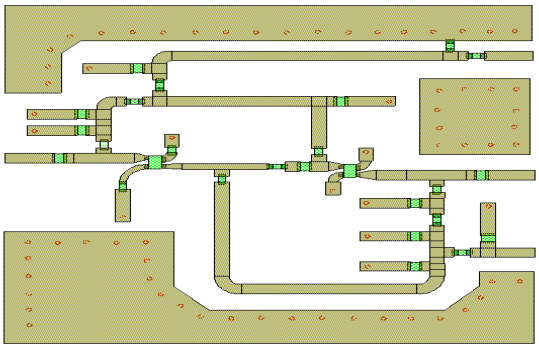

Fig.7 Layout of double stage LNA

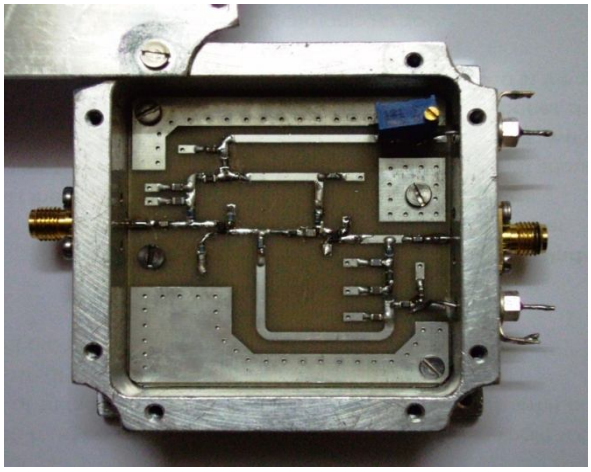

Fig.8 Physical realization of chassis

VII. CONCLUSION

In LNA design, the designer's first goal is to achieve the unconditional stability over the complete range of frequencies along with substantial gain and low noise figure which we have achieved in AWR simulation. Source inductance acts as a series negative feedback which helps to improve input VSWR and low noise by reducing the gain. Extra series resistance at the drain of the transistor is added for unconditional stability. So NF and gain are sacrificed. We have designed two stage LNA at the centre frequency of 1.5 GHz and achieved bandwidth of around 1.2 GHz while maintaining noise figure of 0.54 dB, unconditional stability and gain of 25dB using AWR Microwave Office software.

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