# Implementation of High Speed Low Power Combinational And Sequential Circuits Using Reversible Logi C

**Y.Rajitha[1], E.Rama Krishna[2], Dr.R.Rama Chandra[3]**
[2]HOD & Assistant Professor, Dept of ECE
[3]Principal & Professor
[1, 2, 3] Sri Krishna Devaraya Engineering College,Gooty,A.P

***Abstract-*** *Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realise Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.*

## I. INTRODUCTION

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one. This research paper focuses on implementation of reversible logic circuits in which main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an 8-bit reversible ripple-carry adder is devised and then compared with the conventional 8-bit adder in terms of speed, critical paths, hardware used. Then using the same reversible adder, a Wallace tree multiplier has been implemented, and compared with the conventional Wallace tree multiplier. With the known fact that sequential circuits are the heart of digital designing, the design for the control unit of a reversible GCD processor has been proposed using Reversible logic gates.

## II. REVERSIBLE GATES

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

**Feynman Gate**: Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1

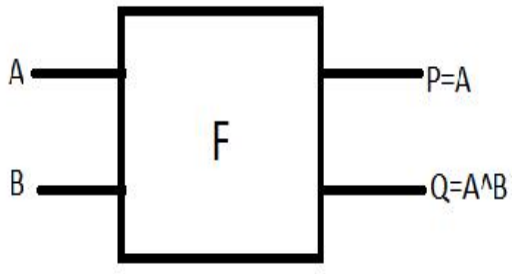



Fig 4.1 Feynman / CNOT Gate

**Fredkin Gate**: It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:

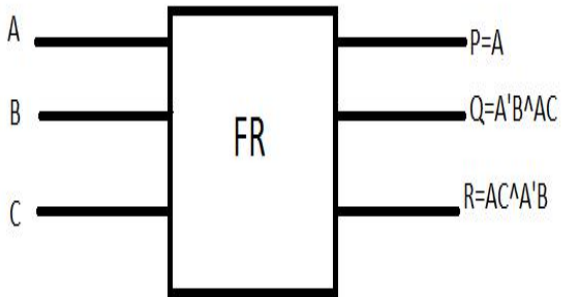



Fig 4.2 Fredkin Gate

**Peres Gate**: It is a basic reversible gate which has 3- inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:

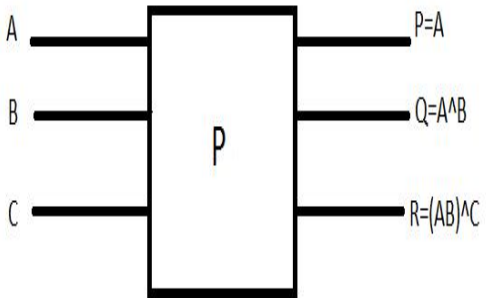



Fig 4.3 Peres Gate

**Toffoli Gate**: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

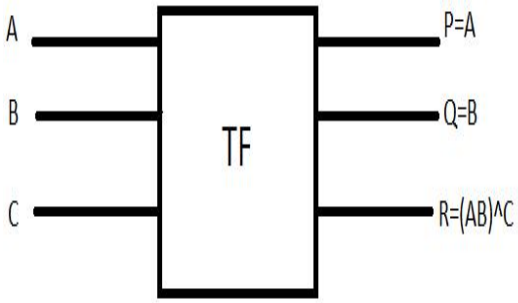



Fig 4.4 Toffoli Gate

**TSG Gate**: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A, Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:

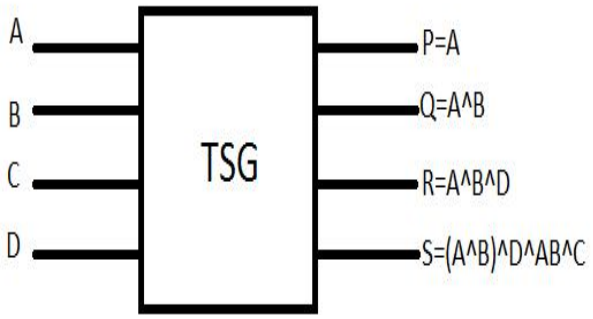



Fig 4.5 TSG Gate

## III. REVERSIBLE 4- BIT FULL ADDER

The gate used in implementing a reversible ripple-carry full adder is the TSG gate [4]. The TSG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths). When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannot start any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.6 and

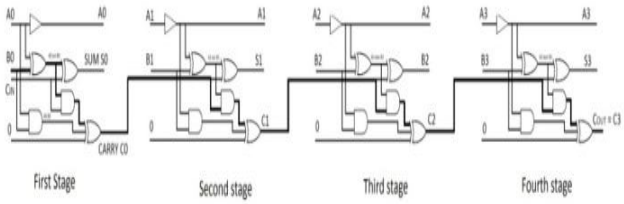



Fig. 4.6: Critical Path of 4-bit reversible adder

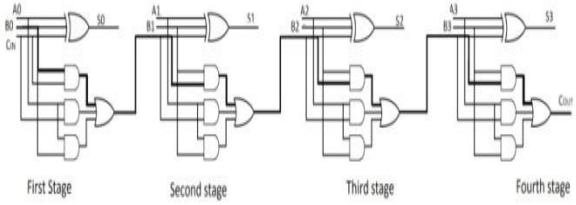



Fig. 4.7: Critical Path of 4 bit irreversible adder

## IV. WALLACE TREE MULTIPLIER

A **Wallace tree** is an efficient hardwired implementation of a digital circuit that multiplies two integers . The Wallace tree has three steps:

1. Every bit of the multiplicand is multiplied (i.e. AND) by every bit of multiplier, thus yielding $n2$ results (for n X n multiplication). Depending on position of the multiplied bits, the wires carry different weights, i.e. weight of bit carrying result of $a5b6$ is 65.
2. The number of partial products is reduced to 2 by layers of full and half adders.
3. The wires are grouped in two numbers, and added using a conventional adder.

The circuit diagram of Wallace tree multiplier using reversible gates is shown in fig. 8:

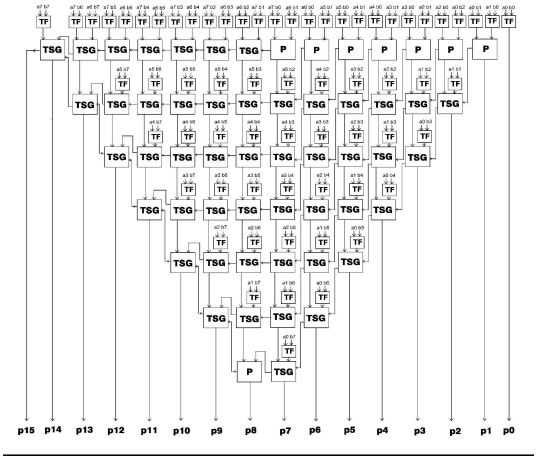


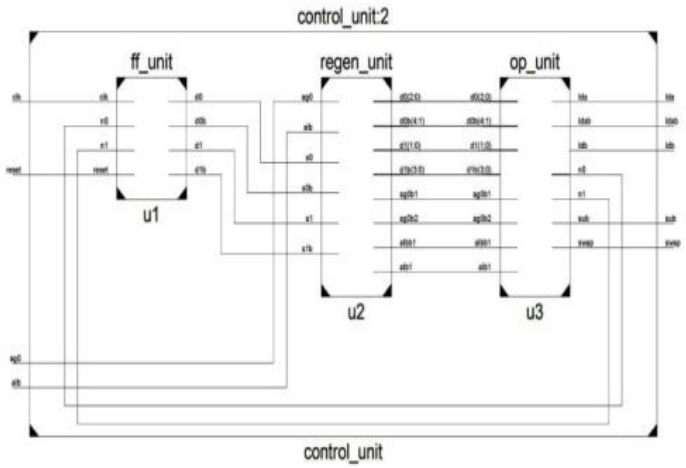

Fig 4.8 Wallace tree multipliers.

## V. DESIGN OF CONTROL UNIT FOR GCD PROCESSOR

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid's Algorithm involving Subtract-Compare-Swap operation of two numbers. The basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another [6].

*A. Control Unit*

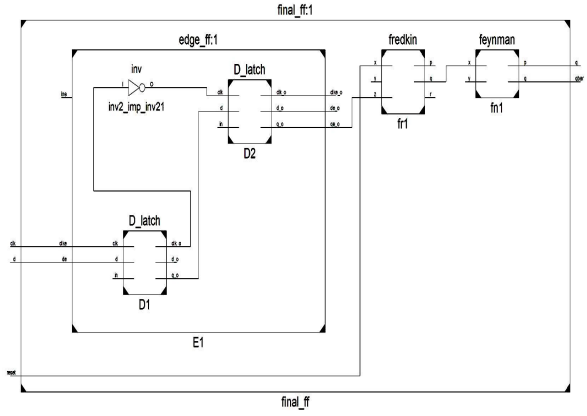
Control unit of GCD processor generates the control signals to manipulate the operations in Data-path.




**Block Diagram Description:**

**1) Flip-flop Module:**

The control unit for GCD processor requires two Flipflops as binary state encoding is used for FSM. In this design reversible edge-triggered D Flip-flop is employed for state transitions .Two D-latches are connected in Master-Slave mode to act as an edge-triggered D Flip-flop. Reversible D-latch is designed using Feynman and Fredkin gates .RTL schematic of reversible D flip-flop obtained is shown in fig. 10:




***Regeneration Module***

To avoid multiple fan-out condition in the design, it is necessary to duplicate signals used for computation of output and next state. The duplication of input signals is achieved using Feynman gates.

***3) Output Module***

The computation of the outputs and Next-state signals is done using reversible Fredkin gates. The functioning of output signals is driven by the algorithm.

## VI. APPLICATIONS OF REVERSIBLE GATES

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

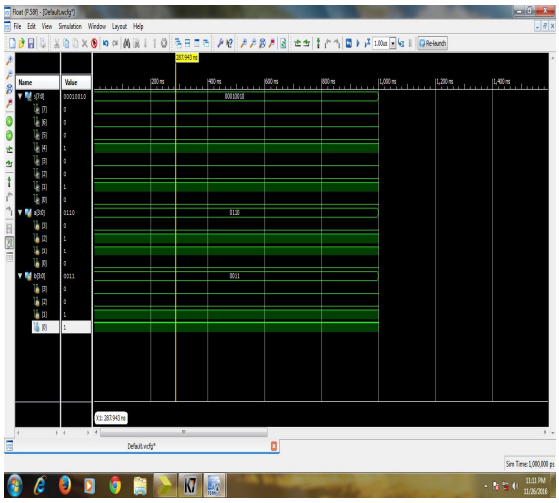
- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.
- The potential application areas of reversible computing include the following
- Nano computing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Implanted Medical Devices
- Wallet “smart cards”
- “ Smart tags” on inventory
- Prominent application of reversible logic lies in quantum computers.
- Quantum gates perform an elementary unitary operation on one, two or more two–state quantum systems called qubits.
- Any unitary operation is reversible and hence quantum networks also.
- Quantum networks effecting elementary arithmetic operations cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).
- Thus, Quantum computers must be built from reversible logical components.

## VII. RESULTS

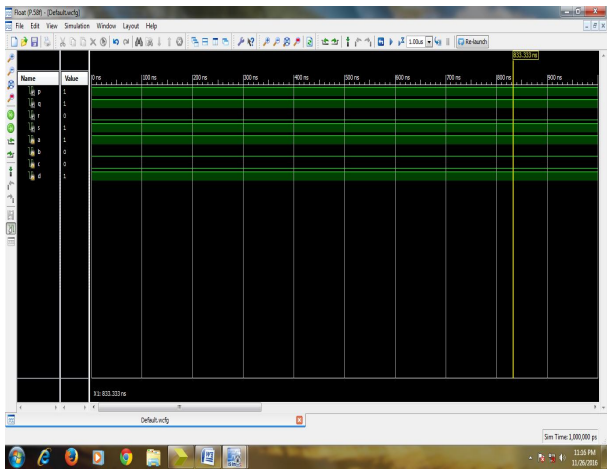
**Simulation Results**

**Multiplier Result:**

**Test bench**:

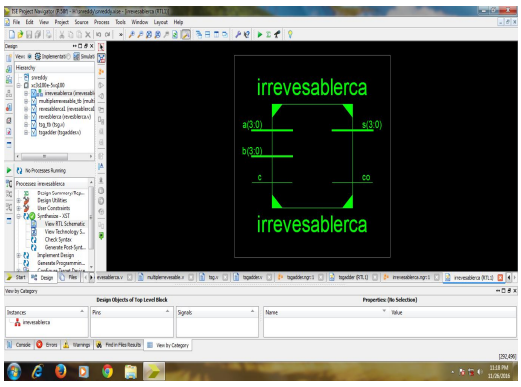


**TSG:**



**Reversible RCA:**

**RTL Schematic**:




## VIII. CONCLUSION AND FUTURE SCOPE

Reversible logic design finds applications in various fields including Quantum computing, Nano-computing, optical computing, Quantum Computing Automata (QCA:

study of mathematical objects called Abstract machines and the computational problems that can be solved using them), ultra- low power VLSI designing, Quantum dot cellular etc. The future of computer chips is limited by Moore's law; hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor capable of ultra-high speed and infinitesimally low power computing.

## REFERENCES


[1] Landauer, Rolf, "Irreversibility and heat generation in the computing process," *IBM Journal of Research and Development* , vol.44, no.1.2, pp.261,269, Jan. 2000 doi: 10.1147/rd.441.0261

[2] Bennett, C.H., "Logical Reversibility of Computation," *IBM Journal of Research and Development* , vol.17, no.6, pp.525,532, Nov. 1973 doi: 10.1147/rd.176.0525

[3] B, Raghu Kanth; B, Murali Krishna; G, Phani Kumar; J, Poornima, "A Comparative Study of Reversible Logic Gates", *International Journal of VLSI & Signal Processing Applications*, vol.2, Issue 1, Feb 2012, (51-55), ISSN 2231-3133 ( Online ).

[4] Morrison, M.; Ranganathan, N., "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," *VLSI (ISVLSI), 2011 IEEE Computer Society Annual Symposium on* , vol., no., pp.126,131, 4-6 July 2011 doi: 10.1109/ISVLSI.2011.30.

[5] Nachtigal, M.; Thapliyal, H.; Ranganathan, N., "Design of a reversible single precision floating point multiplier based on operand decomposition," *Nanotechnology (IEEE-NANO), 2010 10th IEEE Conference on* , vol., no., pp.233,237, 17-20 Aug. 2010 doi: 10.1109/NANO.2010.5697746 (Nachtigal, Thapliyal, & Ranganathan, 2010)

[6] John P. Hayes, "Computer Architecture and Organization", McGraw-Hill, 1998. ISBN 10: 0070273553 / ISBN 13: 9780070273559

[7] Min-Lun Chuang; Chun-Yao Wang, "Synthesis of Reversible Sequential Elements," *Design Automation Conference, 2007. ASPDAC '07. Asia and South Pacific* , vol., no., pp.420,425, 23-26 Jan. 2007 doi: 10.1109/ASPDAC.2007.358022

[8] Yelekar, P.R.; Chiwande, S.S., "Design of sequential circuit using reversible logic," *Advances in Engineering, Science and Management (ICAESM), 2012 Inter.*

[9] R.NareshNaik , P.Siva Nagendra Reddy and K. Madan Mohan "Design of Vedic Multiplier for Digital Signal Processing Applications" in International Journal of Engineering Trends and Technology, volume 4 issue 7-2013 ISSN: 2231-5381(IJETT).

[10] P.Siva Nagendra Reddy et all.."Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates" Indian Journal of Science and Technology, Vol 10(3),DOI:10.17485/ijst/2017/v10i3/109413, January 2017

[11] L. Ranganath, D. J. Kumar and P. S. N. Reddy, "Design of MAC unit in artificial neural network architecture using Verilog HDL," 2016 International Conference on Signal Processing, Communication, Power and Embedded System (SCOPES), Paralakhemundi, 2016, pp. 607-612. doi: 10.1109/SCOPES.2016.7955511