Implementation of OFDM Modulator And Demodulator For FPGA Based Applications

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Abstract- *The new mobile technologies trying to give broadband over wireless channel allowing the user to have bandwidth connectivity even inside moving vehicle. The metropolitan broadband wireless networks require a non-line-of-sight (NLOS) capability, and the scheme Orthogonal Frequency Division Multiplex (OFDM) becomes essential to overcome the effects of multipath fading. Orthogonal Frequency Division Multiplexing (OFDM) has become very popular, allowing high speed wireless communications. OFDM could be considered either a modulation or multiplexing technique and its hierarchy corresponds to the physical and medium access layer. A basic OFDM modulator system consists of a PSK modulator, a serial to parallel, and an IFFT module. The iterative nature of the IFFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. The VHDL implementation allows the design to be extended for either FPGA or ASIC implementation, which suits more for the Software Defined Radio (SDR) design methodology. In this project the OFDM modulator and demodulator will be implemented with full digital techniques. VHDL will be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. The major blocks are Interleaving/Mapping circuit, 8 point IFFT, 8 point FFT, and arithmetic blocks.*

Keywords- NLOS, OFDM, PSK, FFT. IFFT, VHDL, FPGA, RTL.

I. INTRODUCTION

The telecommunications industry faces the problem of providing telephone services to rural areas, where the customer base is small, but the cost of installing a wired phone network is very high. One method of reducing the high infrastructure cost of a wired system is to use a fixed wireless radio network. The problem with this is that for rural and urban areas, large cell sizes are required to obtain sufficient coverage. These results in problems caused by large signal path loss and long delay times in multipath signal propagation. Currently Global System for Mobile telecommunications (GSM) technology is being applied to fixed wireless phone systems in rural areas or Australia. However, GSM uses Time Division Multiple Access (TDMA), which has a high symbol rate leading to problems with multipath causing inter-symbol interference. Several techniques are under consideration for the next generation of digital phone systems, with the aim of improving cell capacity, multipath immunity, and flexibility. These include Code Division Multiple Access (CDMA) and Coded Orthogonal Frequency Division Multiplexing (COFDM). Both these techniques could be applied to providing a fixed wireless system for rural areas. COFDM is currently being used in several new radio broadcast systems including the proposal for high definition digital television, Digital Video Broadcasting (DVB) and Digital Audio Broadcasting (DAB).

However, little research has been done into the use of COFDM as a transmission method for mobile telecom-municateions systems. With CDMA systems, all users transmit in the same frequency band using specialized codes as a basis of channelization. The transmitted information is spread in bandwidth by multiplying it by a wide bandwidth pseudo random sequence. Both the base station and the mobile station know these random codes that are used to modulate the data sent, allowing it to de-scramble the received signal. OFDM/COFDM allows many users to transmit in an allocated band, by subdividing the available bandwidth into many narrow bandwidth carriers. Each user is allocated several carriers in which to transmit their data. The transmission is generated in such a way that the carriers used are orthogonal to one another, thus allowing them to be packed together much closer than standard frequency division multiplexing (FDM). Thisleads to OFDM/COFDM providing a high spectral efficiency. Orthogonal Frequency Division Multiplexing (OFDM) is a multicarrier transmission technique, which divides the available spectrum into many carriers, each one being modulated by a low rate data stream. OFDM is similar to FDMA in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, which are then allocated to users. However, OFDM uses the

spectrum much more efficiently by spacing the channels much closer together.

This is achieved by making all the carriers orthogonal to one another, preventing interference between the closely spaced carriers. Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using Field-Programmable Gate Array (FPGA). This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going to fabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

II. PROPOSED WORK

The block diagram of an OFDM transceiver is shown in Figure 1. The basic component will be discussed in the next few subsections.

1) OFDM Transmitter:

The main components of OFDM transmitter are shown in Figure 1. The randomizer is used as random bit generator. The first three blocks are used for data coding and interleaving. The coded bits will be mapped by the constellation modulator using Gray codification, this way an + jbn values are obtained in the constellation of the modulator. The serial to parallel converter converts the data bits from the serial form to the parallel form. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain. The number of subcarriers determines how many sub-bands the available spectrum is split into [11, 12]. The Cyclic Prefix (CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system [16].

2) OFDM Receiver:

The main blocks of OFDM receiver are observed in Figure 1 [9]. The received signal goes through the cyclic prefix removal and a serial-to-parallel converter [11]. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware [14]. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [13-15]

III. SIMULATION AND RESULTS

In this Section the result and analysis of the each and every block of baseband of transmitter is explained ,showing the RTL view of the building blocks and simulation results.

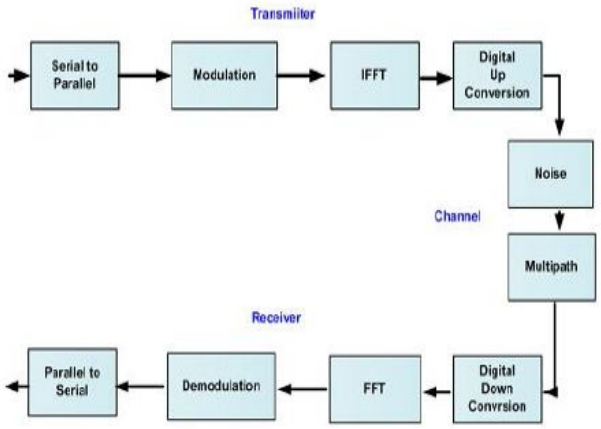

Figure 1: Basic Block Diagram of OFDM Modem.

Simulations Results:

Following are the simulation results observed during the experimental set up of the system. The following three are the simulational results of the prime building blocks of the OFDM systems

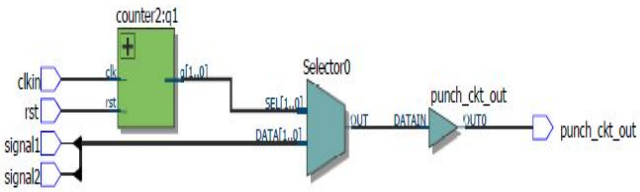

Figure 2: The RTL of Puncher Block

The simulation results of the puncturer are shown below in figure number 2, consisting two bit streams as input and providing only one punctured bit stream as output,which clearly shows that the bit rate is increased , it is shown below

Following is the simulation of the serial to parallel convertor which shows that the serially input data coming from the previous blocks become paralleled .The parallel attribute of the bits arrangement is the main requirement of the OFDM transmission . The simulation results shows the conversion from serial to parallel and RTL view of FFT Design in following figure 3.

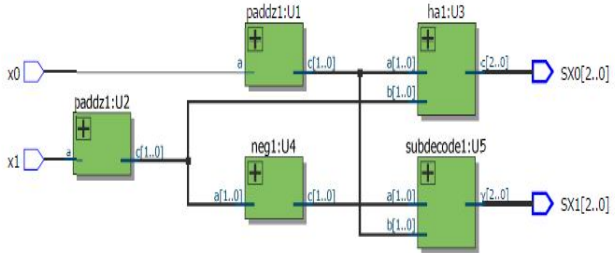

Figure 3: RTL view of FFT Design

After IFFT block the complete baseband simulation will be observed which clearly indicates the multiple ouputs , hence showing digitally the multiple bands of the system. The complete baseband simulation observed after the last block of the OFDM baseband system is shown in figure 6.

OFDM Partition Summary
No partition information was found.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	1,721	4,704	36%	
Number of 4 input LUTs	1,908	4,704	40%	
Logic Distribution				
Number of occupied Slices	1,422	2,352	60%	
Number of Slices containing only related logic	1,422	1,422	100%	
Number of Slices containing unrelated logic	0	1,422	0%	
Total Number of 4 input LUTs	2,457	4,704	52%	
Number used as logic	1,908			
Number used as a route-thru	111			
Number used for Dual Port RAMs	424			
Number used as Shift registers	14			
Number of bonded IOBs	2	140	1%	
IOB Flip Flops	1			
Number of Block RAMs	3	14	21%	
Number of GCLKs	2	4	50%	
Number of GCLKIOBs	2	4	50%	
Total equivalent gate count for design	111,140			
Additional JTAG gate count for IOBs	192			

Figure 4: The Xilinx ISE Summary of Design

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		13
Vccint 2.50V:	3	7
Vcco33 3.30V:	2	7
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 2.50V:	3	7
Quiescent Vcco33 3.30V:	2	7

Figure 5: Power Synthesis Report

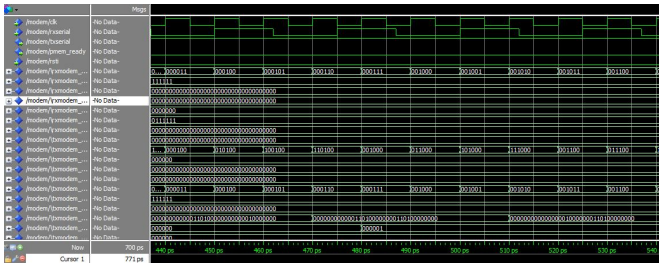

Figure 6: Final Simulation

IV. RESULT COMPARISONS

In Experimental analysis Simulation is carried out using Xilinx ISE software, There are many secure high speed communication systems are available ,but even less are done inside a FPGA. some of the version of the OFDM applications are implemented inside a Spartan II FPGA . MB-OFDM module design using VHDL language and simulations have been done using Xilinx ISE simulation tool to check the functionality of each submodules of MB-OFDM . The serial to parallel Simulation results give output which has a particular importance in OFDM concept. The IFFT simulations at the last shows the multi-banding approach.

Table 1: Comparative Analysis of Proposed and Previous Design

	Ref [5]	Ref [6]	This Work
System Specification	MIMO-OFDM	MIMO-OFDM	MIMO-OFDM
Function	Transceiver	Transceiver	Transceiver
Technology(CMOS)	0.13nm P18M	65nm 1P6M	0.13nm P18M
Gate Count	2.58M	1.87M	1.2M
Supply Voltage (core / I/O)	1.2V / 3.3V	1.2V / 3.3V	1.2V / 3.3V
Power	62.8mW	33.7mW	13mW
Frequency	62.4MHz	62.4MHz	82.4MHz

V. CONCLUSION

In this paper, OFDM MODEM has been studied and implemented for Modulator and Demodulator and Its applications have been extended from high frequency radio communications to telephone networks, digital audio broadcasting and terrestrial broadcasting of digital television. The advantages of OFDM, especially in the multipath propagation, interference and fading environment, make the technology a promising alternative in digital communications including mobile multimedia. Therefore this design can be applied to real-time signal processing system, which completes the main computing modules in the OFDM for multi services. The capability of designing and implementing an OFDM MODEM is presented in this work,the design considered using a pure VHDL with the aid of IPs to implement the IFFT and clock Synthesis Function from the Mapping results the design can be easily fit into Xilinx

REFERENCES

[1] Sheng Zhou, Xiaochun Wang, Jianjun Ji, Yanqun Wang, "Design and Implementation of a 1024-point High-speed FFT Processor Based on the FPGA", 6th international congress on image and signal processing 2013 IEEE.

[2] K.Sowjanya, Leele Kumari, "Design and Performance Analysis of 32 and 64 Point FFT using Radix-2 Algorithm",Proceedings of AECE-IRAJ International Conference, 14th July 2013.

[3] K. Umapathy, Dr. D. Rajaveerappa, "Implementation Of Optimized 128- Point Pipeline Fft Processor Using Mixed Radix 4-2 For OFDM Applications", International Journal of Engineering Science and Technology (IJEST) Vol. 4 No.12 December 2012.

[4] M.Merlyn, ECE,Jayaram College of Engg and Tech, Trichy, India "FPGA Implementation Of FFT Processor With OFDM Transceiver", 2010 International Conference on Signal and Image Processing page (485-489) @ 2010 IEEE.

[5] R. Sai Brunda, M.V.R. Vittal,"Design and Implementation of Variable Length FFT Processor for OFDMA System Using FPGA", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 2, page (1250-1255), March –April 2013.

[6] Paul H. MQose, Member IEEE, "A Technique for Orthogonal Frequency Division Multiplexing Frequency Offset Correction", IEEE TRANSACTIONS ON COMMUNICWIONS, Vol. NO. 2, page (1-7), OCTOBER 2004.

[7] Lokesh C, Dr. Nataraj K. R, "Implementation of an OFDM FFT Kernel for WiMAX", International Journal of Computational Engineering Research (ijceronline.com) Vol. 2 Issue. 8, pp -74-80.

[8] Deepak Revanna, Omer Anjum, Manuele Cucchi, Roberto Airoldi, Jari Nurmi, "A Scalable FFT Processor Architecture for OFDM Based Communication Systems",978-1-4799-0103-6/13/$31.00 2013 IEEE.

[9] Mounir Arioua, Said Belkouch, Mohamed Agdad, Moha Marabet Hassani, "VHDL Implementation of an Optimized 8-point FFT/IFFT processor in Pipeline Architecture for OFDM systems", 978-1-61284-732-0/11/$26.00 2010IEEE.

[10] N Kirubanandasarathy , Dr.K.Karthikeyan and K.T hirunadanasikamani, "VLSI Design of Mixed radix FFT Processor for MIMO OFDM in wireless Communications", 978-1-4244-7770-8/10/$26.00 2010, IEEE.

[11] C.Shashikanth, B.Kedarnath, "Implementation of Virtex-5 Based 1024- Point Fast Fourier Transform (FFT) Computational Module for Wireless Communications", IJSR INTERNATIONAL JOURNAL OF SCIENTIFIC RESEARCH, page -60-62, 2010.

[12] Kai-Jiun Yang, Shang-Ho Tsai, Senior Member, IEEE, and Gene C. H. Chuang, "MDC FFT/IFFT Processor with Variable Length for MIMOOFDM Systems", IEEE Transactions on very large scale integration (vlsi) systems, Vol. 21, No. 4, pp-720-731, April 2013.

[13] K.Harikrishna, T. Rama Rao , Vladimir A. Labay, "FPGA Implementation of FFT Algorithm for IEEE 802.16e (Mobile WiMAX)", International Journal of Computer Theory and Engineering, Vol. 3, No. 2, pp- 197-202, April 2011.

[14] Chandrakanth.V, Wasim Nasir, Paramananda Jena and Ramachandra Kuloor, "Novel Architecture for Hardware Efficient FPGA Implementation of Real Time Configurable Variable Point FFT Using NIOS II", 978-1-4244-2871-7/09, IEEE, 2009.