Based On Computer Power Supply A Power Quality Improved Bridgeless Converter

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Abstract- *Poor power quality, slow dynamic response, high device stress, harmonic rich, periodically dense, peaky, distorted input current are the major problems which are frequently encountered in conventional switched mode power supplies (SMPSs) used in computers. To mitigate these problems, it is proposed here to use a non-isolated bridgeless buck-boost single ended primary inductance converter (SEPIC) in discontinuous conduction mode (DCM) at the front end of an SMPS. The bridgeless SEPIC at the front end provides stiffly regulated output dc voltage even under frequent input voltage and load variations. The output of the front end converter is connected to a half bridge dc-dc converter for isolation and also for obtaining different dc voltage levels at the load end that are needed in a personal computer. Controlling a single output voltage is able to regulate all the other dc output voltages as well. The design and simulation of the proposed power supply are carried out for obtaining an improved power quality which is verified through the experimental results.*

Keywords- Bridgeless converter; PFC; input current; computer power supply; power quailty

I. INTRODUCTION

Many electronic appliances powered up from the utility, utilize the classical method of ac-dc rectification which involves a diode bridge rectifier (DBR) followed by a large electrolytic capacitor. The uncontrolled charging and discharging of this capacitor instigates harmonic rich current being drawn from the utility which goes against the international power quality standard limits . Modern ac-dc converters incorporate power factor correction (PFC) and harmonic current reduction at the point of common coupling (PCC) which improves voltage regulation and efficiency at the load end. Personal computer (PC) is one of the electronic equipment which is severely affected by power quality problems. Single stage and two stage conversions of ac voltage into dc voltage have been used in computers to maintain harmonic contents within limits and also to obtain stiffly regulated multiple outputs. Single stage power conversion is simple, compact and cost-effective. However, it suffers from poor dynamic response, control complexity, high capacitance value and high component stress. So, two stage conversion of ac voltage into multiple dc voltages is mostly preferred in computers . The component count in a two stage power supply is much higher than its single stage counterpart. But, it provides better output voltage regulation, fast dynamic response and blocks the second harmonic (100Hz or 120Hz) component in the first stage itself so that large capacitors at the output side are avoided.

Various front end converters have been employed in the power supplies for providing PFC and output voltage regulation. A boost converter is the common choice for providing PFC in power supplies. However, it is not the preferred choice in computer power supplies due to its requirement for a large input voltage range The output voltage of a boost converter cannot be controlled to a value less than 300V for a 220V ac input. So, a buck-boost converter is preferred in PCs where wide variations in input voltages and load are expected . Low output voltage ripple is preferred in a computer power supply as it is connected to various ICs. Single stage power supplies are used in many applications where power quality improvement and voltage regulation take place in a single stage. However, in computers, single stage configuration increases the stress across the switches and slows the voltage regulation under varying loads . Hence, two stage PFC ac-dc converters based SMPSs are being employed to improve the input power quality and also to obtain an acceptable output voltage regulation. But, the efficiency of a two stage SMPS is lower than the conventional SMPS . To eliminate this disadvantage, a new bridgeless front end converter is proposed in this paper for computer power supplies [14-17] which offers low switching ripple, sinusoidal input current and good dynamic response as compared to other non-isolated buck-boost converters. The elimination of DBR at the front end results in reduced conduction losses and supports a larger output voltage range with enhanced efficiency. At the output of the front end converter, a half bridge converter is used which provides isolation, regulation and multiple dc outputs with a better core utilization.

It is observed from the available literature that the power quality improvement in SMPSs using bridgeless PFC converter has not been attempted by many researchers so far. In this work, a bridgeless single ended primary inductance converter (SEPIC) operating in discontinuous conduction

mode (DCM) is being used at the front end of the SMPS which offers excellent PFC at the rated as well as light load condition. Upper converter operates in the positive half cycle of the ac voltage while the lower converter operates in the negative half cycle. The output of the bridgeless PFC converter is connected to the isolated converter. Test results of the proposed multiple-output SMPS are found in line with the simulated performance demonstrating its improved power quality and output voltage regulation.

II. SMPS CONFIGURATION AND OPERATING PRINCIPLE

The proposed computer power supply consists of mainly two parts, bridgeless front end ac-dc converter and multi-output isolated dc-dc converter. The operating mode out of CCM (Continuous Conduction Mode) or DCM of the bridgeless front end converter may be selected on the requirement of the user. A DCM is selected if the cost is a major consideration; if not, CCM is adopted that reduces device stresses, despite the fact that two voltage and one current sensor are required which makes it costlier. Therefore, a DCM operation of the front end PFC converter is preferred in PCs where only one voltage sensor is needed for sensing and control. Here, the front end converter is designed in DCM for achieving inherent PFC which requires only one voltage sensor while the isolated converter is designed in CCM.

The control loops of both converters are independent of each other. The system configuration and operating principle of SMPS system has been described in following subsections.

A. System Configuration

The configuration of proposed power supply with four regulated dc output voltages is shown in Fig.1. At the input side, DBR is eliminated by using two SEPICs. The upper converter operates in the positive half cycle and the lower one operate in the negative half cycle of the input ac voltage. The switching frequency of both the converters is set at 20 kHz for efficient control. The design of output inductors for both the converters is carried out in DCM to reduce the complexity in control. The regulation of the output voltage is able to take care of wide variations in the input voltage and the load. The output dc voltage (V_{PFC}) is sensed and compared with a reference voltage ((V_{PFCref}) from which the voltage error is obtained (V_{ePFC}= V_{PFCref}-V_{PFC}) which is given to a proportional and integral (PI) controller. The PI controller output (V_{cc1}) is compared with a high frequency saw-tooth 1 wave to yield PWM pulses that are given to both switches simultaneously. If S_t<V_{cc1} and V_{ac} is positive, then S_p is on, else S_p remains off. S_t represents the switching signals for the bridgeless ac-dc converter. The width of these PWM pulses varies according to the output of the PI voltage controller-1 so that the output dc voltage V_{PFC} is regulated effectively which is, in turn, fed to the isolated half bridge converter in the second stage to obtain multiple isolated regulated output voltages. Hence, the width of PWM pulses changes accordingly to maintain dc output voltage V_{PFC} constant. The isolation is effected through multi-winding high frequency transformer (HFT). A centre tapped configuration is chosen at the output side to reduce the conduction losses. All the secondary windings are controlled via one control loop. The highest rated secondary winding of the HFT is selected for voltage sensing. The difference between the output voltage (V_{o1}) and reference voltage (V_{o1ref}) is fed to another PI voltage controller-2 which output is compared with another high frequency saw-tooth wave 2 to generate second set of PWM signals for the half-bridge converter devices S_1 and S_2. Care should be taken to make sure that there is sufficient dead-time between turning OFF of S_1 and turn-ON of S_2 to avoid shoot-through fault. The isolated converter is operated in CCM to take the advantage of reduced stress. If the load in any of the winding changes, the duty cycle changes accordingly to ensure regulated dc voltage outputs. The response of the other outputs is slower than the one where the output voltage is sensed.

B. Operating Principle

The operation of the front end converters and the isolated converter are described independently as follows:

1) Operating principle of front end converter

During the positive half cycle of the input voltage, the upper SEPIC operates as shown in Fig. 2. In the same way, during negative half cycle the lower SEPIC would operate. The operation of the SEPIC in one PWM cycle is described with the help of the following modes: In the first mode, the high frequency switch S_p turns on, the input inductor L_{p1} starts storing the energy which is transferred from the single phase ac mains as shown in Fig. 3a. Diode D_{p1} completes the current path. In the second mode, S_p is turned off and diode D_{p2} starts conducting. The energy in output inductor L_{p2} starts decreasing to zero which is shown in Fig. 3b. In the last switching state, the current in the output inductor remains zero until the start of next switching cycle. This mode ensures the DCM operation as shown in Fig. 3c

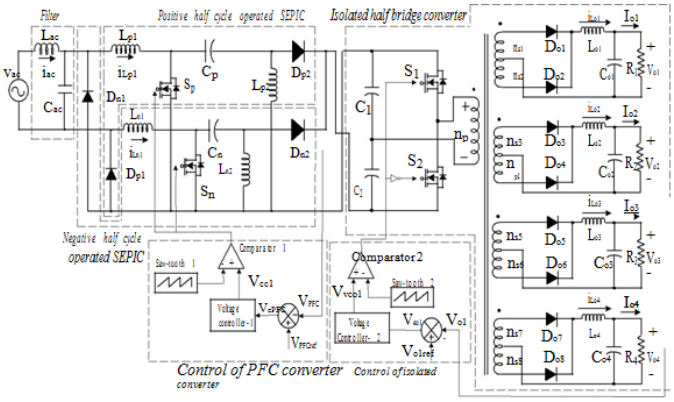


Fig.1 Schematic diagram of the PFC converter based SMPS

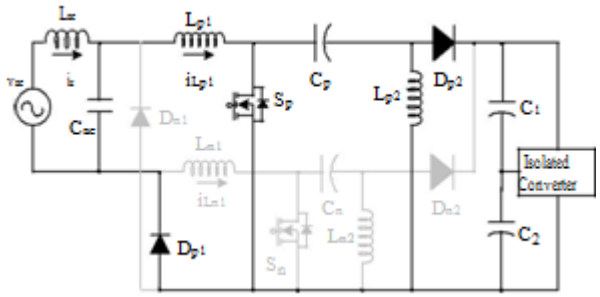


Fig. 2 Operation of PFC converter when the input voltage is positive

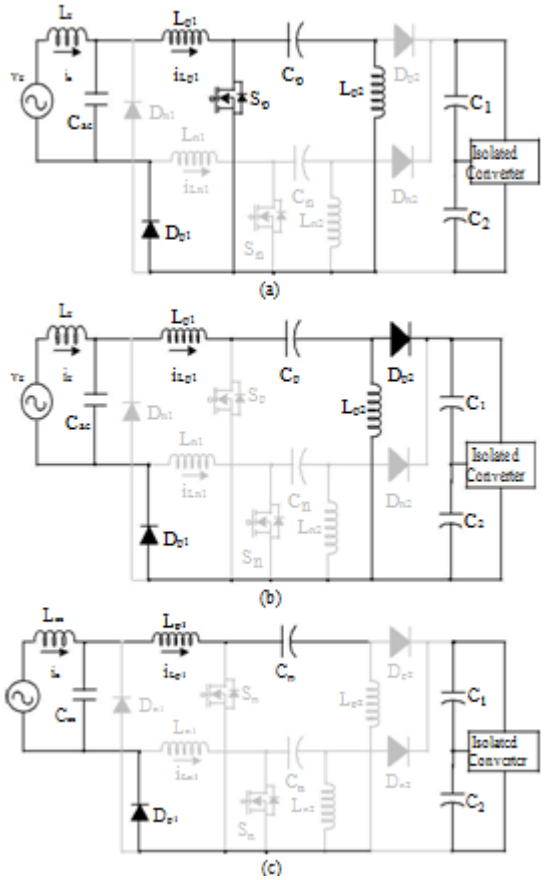


Fig. 3 Operating modes of bridgeless PFC converter when the input voltage is positive

2) Operating principle of isolated converter

Two high frequency switches are turned on and off alternately in one switching cycle. So, the operation of the converter in one half of the switching cycle is the same as that of the other half cycle. In the first half cycle, the upper switch S_1 is turned on. The diodes on the secondary side (D_{o1}, D_{o3}, D_{o5} and D_{o7}) start conducting and the inductors (L_{o1}-L_{o4}) in all the secondary windings start storing energy. When the inductor current reaches its maximum value, upper switch S_1 is turned off. All the filter capacitors discharge through the loads to maintain dc output voltages as constant. In the next half cycle of the PWM period, the upper switch is turned off. The secondary diodes (D_{o1}-D_{o8}) are turned on to free-wheel the inductors currents. The current in all secondary windings cancel core flux so that net voltage across HFT becomes zero. The same inductor charging and discharging take place in next half switching cycle with the lower switch S_2.

III. DESIGN OF PROPOSED BRIDGELESS CONVERTER BASED SMPS SYSTEM

The design of proposed bridgeless converter based SMPS is described in the following section.

A. Design of Proposed SMPS System

The design for the positive half cycle operated PFC converter is carried out here. The negative half cycle operated converter is designed in the same way. The average voltage V_{acav} is calculated as,

$$V_{acav} = \frac{\sqrt{2}V_{ac}}{\pi} = \frac{2\sqrt{2} \times 220V}{3.14} = 198V \quad (1)$$

The duty cycle D of the PFC buck-boost converter is expressed as the ratio of its output dc voltage to the sum of output dc voltage and input voltage.

$$D = \frac{V_{pfc}}{V_{pfc}+V_{acav}} = \frac{300V}{300V+198V} = 0.6 \quad (2)$$

Irrespective of variation in the input voltage from 170V to 270V, the output voltage is maintained constant at 300V. Hence, the duty cycles for supply voltages of 170V voltage, 220V and 270V are calculated as, D_{170V}=0.66, D_{220V}=0.6, D_{270V}=0.552 respectively. The duty cycle D of the PFC converter is taken less than D_{220V} for an efficient control during DCM operation. Therefore, it is considered as 0.25 for the design of the PFC converter.

The input inductor value is calculated for the permitted ripple of 40% of input current.

$$L_{in1} = \frac{DV_{min}}{f \times (i_{ripple})} = \frac{0.25 \times 198V}{20\,kHz \times 0.58\,A} = 4.35mH \quad (3)$$

where, f is the switching frequency of the PFC converter. The critical conduction parameter is given as [21],

$$K_a < \frac{1}{\left(\frac{V}{\sqrt{2}V_{ac}}\right)^2} = \frac{1}{\left(\frac{300V}{311V}\right)^2} = 0.129 \quad (4)$$

where, n is taken as 1 for the non-isolated PFC converter. To operate the PFC converter in DCM, the conduction parameter should be taken less than K_a for efficient control. Hence, it is selected as 0.08.

The equivalent value of inductance of the PFC converter is given as,

$$L_{eq} = \frac{K_a R_o}{2f} = \frac{281.2\Omega \times 0.08}{2 \times 20kHz} = 225\mu H \quad (5)$$

Therefore, the output inductor value is calculated as,

$$L_{in2} = \frac{L_{in1} L_{eq}}{L_{in1} - L_{eq}} = \frac{4.31mH \times 225\mu H}{4.31mH - 225\mu H} = 237\mu H \quad (6)$$

The selected value of output inductor is 100 µH to ensure DCM condition in all operating conditions of input voltages, load and unity PF operation at a low input voltage.

The intermediate capacitor value is estimated as,

$$C_a = \frac{1}{\omega_r (L_{in1} + L_{in2})} = \frac{1}{2 \times \pi \times 2000\ Hz\ (4.3mH + 0.1mH)} = 0.18\mu F \quad (7)$$

where, ωr is the angular frequency (ωr=2πfr). A fr is considered as 2000Hz (f>fr>fL). A capacitor value of 0.22µF is selected for the hardware implementation.

An L-C filter is used at the input side to mitigate higher order harmonics [22]. The maximum value of the capacitor is as,

$$C_{ac} = \frac{I_p \tan\theta}{\omega V_p} = \frac{2.25A \times 0.017}{314 \times 311V} = 391nF \quad (8)$$

The filter capacitor value is selected such that it is less than Cac. Hence, a 330nF capacitor is selected in hardware implementation.

The filter inductor L_{ac} is calculated for mitigating high order harmonics close to 5 kHz frequency.

$$L_{ac} = \frac{1}{4\pi^2 f_c^2 C_d} = \frac{1}{4 \times (3.14 \times 5 \times 10^3)^2 \times 330 \times 10^{-9}} = 3.07mH \quad (9)$$

A 3.1mH inductor is selected for simulation and experimental system.

The input capacitors of the isolated half bridge dc-dc converter act as the output filter capacitors for the PFC converter. So, the design of the capacitor is eliminate the second order harmonic component as well as to provide maximum power for that duration when input voltage falls. This is very crucial for PC power supplies as the rating of the capacitor affects the size and the cost of the overall SMPS.

The expression for calculating the capacitor to reduce second order harmonic is as [3],

$$\frac{C_1}{2} = \frac{C_2}{2} = \frac{I_{PFC}}{2\omega\Delta V_{PFC}} = \frac{1.06\ A}{2 \times 314 \times 6V} = 0.28mF \quad (10)$$

The hold-up capability can be estimated as,

$$t_{hold-up} = \left(V_{PFCm}^2 - V_{PFC\ min}^2\right) \frac{C}{2P_o} \quad (11)$$

where, $t_{hold-up}$ is the holdup time of the capacitor, Po maximum output power, VPFCm is the minimum output voltage (2% ripple is considered) and V_{PFCm} in is the minimum voltage at which the output voltage holds regulation.

Therefore, to maintain 10ms hold-up time, capacitance is calculated as,

$$C = \frac{2t_{hold-up}P_o}{\left(V_{PFCm}^2 - V_{PFC\ min}^2\right)} = \frac{2 \times 10\ ms \times 320W}{(294V)^2 - (260V)^2} = 0.339mF \quad (12)$$

Two capacitors are connected in series. Therefore, the value of C1=C2=0.679 mF. The selected value of the 0.6mF each to meet both the conditions.

The calculation of inductance for the secondary winding with highest rating is shown here, while the

calculation for rest of the secondary windings remains same. The inductance L_{o1} is expressed as,

$$L_{o1} = \frac{V_{o1}(0.5 - D_s)}{f_s \Delta i_{Lo1}} = \frac{12V(0.5 - 0.4)}{60\,kHz \times 0.625\,A} = 0.032mH \quad (13)$$

Similarly, the inductances for the other secondary windings are calculated as 9.5 µH, 6.8 µH and 1.5 mH.

IV. SIMULATED PERFORMANCE OF THE POWER SUPPLY

The performance of proposed power supply is simulated to obtain its performance indices such as input voltage/current of input inductors (L_{p1}, L_{n1}), output inductors (L_{p2}, L_{n2}), intermediate capacitor (C_p, C_n) output voltage (V_{PFC}) and output voltages/currents (V_{o1}/I_{o1}, V_{o2}/I_{o2}, V_{o3}/I_{o3}, V_{o4}/I_{o4}). The simulated performance is discussed in following sections.

A. Full Load Performance

Full load performance of PFC bridgeless converter based computer SMPS is shown in Fig. 4. The input ac current is found to be sinusoidal with a harmonic distortion of 3.33% as shown in Figs. 4a and 4b. The output voltages are maintained constant with their respective output currents. The waveforms at various test points of the bridgeless PFC converters are shown in Fig. 4c. The currents of input inductors of both converters are shown which are maintained in CCM. The voltage across the intermediate capacitor is observed of the order of 450V which is quite satisfactory. The waveform of currents of output inductor of both positive half cycle and negative half cycle operated PFC converter demonstrates the DCM operation and the peak current in both the converters is observed to be about 17A. Both the converters operate in positive and negative half cycles of input voltage alternately.

This validates the bridgeless operation of the power supply. The peak voltage stress and current stress of the switch are observed of the order of 520V and 17A which are within acceptable limits**.**

B. Light Load Performance

Light load performance of the power supply is shown in Figs. 5a and 5b. Loads on +12V and +5V outputs are reduced simultaneously at 0.15s to demonstrate its dynamic performance. The output current is reduced from 12.5A to 3.75A and 18A to 9A as the load is perturbed. The input current is maintained sinusoidal and co-phase with input voltage. The input current THD at the light load condition is observed of the order of 3.76% as shown in Fig. 5b which is within acceptable limits IEC standard [23].

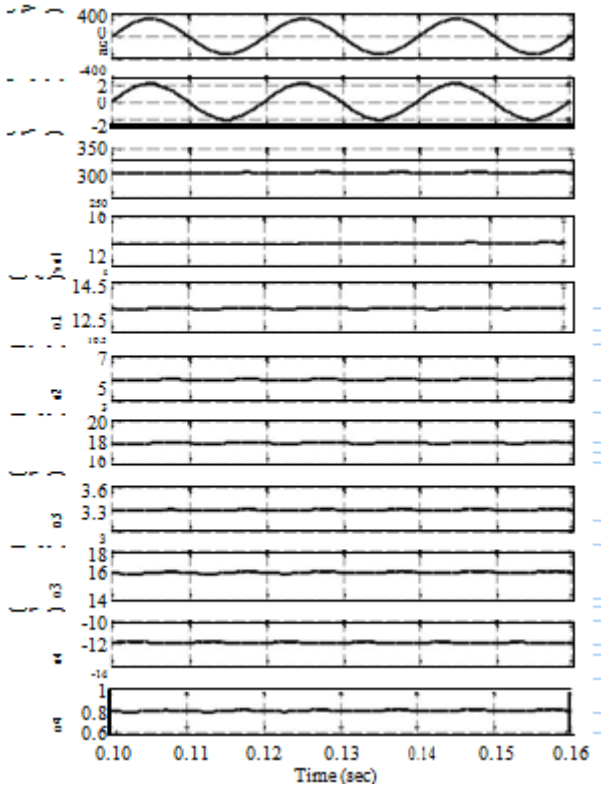


Fig.4a Performance of the computer power supply at rated condition

A. Performance of Conventional SMPS

The conventional computer SMPS draws a harmonic rich, distorted peaky input current with a high crest factor and low PF from the single phase ac mains. The THD of the input current is observed of the order of 80% and the PF is 0.53 which affects the distribution system as shown in Fig. 6. This violates the guidelines of harmonic emission set by the international power quality standards like IEC 61000-3-2, 2004 [23]. Therefore, it is highly recommended to improve the power quality of the conventional computer SMPS.

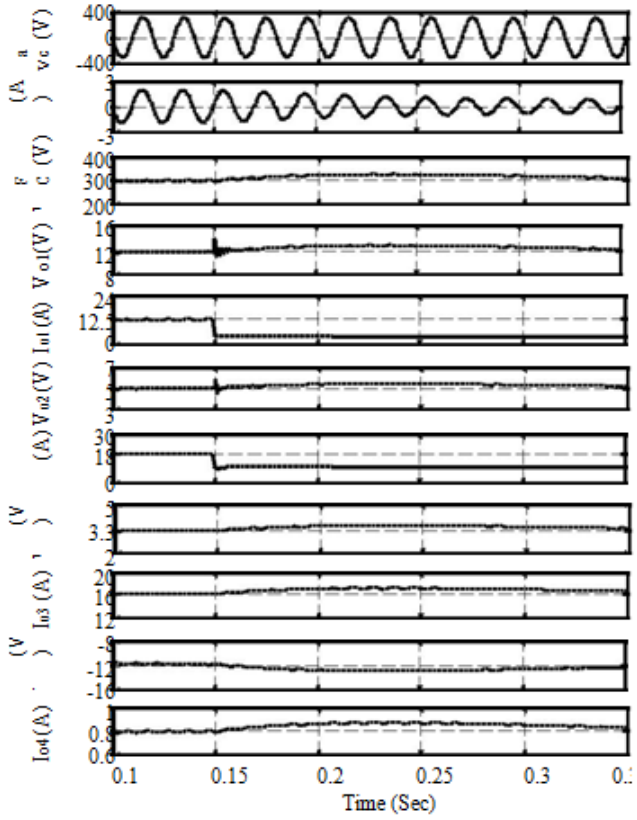


Fig.5a Performance of the computer power supply at light load condition

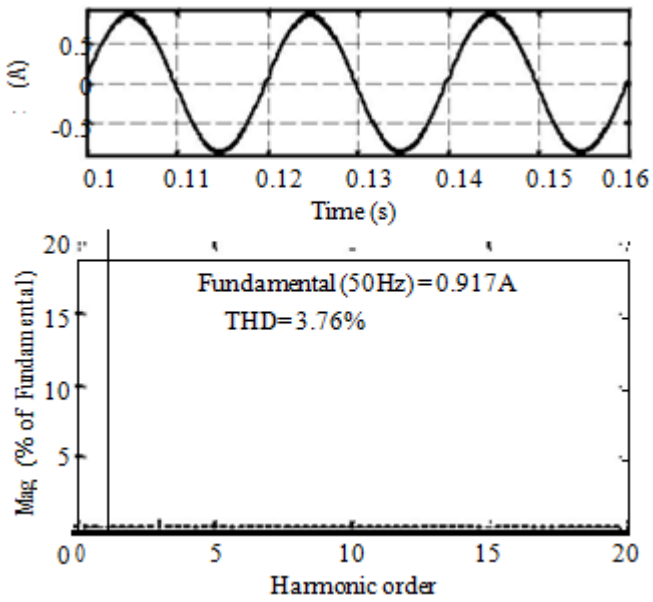


Fig. 5b Input current and its harmonic spectrum at light load condition

(a) (b) (c)

Fig. 6 (a) Waveform of vac and iac, (b) Pac and PF, (c) iTHD at light load.

B. Performance of SMPS under Varying Input Voltages

The experimental performance of PFC bridgeless converter based SMPS is shown in Fig.7 which is recorded at full load and rated voltage conditions. Fig. 7a shows the recorded waveforms of input and output voltages and currents where the unity PF operation is confirmed. The output voltage of the PFC converter is regulated to 300V which corroborates the results obtained from the simulation model. The inductor currents of the positive half cycle converter iLp1 and the negative half cycle converter iLn1 are shown in Fig. 7b which are in CCM as per the design. A similar CCM operation is depicted in the simulated performance Fig. 4c. The bridgeless operation of the proposed power supply is maintained by alternate operation of the upper and lower converter in the positive and negative half cycles of the input voltage and in line with the simulated performance. The inductor current of the positive half cycle converter i_{Lp1} is present during the positive half cycle of the input voltage and whereas i_{Ln1} is present during the negative half cycle. Fig. 7c shows the recorded waveforms of the output inductor currents i_{Lp2} and i_{Ln2} of the positive and negative half cycle converters. The peak current of both the inductors are observed to be 17A which is at the same value in the simulated performance as well (Fig. 4c). Both the currents touch zero in each switching cycle which verifies the design criteria of inductor current being in DCM. The upper inductor operates in DCM when input voltage is positive and the lower inductor operates in DCM when the input voltage is negative ensuring bridgeless operation. The capacitor voltages of both the converters are shown in Fig. 7d which operates alternately in positive and negative half cycles of the input voltage and are in CCM as per the design. Both capacitor voltages are equal in amplitude in simulation as well as in experimental results. The recorded waveforms of the regulated dc output voltages +12V, +5V, +3.3V and -12V with their respective currents are shown in Fig. 7(e)-(h). All the dc voltages are maintained constant and in line with the simulated results as depicted in Fig. 4(a). The recorded full load performance of the proposed SMPS is shown in Fig. 8. It can be seen that he recorded THD of input ac current is slightly higher than the simulated value. This is due to the resistance associated with the inductance used in the bridgeless PFC converter. The input current THD is 6.5% with unity PF. To demonstrate the performance of SMPS over widely varying input voltage range, the test results are recorded at 268.5 V and 176.8 V condition and are presented in Figs. 9 and 10. For this entire voltage range of 170V-270V, the input current remains sinusoidal while the PF is maintained to unity. The dynamic performance during input voltage variation is shown in Fig. 11 where the output voltage and output current are restored to the original values within a few power cycles.

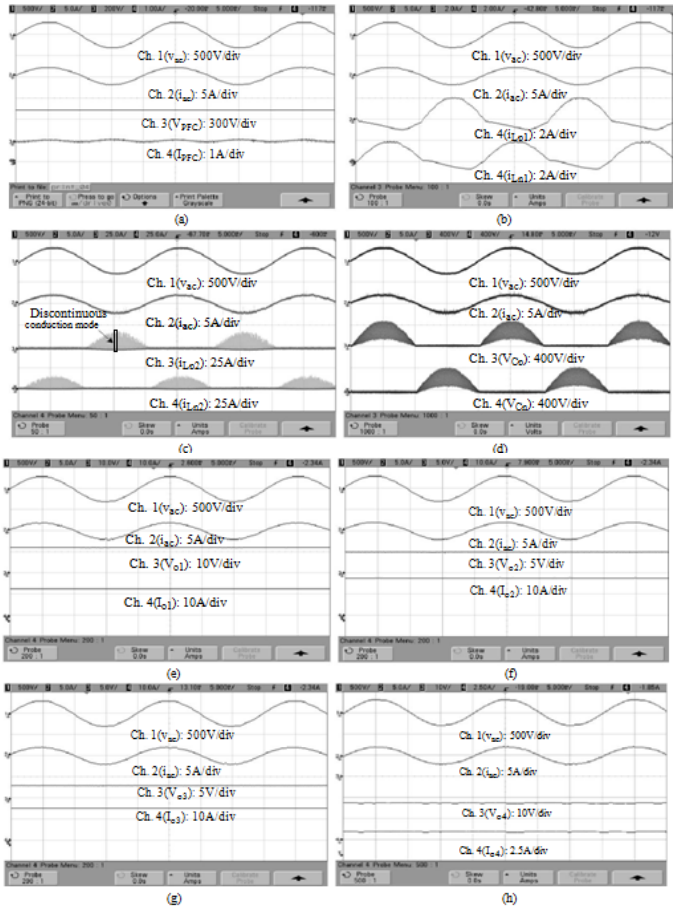


Fig. 7 Recorded waveforms of (a) v_{ac}, i_{ac}, V_{PFC} and I_{PFC}, (b) v_{ac}, i_{ac}, i_{Lp1} and i_{Ln1}, (c) v_{ac}, i_{ac}, i_{Lp2} and i_{Ln2}, (d) v_{ac}, i_{ac}, V_{Cp} and V_{Cn}, (e) v_{ac}, i_{ac}, V_{o1} and I_{o1}, (f) v_{ac}, i_{ac},V_{o2} and I_{o2}, (g) v_{ac}, i_{ac}, V_{o3} and I_{o3}, and (h) v_{ac}, i_{ac}, V_{o4} and I_{o4}

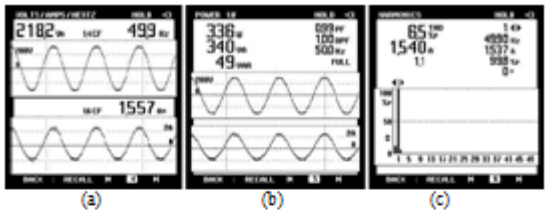


Fig. 8 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at full load

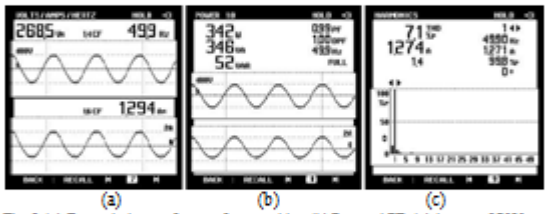


Fig. 9 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at 270V

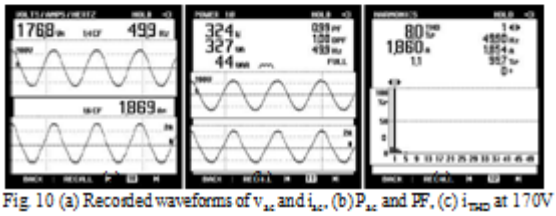


Fig. 10 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at 170V

C. Performance of SMPS Under Light Load

The light load performance of SMPS is recorded by switching on and off some loads and is shown in Fig. 12. The recorded test results demonstrate the fairly improved power quality and the input current being sinusoidal with its THD being 7.3% which is within the limit set by IEC 6100-3-2 [23]. Fig. 13 shows the recoded waveform of input and output voltages and currents when a step change is applied in load. The output voltage remains constant while the input current is changed to maintain the power balance.

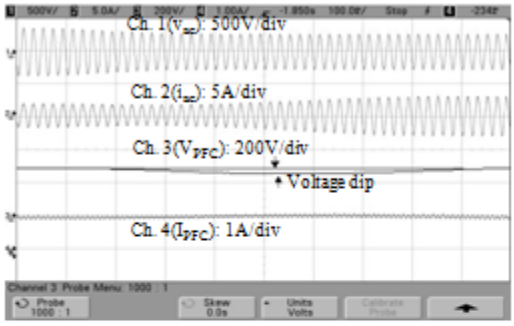


Fig. 11 Recorded waveforms of v_{ac}, i_{ac}, V_{PFC} and I_{PFC} during ac input voltage variation

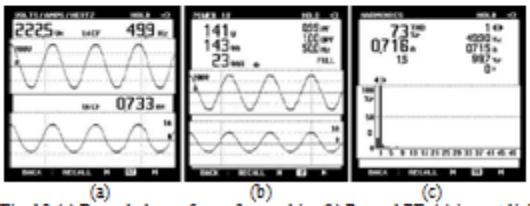
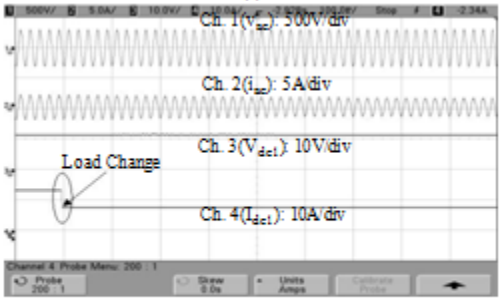


Fig. 12 (a) Recorded waveform of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at light load condition



(b)

Fig. 13 (a) Recorded waveform of load increase in I_{dc1} (b) Recorded waveform of load decrease in I_{dc1}

higher than the conventional PFC converter based SMPS. The efficiency of the SMPS system at full load is 89.1%. Table I shows the comparison of PFC based SMPS and proposed SMPS system. Test results demonstrate the excellent performance of the proposed bridgeless converter based SMPS under all operating conditions and hence it can be recommended as an effective solution for mitigation of power quality problems for computer applications.

V. CONCLUSION

A bridgeless non-isolated SEPIC based power supply has been proposed here to mitigate the power quality problems prevalent in any conventional computer power supply. The proposed power supply is able to operate satisfactorily under wide variations in input voltages and loads. The design and simulation of the proposed power supply are initially carried to demonstrate its improved performance. Further, a laboratory prototype is built and experiments are conducted on this prototype. Test results obtained are found to be in line with the simulated performance. They corroborate the fact that the power quality problems at the front end are mitigated and hence, the proposed circuit can be a recommended solution for computers and other similar appliances.

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