An Integrated Dynamic Voltage Restorer-Ultracapacitor Design For Improving Power Quality of The Distribution Grid

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Abstract- *Cost of various energy storage technologies is decreasing rapidly and the integration of these technologies into the power grid is becoming a reality with the advent of smart grid. Dynamic voltage restorer (DVR) is one product that can provide improved voltage sag and swell compensation with energy storage integration. Ultracapacitors (UCAP) have low-energy density and high-power density ideal characteristics for compensation of volt-age sags and voltage swells, which are both events that require high power for short spans of time. The novel contribution of this paper lies in the integration of rechargeable UCAP-based energy stor-age into the DVR topology. With this integration, the UCAP-DVR system will have active power capability and will be able to inde-pendently compensate temporary voltage sags and swells without relying on the grid to compensate for faults on the grid like in the past. UCAP is integrated into dc-link of the DVR through a bidi-rectional dc–dc converter, which helps in providing a stiff dc-link voltage, and the integrated UCAP-DVR system helps in compen-sating temporary voltage sags and voltage swells, which last from 3 s to 1 min. Complexities involved in the design and control of both the dc–ac inverter and the dc–dc converter are discussed. The simulation model of the overall system is developed and compared to the experimental hardware setup.*

Keywords- DC–DC converter, d–q control, DSP, dynamic voltage restorer (DVR), energy storage integration, phase locked loop (PLL), sag/swell, Ultracapacitor (UCAP).

I. INTRODUCTION

THE CONCEPT of using inverter-based dynamic voltage restorers (DVRs) for preventing customers from momen-tary voltage disturbances on the utility side was demonstrated

for the first time by Woodley et al. . The concept of using the DVR as a power quality product has gained significant pop-ularity since its first use. In , the authors propose the usage of the DVR with rechargeable energy storage at the dc-terminal to meet the active power requirements of the grid during volt-age disturbances. In order to avoid and minimize the active power injection into the grid, the authors also mention an alter-native solution which is to compensate for the voltage sag by inserting a lagging voltage in quadrature with the line current. Due to the high cost of rechargeable energy storage, various other types of control strategies have also been developed in the literature to minimize the active power injection from the DVR. The high cost of the rechargeable energy stor-age prevents the penetration of the DVR as a power quality product. However, the cost of rechargeable energy storage has been decreasing drastically in the recent past due to various technological developments and due to higher penetration in the market in the form of auxiliary energy storage for dis-tributed energy resources (DERs) such as wind, solar, hybrid electric vehicles (HEVs), and plug-in hybrid electric vehicle (PHEVs) . Therefore, there has been renewed interest in the literature to integrate rechargeable energy stor-age again at the dc-terminal of power quality products such as static compensator (STATCOM) and DVR.

Various types of rechargeable energy storage technologies based on superconducting magnets (SMES), flywheels (FESS), batteries (BESS), and ultracapacitors (UCAPs) are compared in [10] for integration into advanced power applications such as DVR. Efforts have been made to integrate energy stor-age into the DVR system, which will give the system active power capability that makes it independent of the grid during voltage disturbances. In , cascaded H-bridge-based DVR with a thyristor-controlled inductor is proposed to minimize the energy storage requirements. In, flywheel energy storage is integrated into the DVR system to improve its steady-state series and shunt compensation.

Of all the rechargeable energy storage technologies, UCAPs are ideally suited for applications which need active power sup-port in the milliseconds to seconds timescale . Therefore, UCAP-based integration into the DVR system is ideal, as the normal duration of momentary voltage sags and

swells is in the milliseconds to seconds range . UCAPs have low-energy density and high-power density ideal characteristics for compensating voltage sags and voltage swells, which are both events that require high amount of power for short spans of time. UCAPs also have higher number of charge/discharge cycles when compared to batteries and for the same module size, UCAPs have higher terminal voltage when compared to batteries, which makes the integration easier. With the preva-lence of renewable energy sources on the distribution grid and the corresponding increase in power quality problems, the need for DVRs on the distribution grid is increasing . Super-capacitor-based energy storage integration into the DVR for the distribution grid is proposed in and . However, the concept is introduced only through simulation and the exper-imental results are not presented. In this paper, UCAP-based

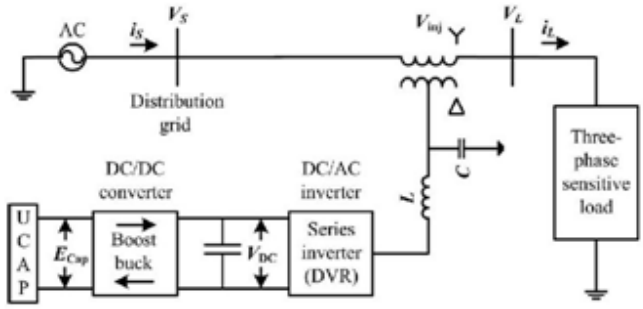


Fig. 1. One-line diagram of DVR with UCAP energy storage.

energy storage integration to a DVR into the distribution grid is proposed and the following application areas are addressed.

1) Integration of the UCAP with DVR system gives active power capability to the system, which is necessary for independently compensating voltage sags and swells.

2) Experimental validation of the UCAP, dc–dc converter, and inverter their interface and control.

3) Development of inverter and dc–dc converter controls to provide sag and swell compensation to the distribution grid.

4) Hardware integration and performance validation of the integrated DVR-UCAP system.

II. THREE-PHASE SERIES INVERTER

A. Power Stage

The one-line diagram of the system is shown in Fig. 1. The power stage is a three-phase voltage source inverter, which is connected in series to the grid and is responsible for compen-sating the voltage sags and swells; the model of the series DVR and its controller is shown in Fig. 2. The inverter system con-sists of an insulated gate bipolar transistor (IGBT) module, its gate-driver, LC filter, and an isolation transformer. The dc-link voltage Vdc is regulated at 260 V for optimum performance of the converter and the line–line voltage Vab is 208 V; based on

these, the modulation index m of the inverter is given by

$$m = \frac{2\sqrt{2}}{\sqrt{3}V_{dc} * n} V_{ab(rms)}. \quad (1)$$

where n is the turns ratio of the isolation transformer. Substituting n as 2.5 in (1), the required modulation index is calculated as 0.52. Therefore, the output of the dc–dc con-verter should be regulated at 260 V for providing accurate voltage compensation. The objective of the integrated UCAP-DVR system with active power capability is to compensate for temporary voltage sag (0.1–0.9 p.u.) and voltage swell (1.1–1.2 p.u.), which last from 3 s to 1 min [15]

B. Controller Implementation

There are various methods to control the series inverter to provide dynamic voltage restoration and most of them rely on injecting a voltage in quadrature with advanced phase, so that reactive power is utilized in voltage restoration [3]. Phase-advanced voltage restoration techniques are complex in imple-mentation, but the primary reason for using these techniques is to minimize the active power support and thereby the amount of energy storage requirement at the dc-link in order to minimize the cost of energy storage. However, the cost of energy storage has been declining and with the availability of active power sup-port at the dc-link, complicated phase-advanced techniques can be avoided and voltages can be injected in-phase with the sys-tem voltage during a voltage sag or a swell event. The control method requires the use of a PLL to find the rotating angle. As discussed previously, the goal of this project is to use the active power capability of the UCAP-DVR system and compensate temporary voltage sags and swells.

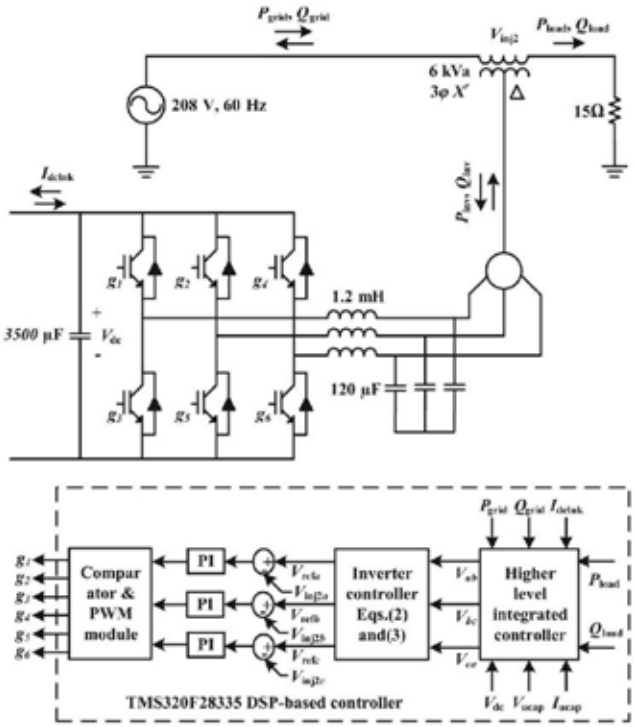


Fig. 2. Model of three-phase series inverter (DVR) and its controller with integrated higher order controller.

The inverter controller implementation is based on injecting voltages in-phase with the supply-side line–neutral voltages. This requires PLL for estimating θ, which has been imple-mented using the fictitious power method described in [18]. Based on the estimated θ and the line–line source voltages, Vab, Vbc, and Vca (which are available for this delta-sourced system) are transformed into the d–q domain and the line– neutral components of the source voltage Vsa, Vsb, and Vsc, which are not available, can then be estimated using

$$\begin{bmatrix} V_{sa} \\ V_{sb} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta - \frac{\pi}{6}\right) & \sin\left(\theta - \frac{\pi}{6}\right) \\ \cdots & \cdots \end{bmatrix} \begin{bmatrix} V_{\phi} \\ \cdots \end{bmatrix} \quad (2)$$

$$v_{ref_a} = m \sin\left(\theta - \frac{16a}{169.7}\right) \quad (3)$$

$$V_{ref_b} = V_{ref_c} = \sin\left(\theta + \frac{2\pi}{3} - \frac{V_{sb}}{169.7}\right)$$

$$P_{inv} = 3V_{inj2a(rms)} I_{La(rms)} \cos\phi$$

$$Q_{inv} = 3V_{inj2a(rms)} I_{La(rms)} \sin\phi. \quad (4)$$

These voltages are normalized to unit sine waves using line– neutral system voltage of 120 Vrms as reference and compared to unit sine waves in-phase with actual system voltages Vs from (3) to find the injected voltage references Vref necessary to maintain a constant voltage at the load terminals, where m is 0.52 from (1). Therefore, whenever there is a voltage sag or swell on the source side, a corresponding voltage Vinj2 is injected in-phase by the DVR and UCAP system to negate the effect and retain a constant voltage VL at the load end. The actual active and reactive power supplied by the series inverter can be computed using (4) from the rms values of the injected voltage Vinj2a and load current ILa, and ϕ is the phase difference between the two waveforms.

III. UCAP AND BIDIRECTIONAL DC–DC CONVERTER

A. UCAP Bank Hardware Setup

The choice of the number of UCAPs necessary for provid-ing grid support depends on the amount of support needed, terminal voltage of the UCAP, dc-link voltage, and distribu-tion grid voltages. In this paper, the experimental setup consists of three 48 V, 165F UCAPs (BMOD0165P048) manufac-tured by Maxwell Technologies, which are connected in series. Therefore, the terminal voltage of the UCAP bank is 144 V and the dc-link voltage is programmed to 260 V. This would give the dc–dc converter a practical operating duty ratio of 0.44–0.72 in the boost mode while the UCAP is discharging and 0.27– 0.55 in the buck mode while the UCAP is charging from the grid through the dc-link and the dc–dc converter. It is practi-cal and cost-effective to use three modules in the UCAP bank. Assuming that the UCAP bank can be discharged to 50% of its initial voltage (Vuc,ini) to final voltage (Vuc,fin) from 144 to 72 V, which translates to depth of discharge of 75%, the energy in the UCAP bank available for discharge is given by

$$E_{UCAP} = \frac{1}{2} * C * \frac{(V_{uc,ini}^2 - V_{uc,fin}^2)}{60} W - min$$

$$E_{UCAP} = \sqrt{2} * 65/3 * 144^2 - 72^2/60 \quad (5)$$

$$= 7128\ W - min.$$

B. Bidirectional DC–DC Converter and Controller

A UCAP cannot be directly connected to the dc-link of the inverter like a battery, as the voltage profile of the UCAP varies as it discharges energy. Therefore, there is a need to inte-grate the UCAP system through a bidirectional dc–dc converter, which maintains a stiff dc-link voltage, as the UCAP voltage decreases while discharging and increases while charging. The model of the bidirectional dc–dc converter and its controller are shown in Fig. 3, where the

input consists of three UCAPs connected in series and the output consists of a nominal load of 213.5 Ω to prevent operation at no-load, and the output is connected to the dc-link of the inverter. The amount of active power support required by the grid during a voltage sag event is dependent on the depth and duration of the voltage sag, and the dc–dc converter should be able to withstand this power during the discharge mode. The dc–dc converter should also be able

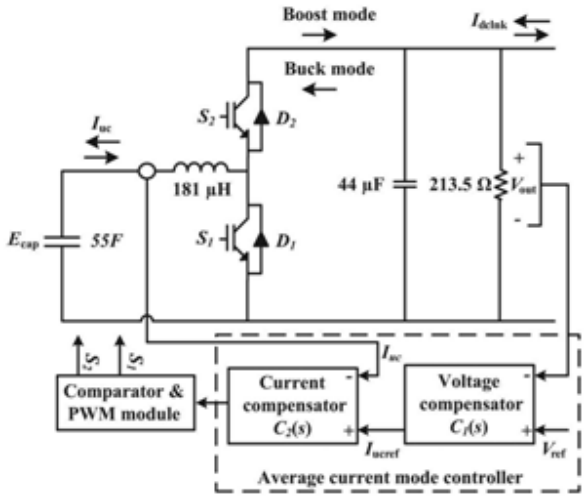


Fig. 3. Model of the bidirectional dc–dc converter and its controller.

to operate in bidirectional mode to be able to charge or absorb additional power from the grid during voltage swell event. In this paper, the bidirectional dc–dc converter acts as a boost con-verter while discharging power from the UCAP and acts as a buck converter while charging the UCAP from the grid.

A bidirectional dc–dc converter is required as an interface between the UCAP and the dc-link since the UCAP voltage varies with the amount of energy discharged while the dc-link voltage has to be stiff. Therefore, the bidirectional dc–dc con-verter is designed to operate in boost mode when the UCAP bank voltage is between 72 and 144 V and the output voltage is regulated at 260 V. When the UCAP bank voltage is below 72 V, the bidirectional dc–dc converter is operated in buck mode and draws energy from the grid to charge the UCAPs and the output voltage is again regulated at 260 V.

Average current mode control, which is widely explored in literature [19], is used to regulate the output voltage of the bidi-rectional dc–dc converter in both buck and boost modes while charging and discharging the UCAP bank. This method tends to be more stable when compared to other methods such as voltage mode control and peak current mode control. Average current mode controller is shown in Fig. 3, where the dc-link and actual output voltage Vout is compared with the reference voltage Vref and the error is passed through the voltage com-pensator C1(s), which generates the average reference current Iucref . When the inverter is discharging power into the grid dur-ing voltage sag event, the dc-link voltage Vout tends to go below the reference Vref and the error is positive; Iucref is positive and the dc–dc converter operates in boost mode. When the inverter is absorbing power from the grid during voltage swell event or charging the UCAP, Vout tends to increase above the refer-ence Vref and the error is negative; Iucref is negative and the dc–dc converter operates in buck mode. Therefore, the sign of the error between Vout and Vref determines the sign of Iucref and thereby the direction of operation of the bidirectional dc–dc converter. The reference current Iucref is then compared to the actual UCAP current (which is also the inductor current) Iuc and the error is then passed through the current compensator C2(s). The compensator transfer functions, which provide a stable response, are given by

$$C_1(s) = 1.67 + \frac{23.81}{s} \quad (6)$$

$$C_2(s) = 3.15 + \frac{1000}{s}. \quad (7)$$

IV. SIMULATION RESULTS

The simulation of the proposed UCAP-integrated DVR sys-tem is carried out in PSCAD for a 208 V, 60-Hz system where 208 V is 1 p.u. The system response for a three-phase voltage sag, which lasts for 0.1 s and has a depth of 0.84 p.u., is shown in Fig. 4(a)–(e). It can be observed from Fig. 4(a) that during voltage sag, the source voltage V_{srms} is reduced to 0.16 p.u. while the load voltage V_{Lrms} is maintained constant at around 0.9 p.u. due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line–line source voltages [V_{sab}, V_{sbc}, V_{sca}; Fig. 4(b)], the line–line load voltages [V_{Lab}, V_{Lbc}, V_{Lca}; Fig. 4(c)], and the line–neutral injected voltages of the series inverter [V_{inj2a}, V_{inj2b}, V_{inj2c}; Fig. 4(d)]. Finally, it can be observed from Fig. 4(e) that V_{inj2a} lags V_{sab} by 30°, which indicates that it is *in-phase* with the line–neutral source voltage V_{sa}. In Fig. 5(a), plots of the bidi-rectional dc–dc converter are presented and it can be observed that the dc-link voltage $V_{f\,dc}$ is regulated at 260 V, the average dc-link current $I_{dclnkav}$ and the average UCAP current I_{ucav} increase to provide the active power required by the load dur-ing the sag. Although the UCAP is discharging, the change in the UCAP voltage E_{cap} is not visible in this case due to the short duration of the simulation, which is due to limitations in PSCAD software. It can also be observed from the various active power plots shown in Fig. 5(b) where the power sup-plied to the load P_{load} remains constant even during the voltage sag when the grid power P_{grid} is decreasing. The active power

deficit of the grid is met by the inverter power P_{inv}, which is almost equal to the input power to the inverter $P_{\text{dc\_}n}$ avail-able from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and the load during the voltage sag event is being met by the integrated UCAP-DVR system through the bidirectional dc–dc converter and the inverter. Similar analysis can also be extended for volt-age sags, which occur in one of the phases (*a*, *b*, or *c*) or in two of the phases (*ab*, *bc*, or *ca*). However, the active power requirement is greatest for the case where all the three phases ABC experience voltage sag.

The system response for a three-phase voltage swell, which lasts for 0.1 s and has a magnitude of 1.2 p.u., is shown in Fig. 6(a)–(e). It can be observed that during voltage swell, the source voltage V_{srms} increases to 1.2 p.u., whereas the load voltage V_{Lrms} is maintained constant at around 1 p.u. due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line–line source volt-ages [V_{sab}, V_{sbc}, V_{sca}; Fig. 6(a)], the line–line load voltages [V_{Lab}, V_{Lbc}, V_{Lca}; Fig. 6(b)], and the line–neutral injected voltages of the series inverter [$V_{\text{inj2}a}$, $V_{\text{inj2}b}$, $V_{\text{inj2}c}$; Fig. 6(c)]. Finally, it can be observed that $V_{\text{inj2}a}$ lags V_{sab} by 150°, which indicates that it is 180° out of phase with the line–neutral source voltage V_{sa} as required by the in-phase control algorithm. In Fig. 7(a), plots of the bidirectional dc–dc converter are pre-sented and it can be observed that the dc-link voltage $V_{f\,\text{dc}}$ is regulated at 260 V, the average dc-link current I_{dclnkav} and the average UCAP current I_{ucav} change direction to absorb the additional active power from the grid into the UCAP during the voltage swell event. The overshoot in I_{ucav} and I_{dclnkav} during startup at 0.1 s and during mode changes at 0.15 and 0.35 s is due to the mismatch between the breaker action and the compensator action in PSCAD, which is a modeling problem present in the simulation and does not shown in the experimen-tal results. Again, due to PSCAD limitations, which restrict the duration of the simulation, the increase in E_{cap} due to charg-ing of the UCAP during the voltage swell is not visible. This can also be observed from various active power plots where the power supplied to the load P_{load} remains constant even dur-ing the voltage swell when the grid power P_{grid} is increasing. It can be observed from the inverter power P_{inv} and inverter input power $P_{\text{dc\_in}}$ plots that the additional active power from the grid is absorbed by the inverter and transmitted to the UCAP. Therefore, it can be concluded from the plots that the additional active power from the grid during the voltage swell event is being absorbed by the UCAP-DVR system through the bidirectional dc–dc converter and the inverter.

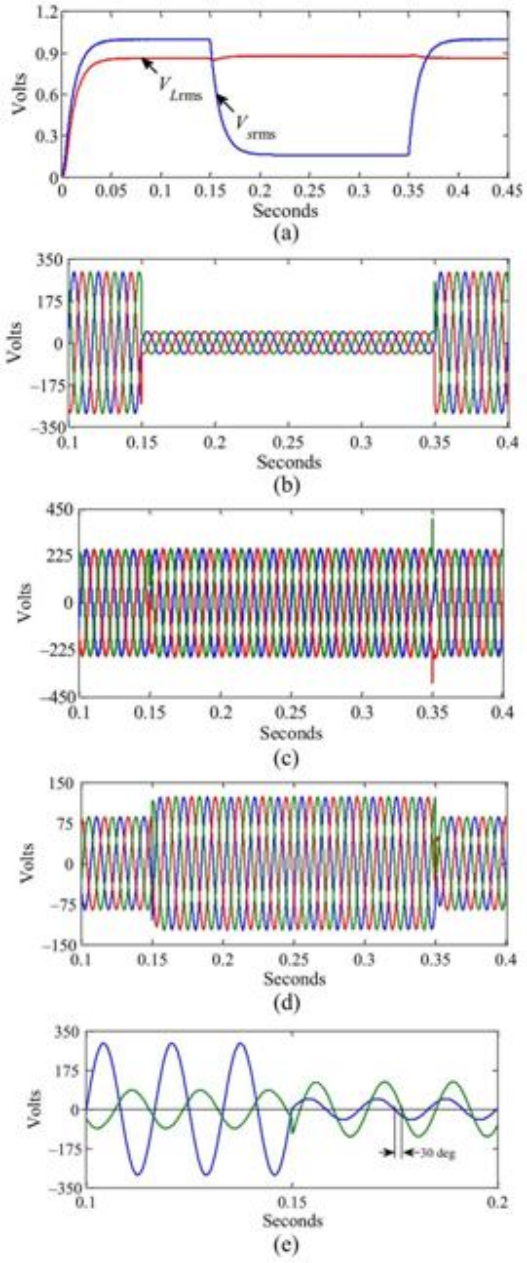


Fig. 4. (a) Source and load RMS voltages V_{srms} and V_{Lrms} during sag.

(b) Source voltages V_{sab} (blue), V_{sbc} (red), and V_{sca} (green) during sag.

(c) Load voltages V_{Lab} (blue), V_{Lbc} (red), and V_{Lca} (green) during sag.

(d) Injected voltages $V_{\text{inj2}a}$ (blue), $V_{\text{inj2}b}$ (red), and $V_{\text{inj2}c}$ (green) during sag.

(e) $V_{\text{inj2}a}$ (green) and V_{sab} (blue) waveforms during sag.

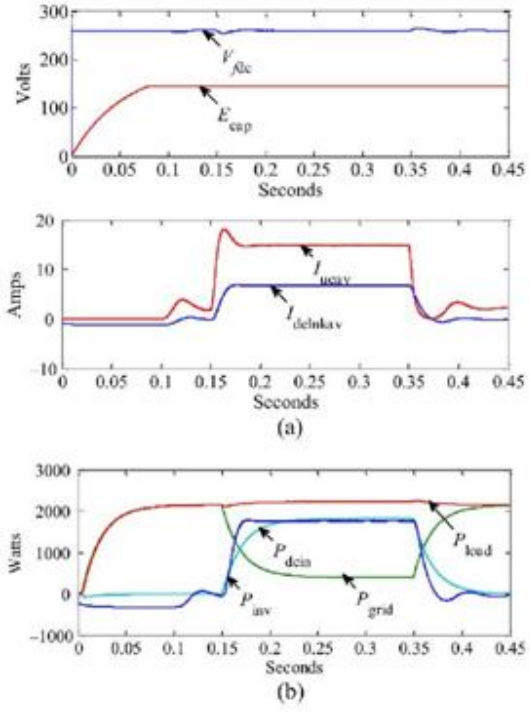


Fig. 5. (a) Currents and voltages of dc–dc converter. (b) Active power of grid, load, and inverter during voltage sag.

V. EXPERIMENTAL RESULTS

In order to verify the concept and simulation results exper-imentally, a hardware prototype of the complete system was constructed and is shown in Fig. 8(a) and (b). In Fig. 8(a), the complete inverter system is shown; it consists of a sen-sor board, an interface board, TMS320F28335 DSP controller, and their power supply circuit in the top (first) shelf. In the second shelf, the Inverter IGBT module (BSM100GD60DLC), which is 600 V 100 A six-pack module from Infineon, its gate driver SKHI 61R manufactured by SEMIKRON, and the 3500 µF 450 Vdc dc-link capacitor are placed; the third shelf has the LC-filter, which consists of 1.2 mH 45 A three-phase inductor and three 120 µF 240 Vac capacitors connected in wye configuration; the fourth shelf consists of three 2 kVa 125 /50 V single-phase isolation transformers

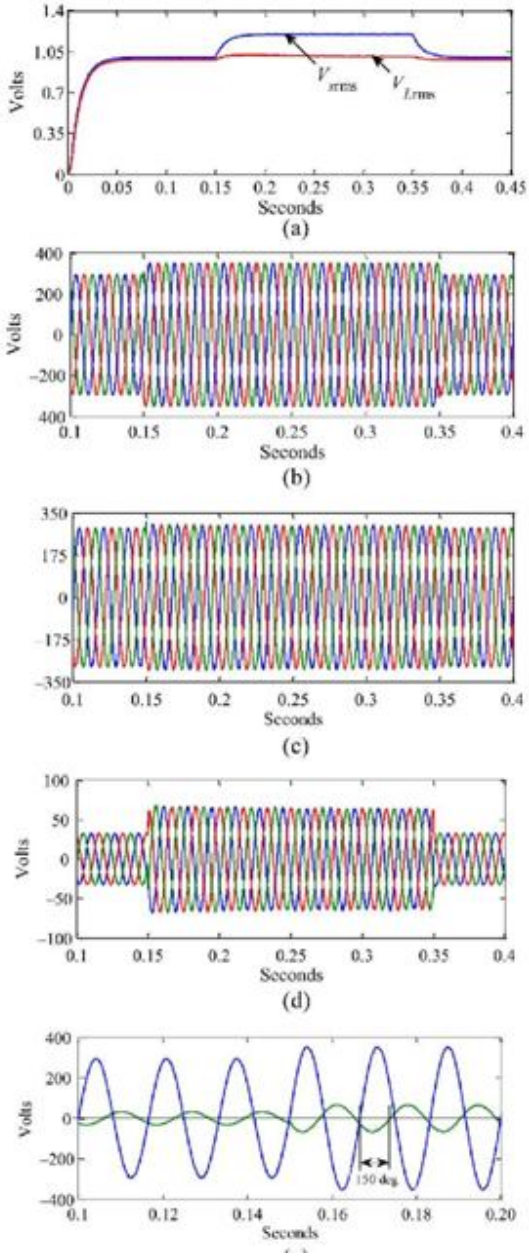


Fig. 6. (a) Source and load rms voltages V_{srms} and V_{Lrms} during swell.

(b) Source voltages V_{sab} (blue), V_{sbc} (red), and V_{sca} (green) during swell.

(c) Load voltages V_{Lab} (blue), V_{Lbc} (red), and V_{Lca} (green) during swell.

(d) Injected voltages $V_{\text{inj2}a}$ (blue), $V_{\text{inj2}b}$ (red), $V_{\text{inj2}c}$ (green) during swell.

(e) $V_{\text{inj2}a}$ (green) and V_{sab} (blue) waveforms during swell.

connected in delta configuration on the primary side, and the secondary sides are connected in series with the grid through a protection circuit breaker. In Fig. 8(b), the UCAP, the bidi-rectional dc–dc converter, the oscilloscope (MSO4034B used

for recording the data), and the industrial power corruptor are shown.

In Fig. 9(a) and (b), the experimental waveforms of the inverter and the bidirectional dc–dc converter are shown for the case where the grid experiences voltage sag of 0.84 p.u. magnitude for 1-min duration. In Fig. 9(a), the dc-link

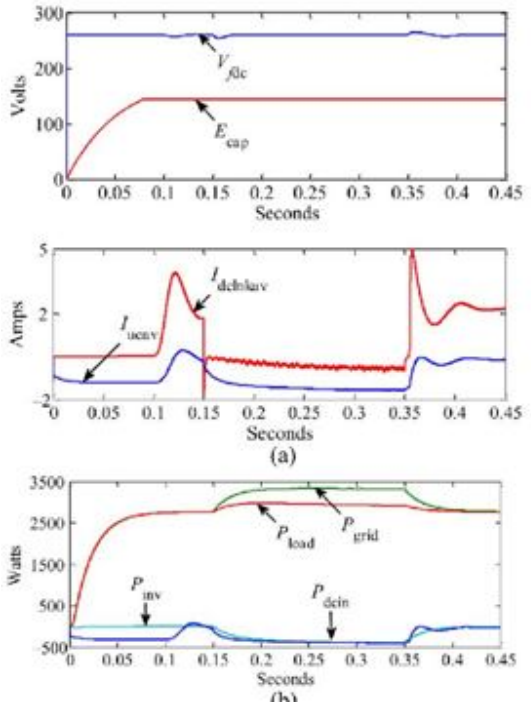
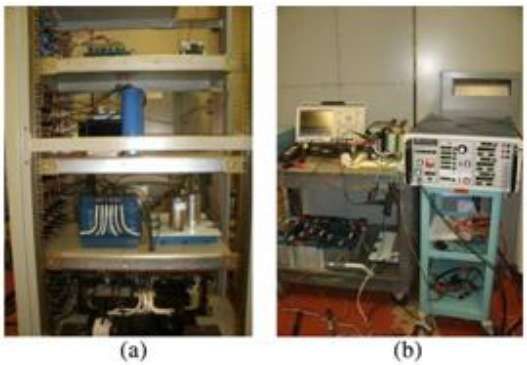


Fig. 7. (a) Currents and voltages of dc–dc converter during swell. (b) Active and reactive power of grid, load, and inverter during a voltage swell.



(a) (b)

Fig. 8. (a) Sensor, interface, and DSP boards (first); dc-link capacitor and Inverter (second); LC filter (third); and isolation transformer (fourth). (b) DC– DC converter and MSO4034B oscilloscope (top shelf), UCAP bank with three UCAPs (bottom shelf) and the industrial power corruptor.

voltage Vf dc (CH1), the UCAP voltage Ecap (CH2), the dc-link current Idclnk (CH3), and the average UCAP current Iucav (CH4) are shown. It can be observed from Fig. 9(a) that during the voltage sag, Ecap is decreasing rapidly and Iucav is increasing rapidly, while Vf dc and Idclnkav are constant. Therefore, the dc–dc converter is able to regulate the dc-link voltage to 260 V and operates in the boost mode to discharge active power during a voltage sag event to meet the active power deficit between the grid and the load. In Fig. 8(b), the zoomed-in versions of the line–line source voltage Vsab (CH1), line–line load voltage VLab (CH2), the line–neutral injected voltage Vinj2a (CH1), and the load current ILa (CH4) during the voltage sag event are shown. It can be observed that

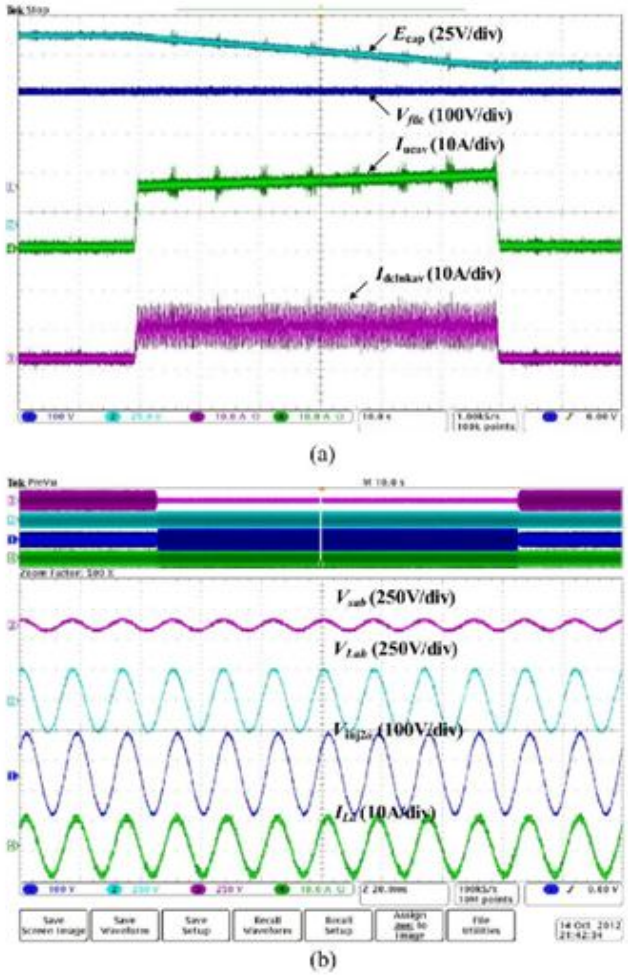


Fig. 9. (a) UCAP and bidirectional dc–dc converter experimental waveforms
Ecap (CH1), Vf dc (CH2), Idclnk (CH3) and Iucav (CH4) during voltage sag. (b) Inverter experimental waveforms Vsab (CH1), VLab (CH2) and Vinj2a (CH3) and ILa (CH4) during the voltage sag.

during the voltage sag event, the magnitude of V_{sab} is reduced, whereas the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a}, which increases during the voltage sag event to compensate for the voltage sag. It can also be observed that the load current I_{La} is constant and in-phase with

the injected voltage V_{inj2a}, which lags V_{sab} and V_{Lab} by 30°. Therefore, from both inverter and dc–dc converter experimental waveforms, it can be concluded that the integrated UCAP-DVR system hardware setup is able to respond instantaneously to compensate voltage sags.

Similarly, in Fig. 10(a) and (b), the dc–dc converter and the inverter experimental waveforms are presented for the case where the grid experiences a voltage swell of 1.2 p.u. magni-tude, which lasts for 1-min duration. It can be observed from Fig. 10(a) that during the voltage swell, E_{cap} is increasing slowly I_{ucav} and $I_{dclnkav}$ are negative while $V_{f\ dc}$ stays con-stant. This indicates that the dc–dc converter is able to regulate the dc-link to 260 V and operate in *buck* mode to charge the UCAP and absorb the additional power from the grid dur-ing the voltage swell into the UCAP, which also proves the

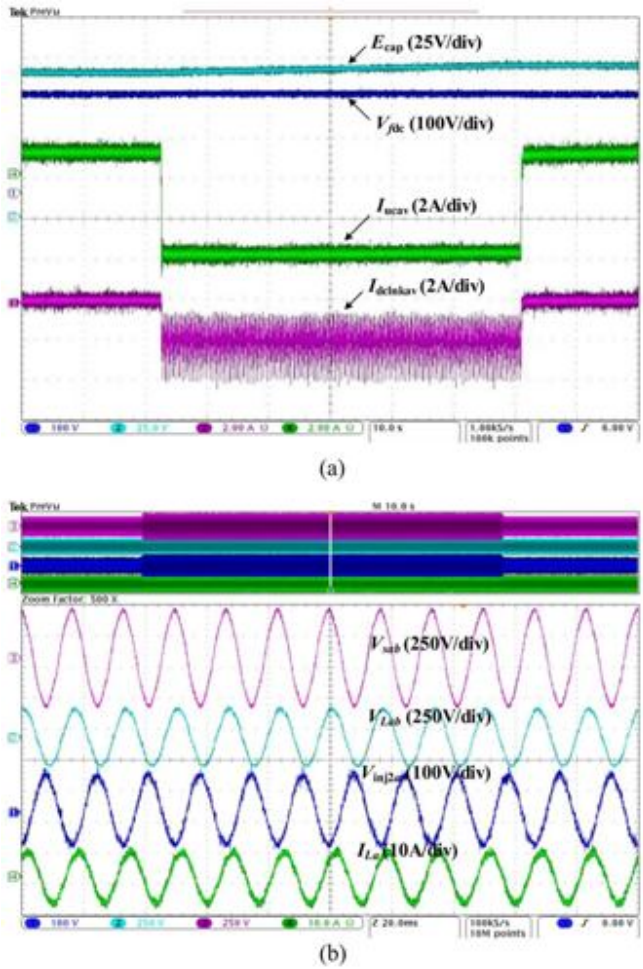


Fig. 10. (a) UCAP and dc–dc converter experimental waveforms E_{cap} (CH1), $V_{f\ dc}$ (CH2), I_{dclnk} (CH3), and I_{ucav} (CH4) during voltage swell.
(b) Inverter experimental waveforms V_{sab} (CH1), V_{Lab} (CH2) and V_{inj2a} (CH3) and I_{La} (CH4) during the voltage swell

bidirectional capability of the converter. It can be observed from Fig. 10(b) that during the voltage swell event, the magnitude of V_{sab} has increased while the magnitude of V_{Lab} remains constant due to the injected voltage V_{inj2a}, which increases to compensate for the voltage swell. It can also be observed that the load current I_{La} is constant and in-phase with the injected voltage V_{inj2a}, which lags V_{sab} and V_{Lab} by 180°. Therefore, from the inverter and dc–dc converter experimental waveforms, it can be concluded that hardware setup is able to respond instantaneously to compensate voltages swells and operates in bidirectional mode.

In Table I, the inverter and the bidirectional dc–dc converter experimental results are presented for both the sag and swell cases. The values listed in the table for the inverter are the rms values of the zoomed-in portion of V_{inj2a} and I_{La} wave-forms in Figs. 9(b) and 10(b). Similarly, the values listed for the dc–dc converter are the values which fall on the *Y* -bar of Figs. 9(a) and 10(a). Based on these values, the inverter output power P_{inv} can be computed using (6) and the inverter input power P_{dc} is the output power of the dc–dc converter. It can be

TABLE I SERIES INVERTER AND DC–DC CONVERTER EXPERIMENTAL RESULTS

Series inverter experimental results						
Zone	φ	V_{inj2a} (V)	I_{La} (A)	P_{inv} (W)	P_{dc} (W)	η (%)
Sag	0°	102.5	6.8	2091	2206	94.7
Swell	225°	42.43	6.7	–603	–494	83.3
DC–DC converter experimental results						
Zone	E_{cap} (V)	I_{ucav} (A)	I_{dclnk} (A)	P_{in} (W)	P_{out} (W)	η (%)
Sag	126.0	19.0	8.1	2406.6	2206	91.6
Swell	106.0	–4.0	1.9	–494.0	–424.0	85.8

observed that both the inverter and the dc–dc converter are very efficient for the voltage sag case, while their efficiencies drop a little for the voltage swell case where the lower power levels of operation impact the efficiency. Finally, it can be concluded that the UCAP-DVR system with active power capability can operate efficiently in a bidirectional fashion to both discharge and absorb active power from the grid. The efficiency of the inverter and dc–dc converter are around 95% and 92%, respec-tively, from Table I when the UCAP-DVR system provides active power support during a voltage sag event. The transient response of the UCAP-DVR system in this case is less than two electrical cycles or 33 ms. Similarly, the efficiency of the inverter and the dc–dc converter while the UCAP-DVR system is providing support during a temporary voltage swell event is 83.3% and 86%, respectively, the transient response remains the same at two electrical cycles or 33 ms. Therefore, the UCAP-DVR system is able to compensate temporary sags/swells or interruptions on the distribution grid, which last from 3 s to 1 min and require

active power support. This kind of integra-tion will be necessary to improve the active power capability of the DVR.

In Fig. 11(a) and (b), the UCAP-PC system performance when the system experiences unbalanced voltage sag is pre-sented. It can be observed from Fig. 11(a) that a 20% voltage sag is generated in phases *a* and *b*, and the system voltages V_{sa} and V_{sb} experience a voltage sag. However, the load current I_{La} remains constant because of the active power support to the sensitive load from the UCAP-DVR system even after the grid experiences unbalanced voltage sag. This clearly indicates that the PLL tracks the fundamental component even during unbalanced scenarios, which allows the UCAP Active Power Filter (UCAP-APF) system to provide active and reactive power support to the grid under unbalanced conditions. From the bidi-rectional dc–dc converter waveforms shown in Fig. 11(b), it can be observed that during the unbalanced voltage sag, which lasts for 1 s, the dc-link voltage $V_{f\ dc}$ has slight fluctuations and settles down to steady-state value of 260 V in less than two electrical cycles or 33 ms.

VI. CONCLUSION

In this paper, the concept of integrating UCAP-based rechargeable energy storage to the DVR system to improve its voltage restoration capabilities is explored. With this integra-tion, the DVR will be able to independently compensate voltage sags and swells without relying on the grid to compensate for faults on the grid. The UCAP integration through a bidirectional dc–dc converter at the dc-link of the DVR is proposed. The power stage and control strategy of the series inverter, which acts as the DVR, are discussed. The control strategy is simple and is based on injecting voltages in-phase with the system volt-age and is easier to implement when the DVR system has the ability to provide active power. A higher level integrated con-troller, which takes decisions based on the system parameters, provides inputs to the inverter and dc–dc converter controllers to carry out their control actions. Designs of major components in the power stage of the bidirectional dc–dc converter are dis-cussed. Average current mode control is used to regulate the output voltage of the dc–dc converter due to its inherently sta-ble characteristic. The simulation of the UCAP-DVR system, which consists of the UCAP, dc–dc converter, and the grid-tied inverter, is carried out using PSCAD. Hardware experimental setup of the integrated system is presented and the ability to pro-vide temporary voltage sag and swell compensation in all three phases to the distribution grid dynamically is tested. Results for transient response during voltage sags/swells in two phases will be included in the full-version of this paper. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP-based energy storages can be deployed in the future on the distribution grid to respond to dynamic changes in the volt-age profiles of the grid and prevent sensitive loads from voltage disturbances.

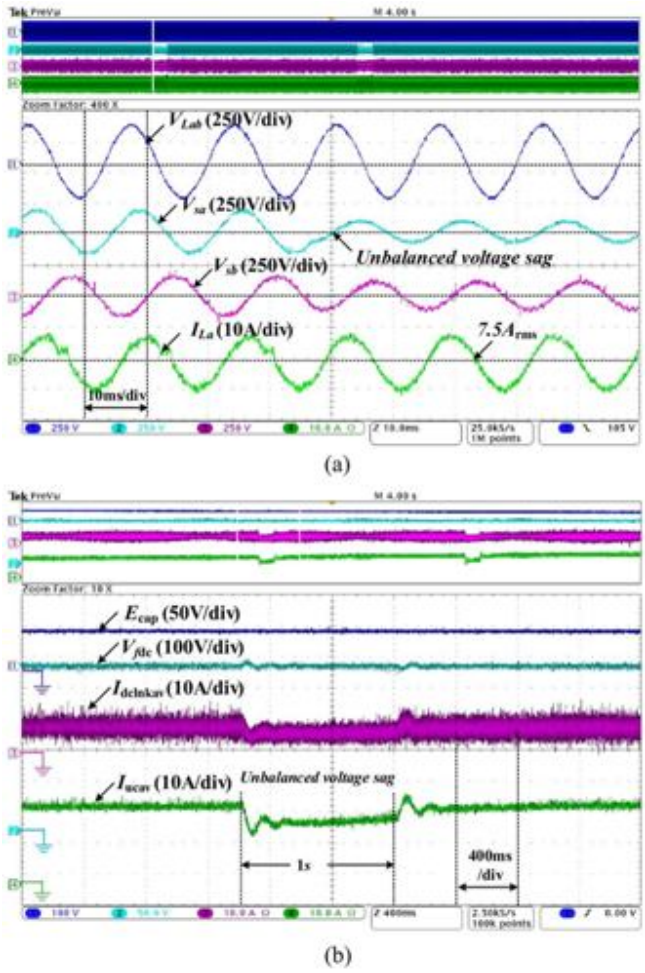


Fig. 11. (a) Inverter experimental waveforms V_{Lab} (CH1), V_{sa} (CH2), V_{sb} (CH3), and I_{La} (CH4) for during an unbalanced sag in phases *a* and *b*.
(b) Bidirectional dc–dc converter waveforms E_{cap} (CH1), $V_{f\ dc}$ (CH2),
(CH3), and I_{ucav} (CH4) showing transient response during an unbal-anced sag in phases *a* and *b*.

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