Optimal Tuning Algorithm of Turbo Decoder Applications

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Abstract- *Soft decision channel decoders are mostly used in many advanced communication receivers. The soft decisions are always denotes in the form of Log Likelihood Ratio (LLR) values, which denotes the reliability of correct decision. Among the soft decision channel decoders, Turbo codes gave a superior performance by achieving half a decibel of Shannon's Limit, thereby providing reliable data transmission use [2]concept. Hence, they find their application in a variety of cellular and wireless communication standards. A generic structure for turbo encoder is based on parallel concatenation of two Recursive Systematic Convolutional (RSC) encoders of [5]. Two identical RSC encoders produce the redundant data as parity bits. The input data stream and parity bits are combined in series to form the turbo coded word. The code structure of turbo code is formed by two constituent convolutional encoders concatenated in parallel through a pseudorandom interleaver. Two iterative decoding algorithms viz. novel Soft-Output Viterbi Algorithm (SOVA) and modified Maximum A posteriori Probability (MAP) Algorithm require complex decoding operations over several iteration cycles. All MAP decoders are based on BCJR (Bahl-cocke-Jelinek-Raviv) algorithm. It tries to minimize the code word error by maximizing the probability and also known as a maximum likelihood (ML) algorithm. MAP decoder involves extensive multiplication and logarithmic computation, which are complicated in hardware implementation.*

Keywords- Turbo decoder, LLR, RSC, MAP decoder, CF.

I. INTRODUCTION

Wireless communication is always used for high-speed data transmission over the world like audio and video, improving voice quality, and expanding broadband data services ,etc., channel decoder which employs turbo codes for error-correction delivers excellent bit- error-rate performance and it has made this code widely accepted by various wireless communication standards.

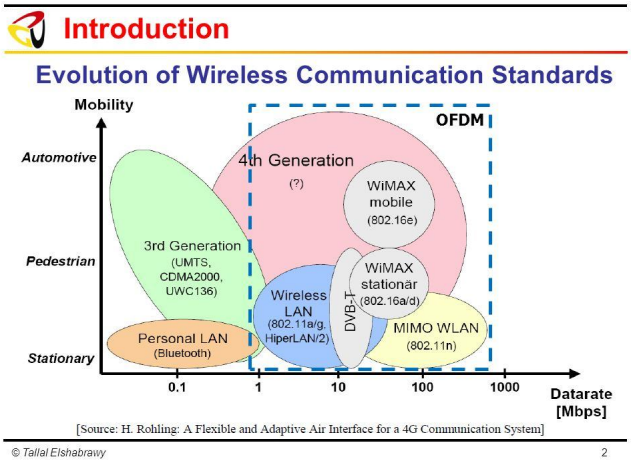

Figure 1. Wireless Communication Standards

proposes optimization based on Correction Factor (CF) approach to be applied to the extrinsic information of both inner and outer Turbo decoder. The pair of correction factors corresponding to the inner and outer decoder that gives the lowest BER for a given SNR is considered to be optimized CF pair. For optimization, a novel convolutional algorithm is proposed which can detect the sequence and has no error prior to the decoding. Thus the proposed decoding operation can reduce the probability of error.This optimized CFs reduces the overestimation of reliability values of extrinsic information and hence minimizes the BER.

II. VLSI DESIGN AND APPLICATION

VLSI - Design Methodology Front-end design procedure Turbo - decoder architecture presented in this chapter is coded with Verilog HDL (hardware descriptive language) and its functional verifications with the test-vectors of input soft-values has been carried out using SYNOP-SYS-verilog-compiler-simulator tool. Advances in VLSI technology allow hardware implementation of the transformation, so that the transform-domain LMS (least-mean-squares) algorithm will produce faster convergence of the adaptation process.

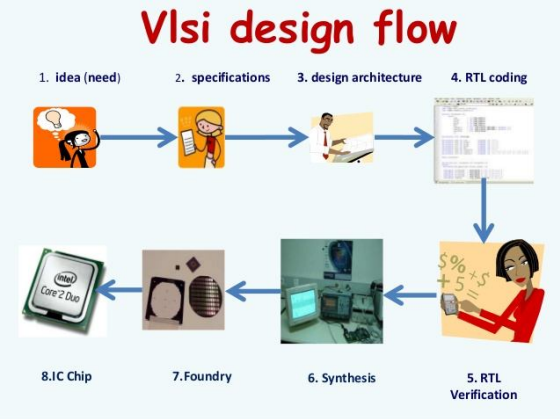

Figure 2. VLSI design flow

we propose a efficient VLSI system architecture for computing the optical flow in video sequences using the Lucas-Kanade (L-K) algorithm. The algorithm is converted into high speed RTL implementation by exploiting the inherent paralellism in the data flow graph. Clever pipelining strategies have been used throughout the design to further improve the speedup of velocity computation. We have mapped the RTL design on a Xilinx Virtex II Field Programmable Gate Arrays (FPGA) supported with Kingston DIMM DDR memory module, and a Pixel-Plus 2.0 Mega-pixel camera on the XUPV2P FPGA board. Experimental results of our proposed design showed significant improvements in accuracy with a speedup of five times when compared with other recent hardware implementations.

III. TURBO DECODER ARCHITECTURE

Optical Turbo decoder using some following applications:

SISO Architecture:

This SISO work presents radix-2 SISO-architecture for eight trellis-states(SN=8) and sliding window size of 23 (M=23) architecture that comprises of BMCbranch metrics computation) unit, BMR (branch metrics routing) unit, FSMC (for-ward state metrics computation) unit, BSMC (backward state metrics computation)unit, DBSMC (dummy backward state metrics computation) unit and LCU (LLRcom-putation unit). Here, the inputsXandXp1 are the received soft values of systematic and parity bits respectively.

The SISO units are given as;

$r_{k(Sa,Sb)}$=-L(Uk)/2-X-Xp1=-L(Uk)/2-(X+Xp1),

$r_{k(Sc,Sd)}$=-L(Uk)/2-X+Xp1=L(Uk)/2-(X-Xp1),

$r_{k(Se,Sf)}$=L(Uk)/2+X-Xp1=-L(Uk)/2+(X-Xp1),and

$r_{k(Sg,Sh)}$=L(Uk)/2+X+Xp1=-L(Uk)/2+(X+Xp1)

where,

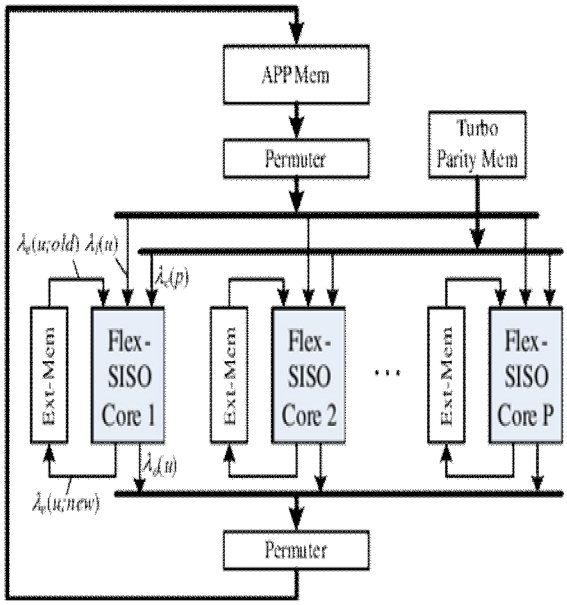

Figure 3. High level SISO architecture with turbo decoder

SISO Scheduling

FirrstSW1 (sliding window) time slot (TSW1), BMC unit computes four parent-branch metrics for each trellis stage in SW1 and these buffered parent-branch metrics (using REG1)are stored in DP-SRAMs (dual port static - random access memories).

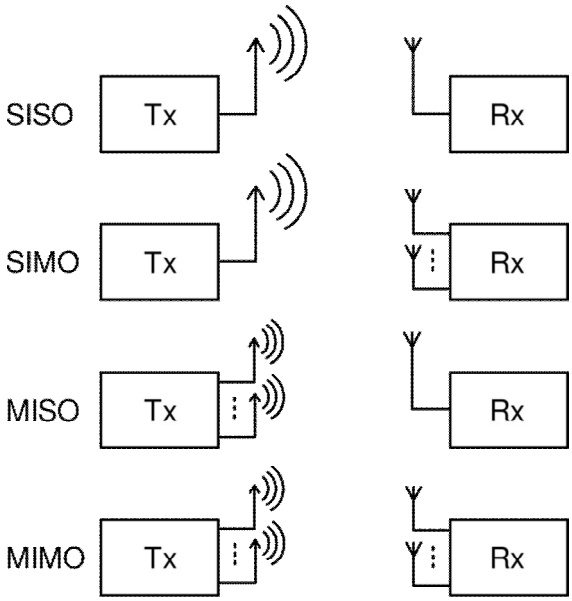

Figure 4. SISO Scheduling

Analysis of Memory Requirement:

Field programmable gate arrays (FPGA) include in addition to look-up tables, reasonably big configurable embedded memory blocks (EMB) to cater to the on-chip memory requirements of systems/applications mapped on them. While mapping applications on to such FPGAs, some of the EMBs may be left unused.

IV. MAP ALGORITHMS

Conventional logarithmic MAP algorithm uses Jacobian logarithm for computing for-ward/backward state metrics and LLR values of a-posteriori probabilities [8]. Accord-ing to Jacobian logarithm, mathematical equation involving logarithmic and exponential functions can be approximated as following figures,

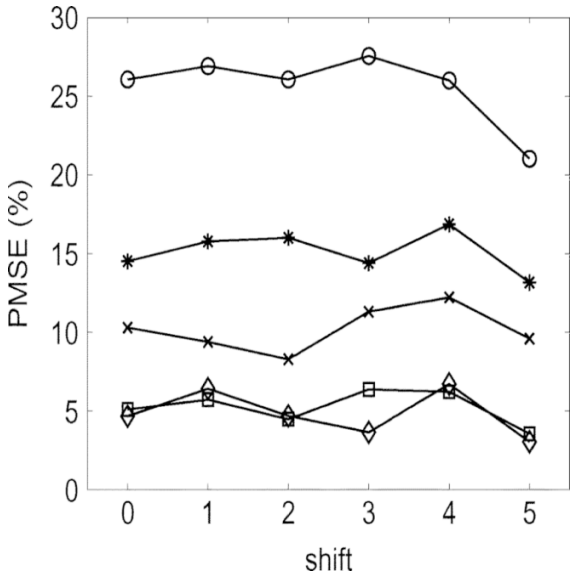

Figure 5. MAP Data

Assuming the data-width of nd; it may be concluded that both these architectures aresuitable for high speed implementations of turbo decoder.

V. HARDWARE TESTING OF MAP & TURBO DECODERS

The real hardware, we have used such FPGAs for testing the proposed MAP and turbo de-coders.

Figure 6. Hardware of MAP Decoder

The other hand, systematic procedure of building wireless-communication test-environment is an essential step for the verification of such hardware prototypes.

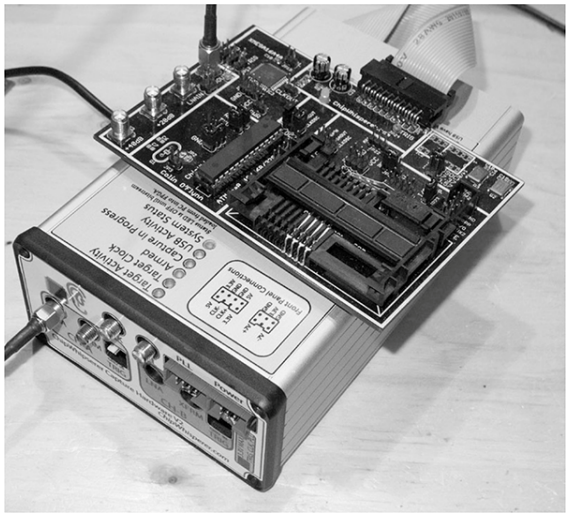

Figure 7. Testing of Turbo decoder

VI. CONCLUSION

This optimal tuning algorithm of turbo decoder applications presented a VLSI implementation of data receiver. The proposed architecture is used to reduce the delay and power. The fast decoding method can be achieved by turbo decoding approach. The combined performance of the turbo decoder along with the quick dta receiver is used to minimize the power consumption and also checking the error rate using error bit in CF(Correction Factor).

REFERENCES

[1] K.Ramya and K.Pavithradevi "Effective Wireless Communication," International Journal of Advanced Research, volume4(12),pp. 1559-1562 Dec 2016.

[2] G.Arunachalam, K.Ramya, M.Vimala, M.Shanmugapriya,C.Krishnaveni,"Future Principle of TCP High-Speed Network "International Journal for Research and development & Technology" Volume-7,Issue-2 (Feb-17) ISSN (O) :- 2349-3585

[3] Karthikeyan.R, Dr.Geetha.T ,Ramya.K ,Pavithradevi.K," A Survey on Sensor Networks", International journal for Research and Development in Technology, Volume 7,Issue 1 Jan 17.

[4] K.Ramya,G.Arunachalam,M.Shanmugapriya,P.Sathya "Mobile Computing Broadband Networks "International Journal for Research in Applied Science & Engineering Technology (IJRASET) Volume 5 Issue II, February 2017 ISSN: 2321-9653

[5] L.Gomathi, K.Ramya "Data Mining Analysis using query Formulation In Aggregation Recommendation", Volume 2 Issue 1- October 2013.

[6] R.Karthikeyan,T.Geetha, K.Ramya, K.Pavithradevi, " A Survey of Sensor Networks" , International Journal for Research & Development in Technology (IJRDT) Vol.7,Issue.1, Januray 2017.

[7] K.Pavithradevi, K.Ramya. S.Nandhini, G.Punitha, " History and Applications in Body Arear Network",International Journal for Researchin Applied Science & Engineering Technology Vol 5, Issue II, February2017.

[8] C.Ganesh,B.Sathiyabama,T.Geetha"Fast Frequent Pattern Mining Using Vertical Data Format for Knowledge Discovery" International Journal of EmergingResearch in Management and Technology",Vol 5,issue 5,2016

[9] C.Schurgers, F.Cathoor, and M.Engels (2001), " Memory optimization of MAP turbo decoder algorithms," IEEE Trans.Very Large Scale Integr.(VLSI) Syst., vol.9.no.2,pp.305-312.