Design and Analysis of Low Power Multiplexer Using Power Efficient Techniques

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Abstract- *This paper presents the design and analysis of 2:1 multiplexer is based on FinFET technology. The Conventional design of 2:1 multiplexer through which we have calculated different performance parameter like noise, leakage power, consumption, efficiency. The design of 2:1 multiplexer for this paper is work on low supply voltage therefore it is appropriate for low power application. The multiplexer is a digital device which as many inputs and single output, select line will select the input so selected input will directly move to the output. For minimizing the power in the circuit, it should be known that what the sources are which dissipate power in the designs. The leakage power consumption is expected to dominate the overall power consumption as the scaling technology for low power issues. In this paper, a MTCMOS technique is used over novel FinFET technology to reduce leakage power and power consumption etc. FinFET processes are a new development of the technology worked in FinFET technology to minimize the power consumption. In MTCMOS technique two sleep transistors are used with high threshold voltage. Sleep transistor will cut the power supply from the circuit and provide virtual Vdd and virtual ground to the circuit. The proposed design of 2:1 multiplexer works on supply voltage of 0.7V. The design and simulation of MTCMOS based 2:1 MUX is done by using 45nm technology at cadence virtuoso version 6.1 platforms.*

Keywords- MUX, noise, Leakage Power, Power Consumption, FinFET.

I. INTRODUCTION

The rapid change of VLSI design with its emerging qualities like high speed low power, increased robustness. Today's CMOS in nano-scale technology evolutionary exponential, predicted by Moore's law and has been followed apparently. The increased variability in recently used advanced CMOS technology plays a vital role to determine the total leakage of chip. . It is very difficult to achieve the required speed while meeting the power constraints, because of excessively large spread in currents. The whole design of chip, is because of large variation in leakage power as a high twenty transistor for 30% variation in its frequency. Multiplexer is a digital device, which consists of 2^n input and has n select line which is used to select the input signal which will directly move forward to the output. The multiplexer is used to send the information within the network with particular amount of time and bandwidth from selected input to output of multiplexer. Multiplexer is a device that allows a system to share multiple signals. MUX we can also use in building digital semiconductor like in central processing unit and graphic controller as programmable logic in telecommunication in computer networks and video. In this dissertation design of proposed 2:1 multiplexer is done by using different techniques like FinFET, MTCMOS, and Transmission gate to enhance the performance of the system at 45nm technology.

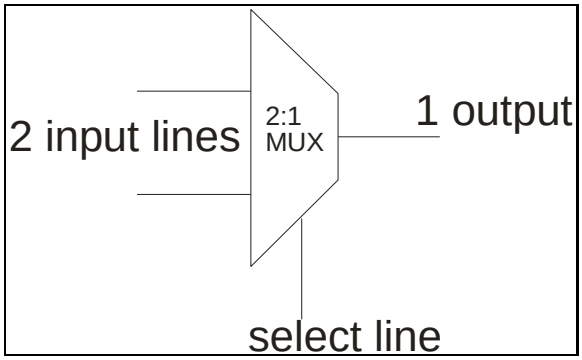


Fig.1 Block representation of 2:1 MUX

Minimizing the power in the circuit, it should be known that what the sources are which dissipate power in the designs. One of the reasons for the power dissipation is the "peak instantaneous power dissipation". During this case maximum power is drawn from the circuit which lead to the spike in the supply voltage occurs due to power line resistance. Heavy flow of current can cause glitches in the circuit which can then lead to malfunctioning of the device. The second reason is the "average power dissipation". It is highly useful for the battery operated device such as portable device etc. it will decide the lifetime of the battery. The mode of reducing the power dissipation in the circuit will lead to reducing the peak power in the device which will further will increase the reliability of the device. The power dissipation in

the recent design of VLSI circuit is the low power design of the large level of reversible circuit. The leakage power consumption in the CMOS VLSI technology due to the sub-threshold current.

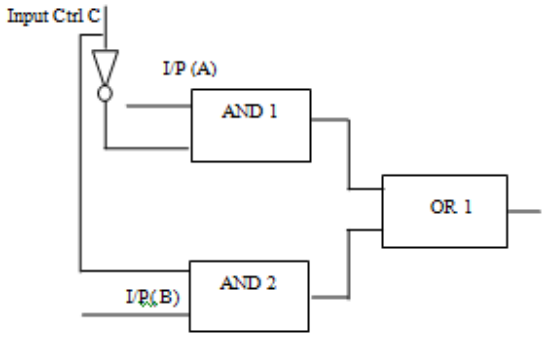


Fig.2 Block representation of 2:1 MUX Using Gates

1.1 MTCMOS TECHNIQUE

Multi-edge CMOS is also called power gating technique is one of the regularly utilized technique to diminish standby leakage power. In MTCMOS method, high-threshold-voltage (High-VTH) sleep transistor is utilized at the header and the footer of the circuit. Low-edge (Low-VTH) transistor is utilized to remove the force supply. A PMOS transistor (High-VTH) is put between the genuine Impact of Techniques in nanosclae CMOS Technology. Power line and the virtual electrical cable, a NMOS transistor (Low-VTH) is put between the real ground and the virtual ground. The power utilization of logic has quickly developed been the main impetus to change to favored decision of ICs The leakage current streaming any intelligent circuit the pile of the association of transistor is serially, lessens when more than the number of transistor of the stack is cutoff. This impact is surely understood as the stacking impact. Whenever two or more than two transistors are OFF they are stacked on top of each other. Under this condition, low measure of spillage force is disseminated than when a solitary transistor is cutoff.

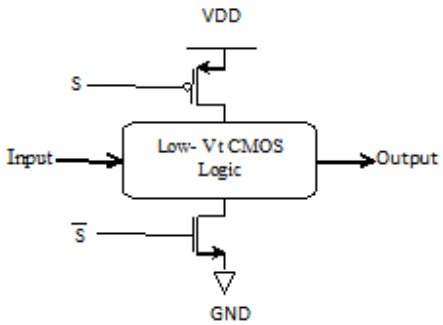


Fig.3 MTCMOS design of 2:1 MUX

1.2 FinFET TECHNIQUE

Bulk CMOS is replaced with FinFET as number of transistor is increasing day by day. FinFET are also known as double gate devices.FinFET uses Dual gate, which are diminutive for enhancing the performance and controlling leakage and reducing transistor count. The FinFET circuitry consists of a thin silicon body. With the scaling of the transistor size, CMOS transistor does not work efficiently at reduced channel length. Proper electrical control of the device is not there and it has reduced speed and high power dissipation in the circuit. It is affected with SCE (Short Channel Effects) in the device. Modern microprocessors are designed using FinFET i.e., Fin Field Effect Transistor. It is built in SOI substrate. Channel like Fin is present above the body of the transistor called as agate electrode. The use of Fin leads to use of many gate in a single transistor. The transistor designed is smaller in size, performs faster operation and consume less energy in circuit. Thus to overcome the limitations of the CMOS transistors FinFET came into existence. Nowadays, circuits are being designed in FinFET technology in order to get better output performance. The body of FinFET is made of Silicon enclosed by the gate terminal. Channel present is perpendicular to the wafer and current flows parallel to the wafer plane. Thus this device is termed as quasi planar.

II. APPLICATIONS OF MULTIPLEXER

Multiplexer is a device which split input signal into different frequency, on the basis of select line selected input signal will forward to the output. - Different combinational circuits are being designed using multiplexer. Multiplexer is a device in which many signal can share one device, in particular time and bandwidth multiplexer send data within network .A list of applications that multiplexer are being used for are

a) Logic function generator
b) Look up tables
c) Adder scale
d) Telephonic network
e) Multiplexer is used for storage of facts in memory of system
f) Transmission of data from satellite system
g) Low operating Voltage.
h) One device can share many signals.
i) Less Power Consumption.
j) We can implement much combinational circuit using MUX.

III. WORKING OF 2:1 MULTIPLEXER

In the conventional design of 2:1 multiplexer number of transistor are eight from M1 to M8 in which P-MOS are pull-up network whereas N-MOS are pull-down network.

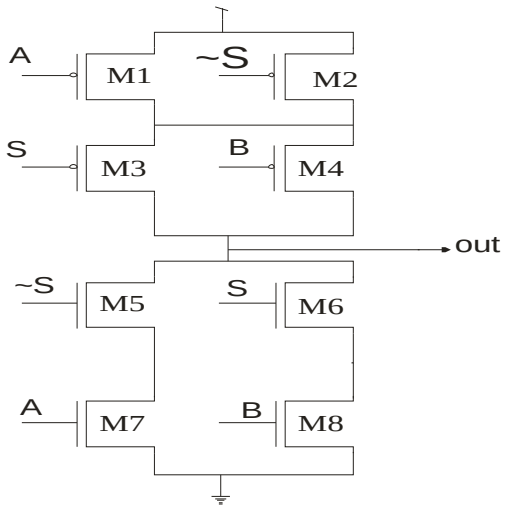


Fig.4 Conventional design of 2:1 MUX

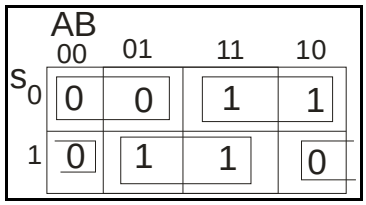
.Conventional design of 2:1 multiplexer working ,we consider two cases if s==0 else s==1.case first if we take S=0, A=0, B=1, Out=1, it means that M1 and M3 transistor will turn-on and generate one at the output of multiplexer and all other transistor of conventional design are turnoff. Second case if S=1,A=0,B=1, then M6 AND M8 transistor will turn on and all other transistor is turn off and produce zero at output .it produces zero because N-MOS always in pull-down network it produces strong zero at output.

TABLEI.TRUTH TABLE OF 2:1 MULTIPLEXER CIRCUIT

Select line	Input		Output
S	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Equation for 2:1 MUX Y=SA+~SB

K-MAP FOR 2:1 MULTIPLEXER CIRCUIT



$$PUN = \sim SA + SB \quad (1)$$

$$PDN = \sim S\sim A + S\sim B \quad (2)$$

TABLE II. REDUCED FORM OF 2:1 MULTIPLEXER TABLE

R0	S	Y
0	0	A
1	1	B

Control bit as a 1 bit number and S== 0 or S == 1,
When S == 1 or ~S== 1 (equivalently, S == 0). When one minterm is 1, the other minterms are 0.
Thus, when S == 0, we get:

Y = ~Sx0 + SB
= 1 A + 0 B
= x0

Now S == 1, we will get:

Y= ~SA + SB
= 0 A + 1 B

A MUX is a digital circuit. The important property of a multiplexer is use to send conditional data within a network with given amount of time and bandwidth from selected input to the output. Data selector in another notation for multiplexer.

IV. PROPOSED DESIGN

In proposed design of 2:1 multiplexer in which MTCMOS technique is applied over conventional design of multiplexer which is based on FinFET technology. The FinFET circuitry consists of a thin silicon body. With the scaling of the transistor size, CMOS transistor does not work efficiently at reduced channel length. Proper electrical control of the device is not there and it has reduced speed and high power dissipation in the circuit. It is affected with SCE (Short Channel Effects) in the device. Modern microprocessors are designed using FinFET i.e., Fin Field Effect Transistor. It is built in SOI substrate. Channel like Fin is present above the body of the transistor called as agate electrode. The use of Fin leads to use of many gate in a single transistor. Multi-

Threshold CMOS (MTCMOS) has risen as an extremely mainstream technique for standby mode leakage power decrease. In this method, arrangement with the power supply and the obtainable design and ground, a high-threshold voltage transistor is embedded. Actually, stand out sort of highV_{th} transistor is attractive for threshold decrease.

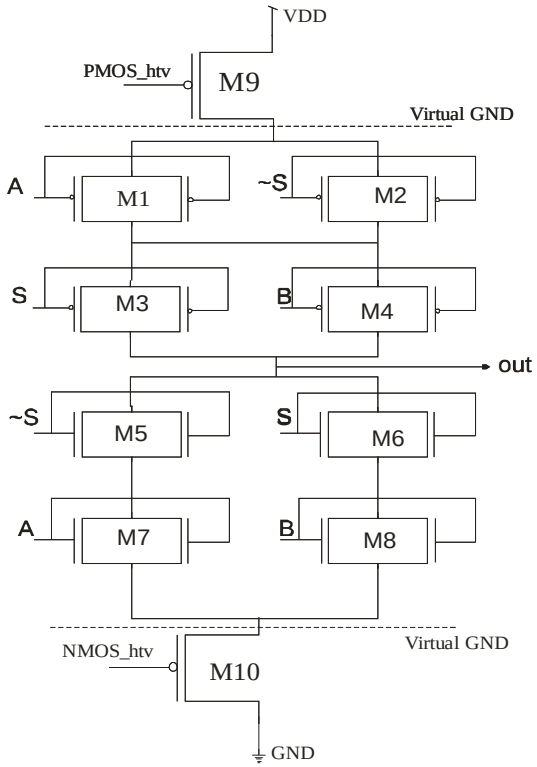


Fig. 5 Proposed design of 2:1 MUX

V. PERFORMANCE PARAMETERS

1. Power Consumption

Power consumption is the average power consume by the circuit to generate output. By decreasing the power supply from the circuit then by design power consumption of the circuit will decrease. Therefore by using MTCMOS technique the average power is reduce.

$$\text{Power (P)} = (\text{Vdd}) * (\text{Iavg}) \quad \textbf{(3)}$$

2. Leakage Power

Leakage power may be defined as unwanted sub threshold current has been introduce in the channel of transistor when the transistor is turned off .Then difference in threshold voltage . It will strongly affect leakage power. Leakage power is due to static or dynamic power. When system in working form is known as dynamic power and when system is in sleep form is called static power .By using different technique we can reduce leakage power .In this paper we have applied MTCMOS technique to reduce leakage power.

$$\text{Power (Ptotal)} = \text{Static power} + \text{Dynamic Power}$$

$$P(t) = (Vdd) * (Idd(t)) \quad \textbf{(4)}$$

3. Noise

Noise in any digital or analog circuit provide undesired output that will reduce the effectiveness of output signal and misrepresentation input signal .so undesired signal noise is created .Many technique to reduce noise from the circuit here we have apply MTCMOS based technique.

$$Sv(f) = 4kTR, \quad f \geq 0 \quad \textbf{(5)}$$

Where k is Boltzmann constant.

4. Efficiency

It is defined as the ratio of the output power consumed to the input power supplied to the circuit. Higher the efficiency better the circuit is. It is defined in percentage.
η = Output Power/Input Powers or and T is temperature

VI. SIMULATION RESULT

The data acquired regarding the parameters of CMOS based and MTCMOS based 2:1 MUX is shown in Table III.

Table III. Comparison of different parameters of 2:1 MUX

Sl. No	Parameter	FinFET based 2:1 MUX	MTCMOS based 2:1 MUX
1	Noise (V^2/Hz)	14.255p	1.221P
2	Power Consumption(W)	2.68n	1.262n
3	Leakage Power(W)	16.89p	6.1p
4	EFFICIENCY (%)	74	89.4

The graph of the FinFET and MTCMOS based 2:1 MUX parameters are calculated in Table III and the comparison graph is shown in Fig. 8 which tells us that there is reduction in every performance degrading parameter studied above and we get a better output performance using MTCMOS.

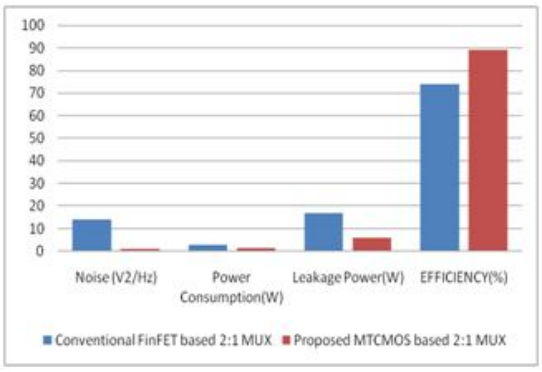


Fig. 6: Comparison graph of parameters

OUTPUT GRAPH

1. The output of 2:1 MUX is shown in Fig7.

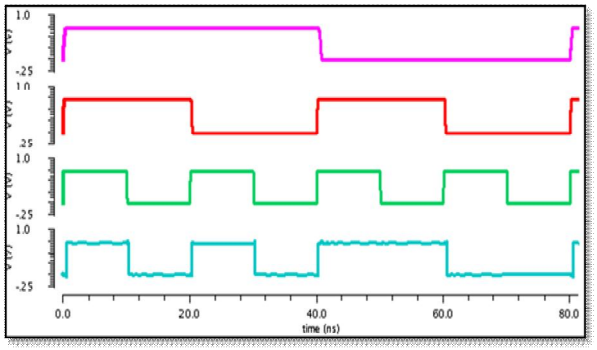


Fig.7: Output of 2:1 MUX

2. Leakage power is depicted in Fig9. Leakage power in the circuit reduces with the proposed design.

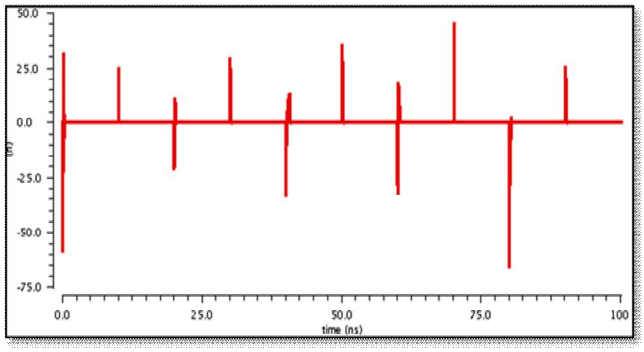


Fig.8: Leakage Power

3. Power consumption is depicted in Fig. 10. Power consumption in the circuit reduces with the proposed design.

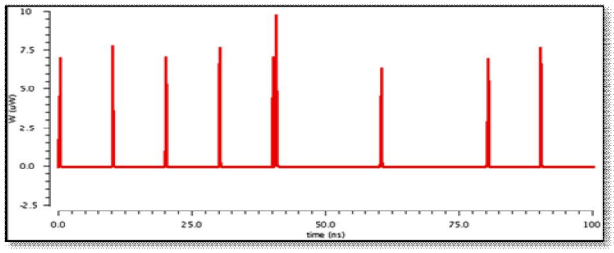


Fig. 9: Power consumption

VII. CONCLUSION

In this paper we successfully implemented Multiplier using MTCMOS based technique over FinFET technology. In MTCMOS two sleep transistors are used with high threshold voltage. Thus, result and simulation are measured in table III .The analysis and simulation of the desired circuit is done with supply voltage of 0.7 V. By using MTCMOS based design we reduced such parameter like leakage power and power consumption i.e. 6.1. And 1.262 form 16.81 and 2.68 respectively is been observed which will increase the efficiency of your. The efficiency of the circuit is increased from 74% to 89.4% are also being observed.

VIII. ACKNOWLEDGEMENT

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