Design & Analysis of CMOS Direct Conversion Receiver For Wireless Applications

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Abstract- *- A compact direct conversion receiver (DCR) front-end has been realized in CMOS process technology. Compared to other prior pieces of work, this very receiver design achieves the high gain without an output buffer, high linearity, low noise, low power consumption. The proposed system has demonstrated the behaviour for the high data rate wireless communication system. While mobile broadband systems may not be feasible, there are still promising applications for WLANs, WPANs etc. to take the advantage of the large bandwidth offered the antenna parameters and transceiver characteristics. Importantly, ultra-low-power direct conversion receivers with high gain and low noise figure are desired for the CMOS technologies based wireless communication systems. It has also been observed that the values of noise figure, power dissipation should be low for the optimum performance of the same. Direct conversion exhibits potential for compact, low power Radio Frequency implementation devices. The present work will be very useful for the design of a simple and low cost chip solution for multi-gigabit wireless communication applications.*

Keywords- Direct Conversion Receiver, CMOS, Gain, Linearity, Noise Figure, Wireless Communication System, Radio Frequency

I. INTRODUCTION

Recent studies have indicated a promising technology i.e.; deep scaled CMOS technology to reach th4 cost effective monolithic solutions for cloud computing (Wi-Gig), ultra-high throughput WLAN (IEEE 802.11 AD) and Video Data Streaming (Wireless HD). The receiver sensitivity must be raised with gain, low noise and high linearity in order to resolve high order modulation for more efficient bandwidth utilization and distant communication range [1]. The 7 GHz of unlicensed band around 60 GHz has spurred intense research activities in low power, low cost and highly integrated circuits for applications in various spheres. The low noise and high linearity performance must not be realized at the cost of power overhead for portable or mobile systems. Resultantly, a low noise, high linearity and low power consumption and dissipation device design is highly desirable [2].

Also, recent advances in Si-Ge, CMOS and Bi-CMOS technologies and continued progress in various III-V technologies have made it possible to build low cost radio receivers operating at millimeter wave frequencies including the 57-64 GHz ISM (Industrial, Scientific and Medical) band. The wide bandwidth available at such frequencies makes possible multi Gb/s data transmission using a range of modulation techniques and formats from non-coherent amplitude shift keying (ASK) to complex orthogonal frequency division multiplexing. The attractive combination of low cost radio frequency ICs, small antenna designs and high data rates has sparked a variety of potential applications such as wireless personal area networks (WPANs), wireless docking for portable devices and wireless uncompressed digital video transmission. The unlicensed band around 60 GHz offers the possibility of short range communication at high data rates. The anticipated complexity of transceivers designed for operation in this very band makes the use of CMOS technology attractive especially if techniques such as beam forming, multiple input multiple output etc. signaling are considered. In today's world, development of 60 GHz CMOS transceiver is reminiscent of the challenges that faced 5 GHz CMOS wireless LNA circuits in the 90s. The intrinsic speed of the erstwhile available transistors was not adequate and not commercially viable [3].

II. COMMUNICATION SYSTEMS

Most computing devices today require some kind of wireless functionality and with rise of portable electronics this trend will only increase. A need for better, efficient and more reliable signals comes with this increase which in turn has cleared a way for the use and design of different wireless data transmission methods. Digital communication is one of the most commonly used ways to implement data transfers over long distances. The figure below shows a rudimentary block diagram of a digital radio communication system which usually consists of a transmitter, channel and receiver. The digital radio signal experiences many transformations in its migration from baseband signal at the transmitter to its replication at the receiver. The system level diagram displays the symmetry of the digital radio. The receiver can be considered a reverse implementation of the transmitter.

Resultantly, the measurement challenges are similar for both parts of the digital radio system. Though, unique problems exist at the various locations in the system since the modern day receivers and transmitters face different design problems. The receiver has correction and synchronization schemes to help clear and decipher noise contaminated and time delayed signals [4].

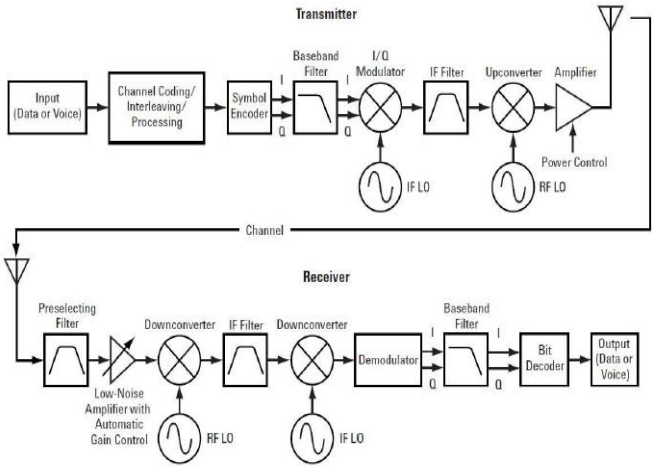

Figure 1. Block diagram of Conversion receiver [5]

However, both the issues will be resolved soon if 60 GHz transceivers follow the path of 5 GHz counterparts. The Challenges faced by 60 GHz front-end designs in super scaled CMOS are attributed to some of the major reasons which are as follows: the inherent capacity nature of CMOS diminishes device gain at high frequency and the continual lowering supply voltage required by low power digital circuit shrinks voltage headroom and thus degrades the gain and linearity in RF CMOS [6].

The aforementioned problem can be solved by using horizontal cascade topology. The coupling between consecutive stages raises other design issues e.g.; DC coupling requires bias levelling circuitry between the stages which often induces additional parasitic and degrades circuit high frequency performance. The capacitive coupling not only constrains the bandwidth but also consumes large area. The introduction of an on-chip transformer enabled horizontal structure which relaxes the headroom problem and helps accomplish high gain and high linearity for low power operation. A 60 GHz direct conversion receiver front-end CMOS is implemented to verify the feasibility [7].

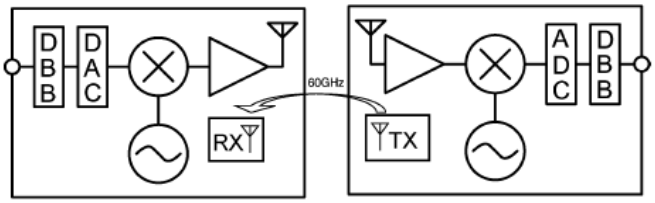

Figure 2. CMOS IC with on-chip antenna [8]

Recently, with the exponential advancement in the area of scaling of CMOS technology, it has become feasible to realize millimeter wave integrated circuits (MMICs) for high data rate wireless communication systems. It is very important to design low phase noise MMIC oscillator. Although, loss from silicon substrate and metal interconnects is high in the millimeter wave region. Electrical-Magnetic (EM) wave based oscillators have been studied to improvise the existing factor. The generally employed standing wave based oscillator increases the co-planar strip-line resonators by forming an open circuit load when the incident and reflected EM waves perfectly move in-phase with each other.

There are limitations of this approach as well. First, the open circuit condition is tough to achieve due to loss in the CPS line and second, dimensions are large when implementing CPS lines on-chip. A number of pieces of work have been proposed of late for design of a transmission line loaded high metamaterial resonator at the PCB scale. Placing additional floating metal shielding to form slow wave lines may alleviate the said issues [9].

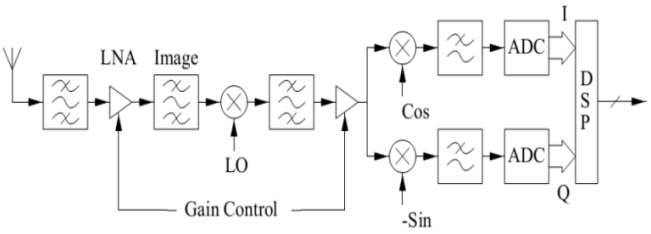

Figure 3. Diagram of a super-heterodyne receiver

A super-heterodyne receiver, also known as two-stage conversion, is basically composed of two blocks of mixers that down-converts signals from RF to IF in the first stage and from IF to baseband in the second stage as shown in the figure below. Different filters with different technologies and specifications are needed to select the RF channel or for image rejection. The super-heterodyne receiver offers superior sensitivity, selectivity and frequency stability. It provides better stability as compared to tuned radio frequency receiver because a tunable oscillator is more easily realized than a tunable amplifier.

III. SYSTEM DESIGN & DISCUSSIONS

The high data rate communication technology leveraging the unlicensed spectrum is almost ready for deployment with several demonstrations of successful wireless links. One of the key aspect of the transceiver is the ability to handle analog fractional bandwidths in the order of 20%, challenging for both the linear processing chain and the frequency reference generator. In classical LC loaded stages bandwidth trades with gain making them unsuitable for wide band amplifiers at millimeter waves where the available device gain is relatively low [10].

In this piece of work, the author has exploited inter stage coupling realizing higher order filters where wider bandwidth is achieved at the expense of in-band gain ripple only. The receiver adopts a sliding IF architecture employing an integer-N type-II synthesizer with a three state phase frequency detector charge pump combination, a switched tuned LC VCO followed by a low power wide range divider chain. By judicious choice of charge pump current and filter components integrated phase noise, critical for signal constellation integrity at high rate is kept low. This paper clearly inspects the inter-state coupling technique providing design formulas and discusses the design of each receiver block [11].

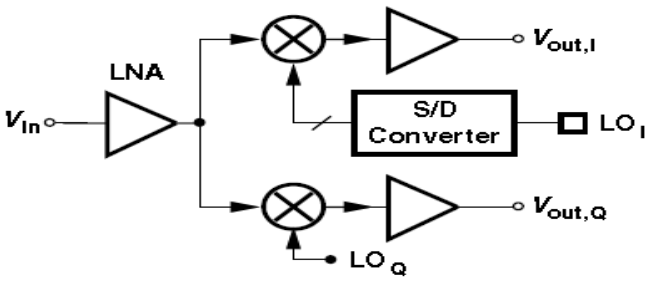

Figure 4. General Receiver architecture [8]

The outcome of the research effort in the design ok Ka band and mm wave silicon ICs has motivated several industrial projects toward the realization of chipsets for broadband communications and automotive cruise control applications. Performance of standard CMOS implementations have proved sufficient up to 60 GHz range and examples of operating blocks even beyond 60 GHz have been presented. Still, the choice of the receiver architecture entails several peculiar considerations in order to achieve a robust low power solution. Frequency conversion to DC has been used in most cases to allow a high level of integration in CMOS [12].

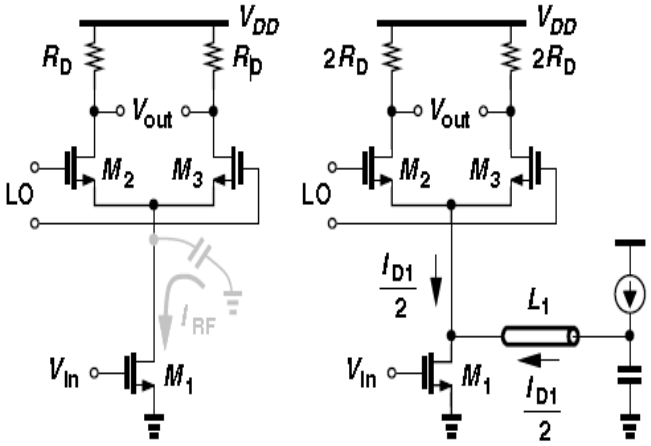

Figure 5. Conventional and proposed mixer topologies [8]

On the other hand, it is desirable to synthesize a reference frequency that is lower than the received frequency at high frequencies to save power in both the VCO and dividers. A multiplier following the synthesizer can be used but this prevents I/Q down conversion, mandating a further IF processing stage. Moreover, leakage between signal and LO ports, exacerbated at high frequency, determines off-set, inter-modulation distortion and LO deleterious for example in automotive radars [13].

IV. DESIGN ISSUES & SOLUTIONS

There are many design issues concerning the realization of CMOS 60 GHz receiver RF front-ends. Attention should be paid to the given issues to reduce design time and power consumption of the receiver. The amplifier is composed of an nMOS device and short stubs for input matching and output load matching circuit. These short stubs act as inductors and their impedance is controlled by the length of stub. Thus, parasitic parameters should be estimated neatly using may be electromagnetic simulator or must be modelled using the test device.

Therefore, the simulation and estimation must be done with the exact pattern of these nodes and the bonding wires should too be simulated in case of packaged RFICs. For low noise, the amplifier needs to have a high amplification in its first stage. Input and output matching circuits for narrow-band circuits enhance the gain. Using an LNA, the effect of noise from subsequent stages of the receiver chain is reduced by the gain of the LNA while the noise of the LNA itself is injected directly into the received signal. The input noise of the following stages e.g., amplifiers and filters, is thus still critical. Since, the down-converted spectrum is located around zero frequency, the 1/f noise of device has a profound effect on the signal, a severe problem in MOS implementation [14].

The other issue is of the need for large LO signal for mixer. The transmission lines are used as stubs or phase rotator for impedance matching. Since the input or output impedance of these circuits is tuned to the characteristic impedance of the transmission line, the interconnection of these circuits is achieved by simple connection of transmission line. Thus, the impedance matching between these circuits is preferable for flexibility of the placements of these circuits. However, these T-line have resistive loss due to the sheet resistance of the metal and LO signal amplitude should be large to drive the mixer. Such an LO output buffer requires large current and causes unwanted large LO signal emission [15].

V. RESULTS & ANALYSIS

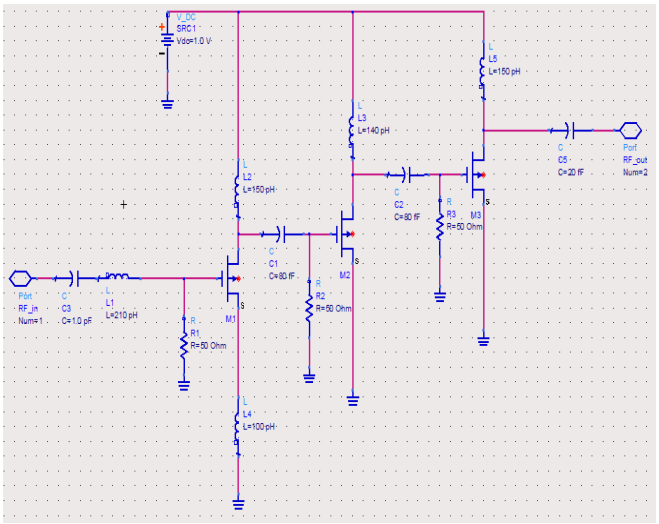

Figure 6: Design of an LNA

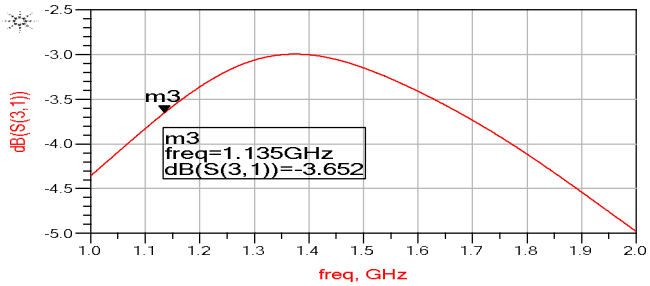

Figure 7: Rectangular Plot between S31 and Frequency

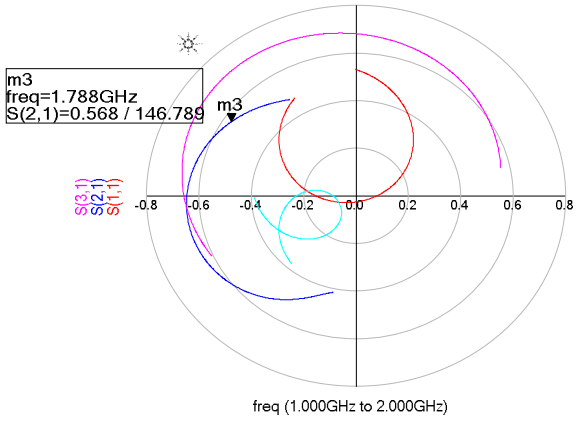

Figure 8: Polar Plot between S31 and Frequency

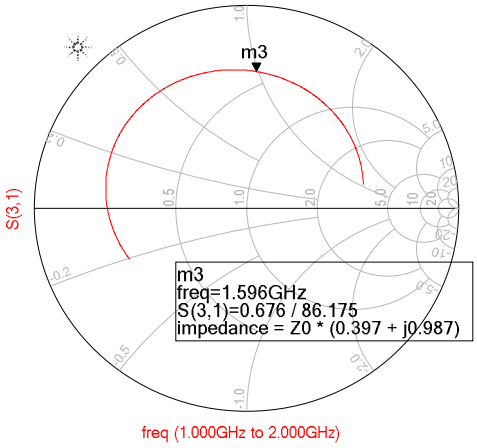

Figure 9: Smith Chart between S31 and Frequency

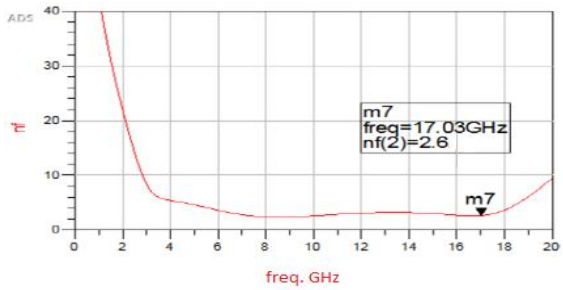

Figure 10: Noise figure of the system design

VI. CONCLUSION

The compact design of the receiver offers high gain and high linearity, low noise and low power dissipation and consumption through signal headroom and optimized impedance matching while compared with earlier CMOS process technologies. Emerging applications for the high bandwidth unlicensed spectrum include extremely high data rate short range communication systems. Many of these applications are expected to enter the realm of consumer

electronics where low cost and mass production are prerequisites, favoring the application of digital CMOS technology. High data rate communication technology leveraging the unlicensed spectrum around 60 GHz is almost ready for deployment with several demonstrations of successful wireless links. In classical LC loaded stages bandwidth trades off with gain making them unsuitable for wideband amplifiers at mm-wave where the available device gain is relatively low.

A highly integrated receiver front-end is demonstrated that is manufactured in a digital CMOS process using a design approach amenable to mass production. Unlike many previous attempts in CMOS technology, the results of the design are well predicted by the simulation results by matching the desired frequency band and simulated gain to a very high accuracy. The low noise and high gain are demonstrated with low power consumption. These factors make the front-end suitable for small footprint mobile applications such as a cell phone or laptop computer.

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