Low Phase Noise Eight Phase Voltage Control Oscillator Using Series Transister Coupling

Monika Patidar[1], Vinod Sonkar[2], Deepak Sharma [3]
Department of EC
[1, 2, 3]SDBCT,Indore

Abstract-*An ultra-low-voltage and back-gate-coupled 8-phase LC-VCO for beam forming satellite receivers has been proposed .This thesis presented eight phase voltage controlled oscillator using series transistor coupling which consists of two quadrature voltage controlled oscillator(QVCO). Each QVCO has LC selective frequency tank with one NMOS and one PMOS with it. Eight Phase was obtained by connecting output of one QVCO to the another QVCO. Low phase noise have been obtained by increasing number of finger of NMOS and PMOS, LC filter circuit is added at the end of source of NMOS block and finally, substrate of NMOS is connected to 0.8 V. Whole circuit is designed and simulated on ADS software using 65 nm technology. Phase noise of -97 dBc/Hz at 1 MHz offset is obtained for 33.3-54.85 GHz carrier frequency. With 0.7 V of supply, this design consume only 1.228 mW. Since FOM is dependent on phase noise, -186.55 dBc/Hz is achieved with tuning range of 21.5 GHz.*

I. INTRODUCTION

The voltage-controlled oscillator (VCO) is an essential building block of all wireless and wireline communication systems. Especially, a poly-phase local oscillator (LO) signal provided by the VCO supports a wide variety of transceivers with image-rejection [28], harmonic-rejection [29] and phased-array beamforming [30] capabilities. This paper proposes an ultra-low-voltage 8-phase LC-ring VCO which is suitable for 10GHz beam forming satellite receivers.

The design of a high-frequency 8-phase VCO is non-trivial and frequency division is a common practice to achieve it. A differential VCO followed by a div-by-4 circuit can generate the desired 8-phase LO, with the schematic presented in Fig. 1(a). However, the VCO must operate at a frequency 4 times higher than the output (i.e., 40GHz), significantly penalizing the power and tuning range. A possible alternative is depicted in Fig. 1(b), where four differential LC-ring VCO cells are coupled to construct an 8-phase VCO. This scheme has the advantage of excellent phase noise, at the expense of power and chip area.

Within the nanoscale CMOS environment, the high fT of MOS devices allows operation in the moderate inversion region for GHz-range applications, resulting in substantial power savings. Specifically, when a 0.5V supply is adopted, the MOSFET can be considered as a four terminal device without the risk of forward bias the substrate p-n junctions. The body can be properly biased to reduce the threshold voltage (VT) [31], thus serving as the direct coupling terminal of multiple VCOs to synthesize a poly-phase LO. Another power-reduction technique can be implemented by modifying the typical cross-coupled pair from purely NMOS or PMOS, to a PMOS-NMOS hybrid topology. As a result, the number of current paths will be halved from 8 to 4 for an 8-phase VCO. Together with the use of a minimized 0.5V supply, the power efficiency of this work would be strongly improved (i.e., 0.25mW per LO-phase at 10GHz).

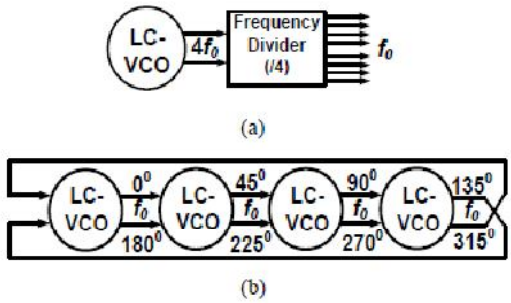

Fig. 1 8-phase LO generation by: (a) one LC-VCO followed by divide-by-4. (b) Direct coupling of four LC-VCOs.

II. LITERATURE SURVEY

Xiang Yi and his friends [32] designed fully integrated 60 GHz frequency synthesizer with an in-phase injection-coupled quadrature voltage-controlled oscillator (IPIC-QVCO). Through a particular symmetrical coupling network formed by diode-connected transistors, the in-phase coupling is realized in the IPIC-QVCO, which reduces both phase noise and phase error.

Jiaqi Shen[24] designed QVCO for radar application achived phase noise of -76 dBc/Hz at 1 MHz.

Md.Tawfiq Amin and his friends[33] direct-back-gate coupling method, featuring independent sizing of coupling strength and frequency tuning, while avoiding the risk of forward bias the substrate p-n junctions. Optimized in 65nm CMOS, the 8-phase VCO draws only 2mW.

Chihun Lee and his friends[27] designed 37-38.5GHz octave-phase clock generator. An octave-phase *LC* voltage-controlled oscillator and the split-load divider are presented. The proposed PD improves the static phase error and enhances the gain. The clock generator has been fabricated in 0.13um.

Marc Tiebout[34] describes the design and optimization of voltage controlled oscillators with quadrature outputs. Systematic design of fully integrated *LC*-VCOs with a high inductance tank leads to a cross-coupled double core *LC*-VCO as the optimal solution in terms of power consumption. Futhermore, a novel fully differential frequency tuning concept is introduced to ease high integration.

Yu-Ching Tsai and hi friends[35] designed a novel quadrature voltage controlled oscillator (QVCO) using current-reused tech-nique and back-gate coupling . The QVCO realized with LC-tank is demonstrated in a 0.18um RF CMOS 1P6M process. Using the current-reused technique efficiently reduces the power dissipation. However, by stacking switching transistors in series like a cascade, the architecture cannot perform well in phase noise. Through an improved circuit schematic with back-gate coupling, the phase noise of the circuit can be lowered. As a result of reducing four transistors in the circuit, the total power dissipation can be cut down even more.

Khaled Khalaf[23] described the design of a receiver front-end circuit for operation in the 60GHz range in 90nm CMOS.The QVCO predicts 56.8-64.8GHz tuning range from schematic simulations.

III. DESIGN

The schematic of the QVCO[4] is presented in Fig. 2. The QVCO consists of two negative resistance LC oscillators, and they are coupled with each other by using four transistors (*Ma*,*Mb*, *Mc* and *Md*).

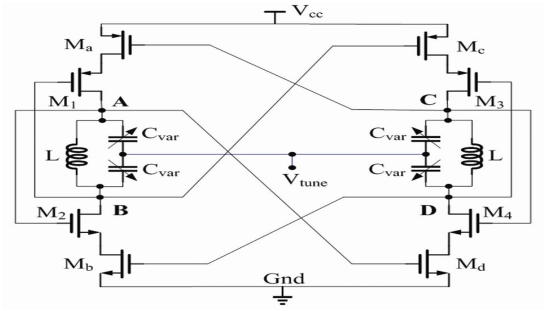

Fig. 2 Schematic of Conventional design

The proposed 8 phase VCO consists of two QVCO in which output of QVCO is connected to the input of another QVCO. Each QVCO consists of two negative resistance LC oscillators which consists of two transistors (one NMOS transistors and one PMOS transistors) and a LC frequency selective tank, and each LC oscillator are coupled with each other by using four transistors. NMOS at the bottom are body bias .Each transistor except in LC oscillator have number of finger of 5.Finally LC tank is added at source end of NMOS transistor which is reducing phase noise more in addition to the two NMOS and two PMOS added previously. The values of NMOS and PMOS adjusted to obtain the better results.

Measurement of frequency

The frequency of CMOS LC VCO design can be calculated by transient response as show in Fig.2. For frequency calculation, time period (dx) is directly read by oscillation as show in Fig.2 which is equal to 30 ps at 0V and Vb=0.8 V. The relation between frequency and time is given below

$$F = \frac{1}{T}$$

In the above expression T is time period of oscillation. The time period of oscillation T is equal to dx. Substituting the value of time in above equation frequency comes out to be,

$$F = \frac{1}{30\,ps}$$

$$F = 33.3\,GHz$$

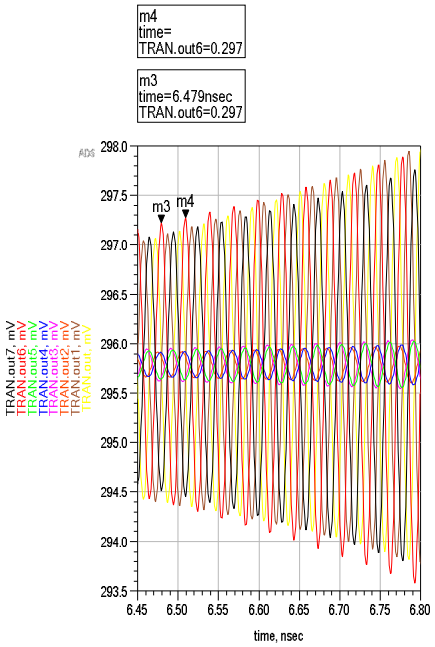

Fig.3 Transient Response of LC VCO.

Measurement of tuning range

The fractional tuning range of LC VCO design can be calculated by plotting graph between control voltages and frequencies as show in Fig. 3 by transient analysis.

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0} \times 100$$

By the graph is clear that $f_{max}$and f_{min} is 54.85GHz and 33.3 GHz where f_0 is 33 GHz

Power Consumption

The power consumption of VCO can be calculated by formula given below

$$\max d.c.\ power\ dissipation = V_{supply} I_{bias}$$

It gives total power consumed by the integrated parts in the circuit. The power consumed by this VCO is 1.228 mW.

IV. RESULT

Tabulation of Parameters extracted

Table 1
Results of CMOS LC VCO.

S.No.	Parameter	Simulation result
1.	Technology	65nm
2.	Power Consumption(mW)	1.228
3.	Frequency(GHz)	33.3-54.85
4.	Tuning Voltage(V)	0.0-1.0
5.	Tuning Range (%)	21.5
6.	Phase Noise(dBc/Hz)	-97@1MHz, 33.3-54.85 GHz
7.	FOM(dBc/Hz)	-186

Phase Noise & FOM

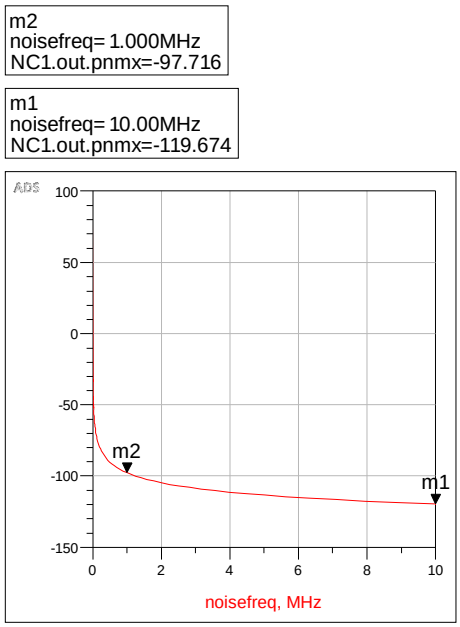

Fig.4Phase Noise at 33.3 GHz-54.85 GHz when Vtune=0.0-1.0 V at Vb=0.8 V

Fig. 4 shows that the phase noise at an offset of 1MHz and 10 MHz is -97 dBc/Hz and -119 dBc/Hz at 33.3 GHz-54.85 GHz.FOM of the proposed VCO is -186.55 dBc/Hz at 33.3 GHz-54.85 GHz at 1MHz offset.

Comparative study of results

Table 2

S.No.	Parameter	Ref. [23]	Ref. [24]	Ref. [25]	Ref. [26]	Ref.[27]	**This work**
1.	Technology (nm)	90	130 SiGe BiC MOS	65	65	130	**65**
2.	Supply Voltage (V)	1	2.5	1.0	1.2	1.2	**0.7**
3.	Power Consumption (mW)	91.7	28	24	15.6-30	51.6	**1.228**
4.	Frequency (GHz)	55.4-61.7	53-59	51.7 - 56.6	48.8-62.3	37-38.5	**33.3-54.85**
5.	Tuning Voltage(V)	0.5-1.0	0.5-2.3	-	-	0-1.6	**0.0-1.0**
6.	Tuning Range(GHz)	8	6	4.9	13.5	1.5	**21.5**
7.	Phase Noise(dBc/Hz)	-97.4@ 1 MHz	-88@ 1 MHz	-95 @1 MHz	-88 to -96@1 MHz	-88.67 @ 1MHz	**-97@1MHz**
8.	FOM(dBc/Hz)	-	-171.1	-179	-173	-	**-186.55**

V.CONCLUSION

A CMOS LC VCO is designed in 65nm CMOS process for high frequency application. This design is simulated on ADS software. In this design,two QVCO are connected with output of one is connected to input of another.Each QVCO is having LC oscillator with NMOS and PMOS in between PMOS and NMOS block.NMOS block at the bottom are body bias at 0.8 V which gives better phase noise. Finally LC filter circuit used at the source of NMOS block. All this gives 8-phase output which is novel technology for upcoming devices. This 8 phase VCO works between 33.3 GHz-54.85 GHz frequency with control voltage from 0.0 to 1.0V and bias voltage of 0.8 V which helps in reducing power consumption. This design has power consumption of 1.228 mW.

REFERENCES

[1] Purushothama Chary P, Rizwan Shaik Peerla, Sesha Sairam Regulagadda, Mohd Abdul Naseeb,Amit Acharyya, Rajalaksmi P, Debashis Mandal and Ashudeb Dutta, "0.8 V 450 _W 2.4 GHz PLL using Back-Gate QVCO for ZigBee/BLE standard in 0.18 µm CMOS", IEEE, 2016.

[2] Guang Zhu, Shengxi Diao, Fujiang Lin and Daniel Guidotti, "A Low-Power Wide-Band 20GHz VCO in 65nm CMOS", Global Symposium on Millimeter Waves,2012.

[3] Qiuzhen Wan, Yaneng Liu1 and Qingdi Wang, "A CMOS Back-Gate Coupling LC Quadrature VCO with Switched Self-Biasing Tail Transistor Technique", Circuits Syst Signal Process, March, 2015.

[4] Jie Jin, "Novel quadrature voltage controlled oscillator using series transistors coupling", Indian Journal of Pure & Applied Physics Vol. 54, December 2016, pp. 765-770.

[5] M.Moghavvemi and AliyarAttaran"Performance Review of High-Quality-Factor, Low-Noise, and Wideband Radio-Frequency LC-VCO for Wireless Communication [Application Notes]",Microwave Magazine, vol. 12, pp. 130-146, June 2011.

[6] Mohammad Niaboli-Guilani, Dalenda Ben Issa, AbdennaceurKachouri and MounirSamet, "A Low Power Low Phase Noise CMOS Voltage Controlled Oscillator", 17th International Conference Electronics, Circuits, and Systems (ICECS), pp. 422 – 425, Dec. 2010.

[7] Alex Katz, OfirDegani, YosiShacham-Diamandand EranSocher, "A beyond 60GHzCross-Coupled Fundamental VCO in 45nm CMOS", in IEEE InternationalConference on Microwaves, Communications, Antennas and Electronics Systems, pp. 1-5, Nov. 2009.

[8] Nabil Boughanmi,Dalenda ben issa, Abdennaceurkachouri andMounirsamet"HighQ-VCO with Low phase noise for Communications applications",in the International, Design and Test of Integrated Systems in Nanoscale Technology, Conference, pp. 370- 373, 2007.

[9] Ali Fad, Tord Johnson, Martin Linder and Denny Biberg "A Comparative Study ofCMOS LC VCO Topologies for Wide-Band Multi-Standard Transceivers",The 47th IEEE International Midwest Symposium on Circuits and Systems, pp. 17-20 July 2004.

[10] Jie Long and Robert J. Weber, "A 2.4GHz Low-Power Low-Phase-Noise CMOSVCO Using Spiral Inductors and Junction Varactors", in Proceedings of the 2004International Symposium on Circuits and Systems , Vol.4, pp. 545-548, 23-26 May2004.

[11] S. Levantino, C. Samori, A. Bonfanti, S.L.J. Gierkink and A.L. Lacaitai, "Frequencydependence on bias current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise up conversion", IEEE J. of Solid-State Circuits, vol. 37, pp. 1003-1011, Aug. 2002.

[12] BehzadRazavi, Design of Analog CMOS Integrated Circuits, Tata McGraw hill ed.,2002.

[13] JakubKucera and Bernd-Ulrich Klepser, "3.6 GHz VCOs for multi-band GSMtransceivers", in Proceedings of the 27th European Solid-State Circuits Conference,pp. 325-328, 18-20 September 2001.

[14] A. Hajimiri and T. H. Lee, "Jitter and Phase noise in ring oscillators", IEEE J. Solid State Circuits, 34(6):790-804, June 1999.

[15] Ali Hajimiri and Thomas H. Lee,"Phase Noise in CMOS Differential LC Oscillators", 1998 Symposium onVLSI Circuits-Digest of Technical Papers, pp. 48-51, Jun. 1998.

[16] Yongwang Ding and Ramesh Harjani, "Introduction," High-Linearity CMOS RFfront-end circuit, New York, NY, Springer, 2005.

[17] R. Saeidi, N. Masoumi, F. Kalantari and M. S. Oskooei,"Analyzing of Phase Noisein CMOS LC Oscillators" in the 17th International Conference on Microelectronics (ICM), pp. 330-337, Dec. 2005.

[18] Sherif Mohamed, MauritsOrtmanns, and YiannosManoli "Design of Current Reuse CMOS LC-VCO", IEEE, 2008.

[19] MrunaliniNandanwar and Deepak Dandekar, "High Performance VCO for Low Power RF Transmitter-A Review", the National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012), pp. 22-25, 2012.

[20] Jongsuk Lee and Yong Moon, "A W-band VCO using center-tapped basic inductor in 65 nm CMOS".

[21] Kwok K, Long J R. A 23-to-29 GHz transconductor-tuned VCO MMIC in 0.13 um CMOS. IEEE J Solid-State Circuits, 2007

[22] Ioannis Zographopoulos, Fotis Plessas, Emmanouil A. Antonopoulos and Fotis Foukalas, "A 16-nm FinFET 16-GHz Differential LC-VCO", IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems(COMCAS 2015), 2 – 4 November 2015.

[23] Khaled Khalaf, "60GHz receiver front-end chain in 90nm CMOS technology",Thesis, DELFT UNIVERSITY OF TECHNOLOGY ,August 2010.

[24] Jiaqi Shen,"60GHz Quadrature Voltage-Controlled Oscillator for Radar Application", Thesis, DELFT UNIVERSITY OF TECHNOLOGY, August 2010.

[25] Tianzuo Xi,Shita Guo,Ping Gui,Jing Zhang,Kenneth K. O,Yanli Fa,Daquan Huang, Richard Gu, and Mark Morgan, "Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS Process", IEEE Radio Frequency Integrated Circuits Symposium, 2014.

[26] Liang Wu and Howard C. Luong, "A 49-to-62 GHz Quadrature VCO With BimodalEnhanced-Magnetic-Tuning Technique", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, 2014.

[27] Chihun Lee, Lan-Cho Chou and Shen-Iuan Liu, Chun-Lin Ko*, Ying-Zong Juang*, Chin-Fong Chiu, "A 1.2V 37-38.5GHz 8-phase Clock Generator in 0.13um CMOS Technology", Symposium on VLSI Circuits Digest of Technical Papers, 2006.

[28] S. L. J. Gierkink, S. Levantino, R. C. Frye, C. Samori, and V. Boccuzzi,"A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling," IEEE J. Solid-State Circuits, vol. 38, pp. 1148–1154, Jul. 2003.

[29] M. Soer, E. Klumperink, B. Nauta, F. E. van Vliet, "Spatial Interferer Rejection in a 4-Element Beamforming Receiver Frontend with a Switched-Capacitor Vector Modulator", IEEE J. Solid-State Circuits, vol.46, no.12, pp.2933-2942, Dec. 2011.

[30] S. Patnaik, N. Lanka, and R. Harjani, "A dual-mode architecture for a phased-array receiver based on injection locking in 0.13 μm CMOS," in IEEE ISSCC Dig. Tech. Papers, Feb. 2009, pp. 490–491.

[31] S. Chatterjee, Y. Tsividis, P. Kinget, "0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design," IEEE J. Solid-State Circuits, vol. 40, No. 12, pp. 2373-2387, Dec. 2005.

[32] Xiang Yi, Chirn Chye Boon, Hang Liu, Jia Fu Lin,and Wei Meng Lim, "A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer With In-Phase Injection-Coupled QVCO in65 nm CMOS Technology", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 49, no. 2, February 2014.

[33] Md.Tawfiq Amin, Pui-In Mak and Rui P. Martins, " A 0.5V 10GHz 8-Phase LC-VCO Combining Current-Reuse and Back-Gate-Coupling techniques Consuming 2mW", IEEE,2013.

[34] Marc Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 36, no. 7, July 2001.

[35] Yu-Ching Tsai, Yi-Shing Shen, and Christina. F. Jou, "A Low-power Quadrature VCO Using Current-reused Technique and Back-gate Coupling", PIERS ONLINE, Vol. 3, no. 7, 2007.