Multistandard LNA With High Gain, Low Noise Figure Using 32 Nm Technology

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Abstract*-Low noise amplifier is an important component of many receivers placed after RF filter. It is used to reduce the noise level of the received signal ,amplify it and send it to the next stage .The parameters on the basis of which many LNA are differentiate are noise figure,gain,S-parameter,third intercept point,1dB compression point and power consumption.*

Various architecture have been adopted to this component of which cascode topology found to be better candidate for LNA. Since technology are advances very rapidly, multistandard LNA took place of the single standard LNA. All the parameters are dependent on each other.

This thesis based on designing of multistandard LNA for GSM,UMTS and WLAN802.11b band. This LNA consist of resistive feedback amplifier followed by cascode stage with body bias. Various band selected on the basis of capacitive switching. Inductor at the gate of bottom transistor and inductor in between of cascode transistor is added and body is biased by 1V.

Better results have been obtain with help above changes. Whole circuit designed on ADS software using 32 nm technology.

I. INTRODUCTION

For years, LNA has been the topic of research due to its different performance requirements for different standards [5-13]. Gain, NF, linearity, and low power consumption are the major specifications in the design of LNA, and the most importantparameter is NF. To achieve a low NF, common source stage with inductive degeneration showed the best noise performance with good gain and sufficient linearity with a trade-off with power consumption [5-7]. Several techniques and methods have been tried in order to produce a LNA with low NF [5-13], but, most of these methods and techniques are limited to the single standards only.

However, due to the high demand of multi-standard device, the trend of LNA design seems to move from single-standard to multi-standard LNA, with different methods andtopologies as appears in literatures [14-19]. The most popular technology nowadays used to implement LNA is complementary metal oxide semiconductor (CMOS) technology which offers low power consumption and low cost solution.

II. LITERATURE SURVEY

AbdelkaderTaibi and his friends[21] presents a low power and high linear reconfigurable CMOS low noise amplifier for wireless multistandard applications including GSM (PCS1900), 3G (UMTS),Bluetooth and WLAN b/g. Based on inductive degenerated cascade topology, this LNA achieves a good trade-off between high gain, noise figure and power consumption. The input and output matching networks include controlled MOS-varactor devices to select the desired bands for multi-standard purpose.

AnishazielaAzizan and his friends[22] use forward body bias technique with cascode configuration in order to implement a suitable LNA for low power consumption target.

SaeidYasami[23] designed forward body biasing technique in current folded architecture, so that the LNA is biased in subthreshold region with supply voltage of 350 mV and DC current consumption of 503 uA.

NajeemullaBaig[24] observed that the main trade-off is between Noise Figure and the size of inductor.

AwatifHashim[25]worked on the design of a fully integrated 0.13-mm CMOS multi-standard power constrained simultaneous noise and input matching low-noise amplifier (PCSNIM LNA). The multi-standard capability is obtained via the implementation of CMOS switches. The input and output matching are fully implemented on a chip, which is uncommon when compared to the existing multistandard LNA topologies. The multi-standard LNA is operated at 0.9, 1.8, and 2.1 GHz frequencies. The design covered wireless standards of GSM900, DCS1800, and W-CDMA applications.

Liu Baohong[26] implement multi-gigahertz cascode CMOS LNA for low power wireless communication. By splitting the direct current through conventional cascode topology, the constraint of stacking-MOS structure for supply voltage has been removed and based on forward-body-bias technology, the circuit can operate at 0.5 V supply voltage.

Srigayathri.y[27] designed multiband Low Noise Amplifier (LNA) for receiver system to work at 950 MHz,GHz, 2.2 GHz, and 2.4 GHz centre frequencies. It was designed using HJ-FET NE32500 transistor which has self bias characteristics.

AbdelhalimSlimane[28] presents a design of a low power single ended CMOS LNA for reconfigurable applications including GPS, GSM (DCS1800, PCS1900), 3G (UMTS), WLAN b/g and LTE. Based on a wideband input matching, the LNA stages cover all band of interest while achieving a good trade-off between high gain, low noise figure and low power consumption. For multi-standard aim, the LNA selects the desired bands usinga high output resonant impedance with a switching technique.

AmraFathima[29] added inductor at the source of bottom to increase noise factor and stability.

III. DESIGN

Fig. 3.1 shows the schematic of proposed multi-standard LNA.

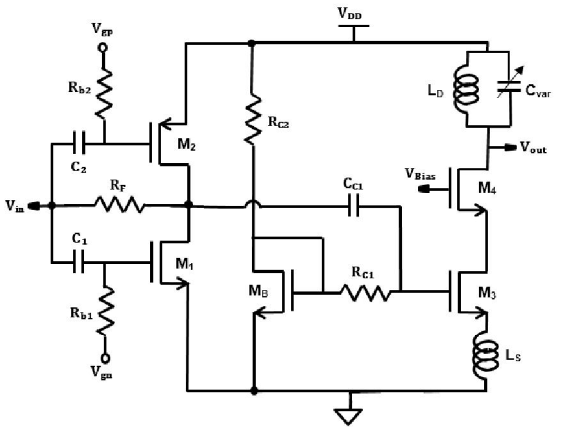


Fig. 3.1 Schematic of Multi-Standard LNA

In addition to the above circuit arrangement , two inductor have been added to increase noise figure and S-parameter.LM is connected at the middle of both the transistor and Lg is connected at the gate of M3.The design equations of proposed multi-standard LNA is shown in[28] and the design is based on the forward body bias technique[22] because the transistors canoperate under a lowsupply voltage, which is one of the effective ways to consume less power . Besides, this technique could be employed with simplicity so as to minimize the size and cost. The gain will decrease when the supply voltage is low.

The proposed design(figure 3.2) have been simulated in Advanced Design Software(ADS) using 32 nm technology.

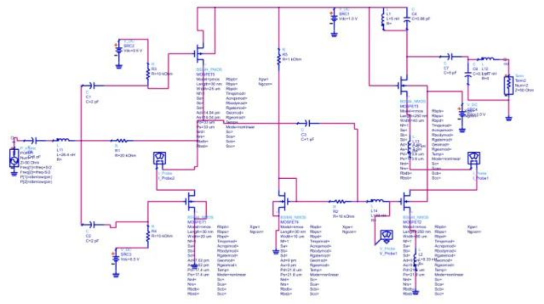


Fig.3.2 Multistandrad LNA on ADS software

This circuit consist of resistive feedback topology with input matching network followed by cascode topology with output matching network. The resistive feedback network consists of two MOSFET'S,PMOS at upside and NMOS at downside. Two bias resistor is conneted at the gate of both the transistors and a resistor is connected between input and output of resistive feedback circuit.Two capacitors are also connected at the gate's of MOSFET. The input matching network consist of capacitor in series with a inductor.Both bias resistor is connected with bias voltage. The cascode topology consist of two NMOS with a inductor between them. One inductor is connected at the gate of bottom transistor and one inductor is connected at the source of the same transistor.An inductor is connected in parallel with capacitor above the top MOSFET. Bias circuit is designed to bias the bottom transistor.this circuit consist of two resistor and a NMOS transistor. Coupling capacitor is connected between output of previous stage and at the gate inductor of following stage. A bias voltage is also connected to the substrate of cascode topology transistor. Output matching network is connected at the output of cascaded stage which consist of two capacitor's and a inductor. Finally forward body bias technique is used where body of both NMOS transistor of cascode stage is tied to 1.0 V. In this circuit, inductor of input matching network and capacitor at cascode stage have been varied to obtain result's for various band's.

IV. RESULT

4.1 Stability

The system should be unconditionally stable and K>2. As the graph(figure 4.1) shows that the stability for various frequency is greater than 2 and it is unconditionally stable. The value for 1.9 GHz is 4.563, for 2.1 GHz is 8.463 and for 2.4 GHz is 22.763.

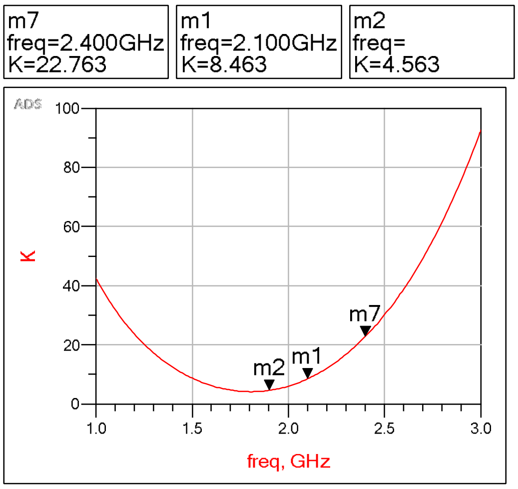
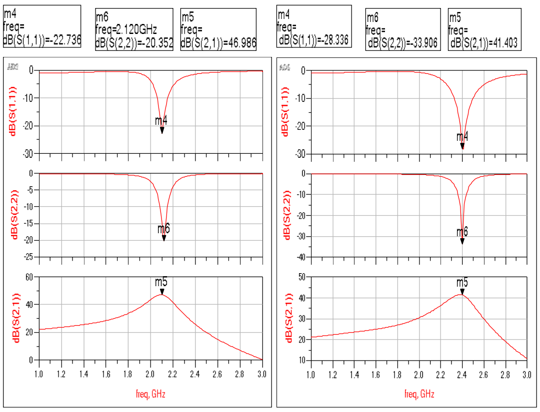


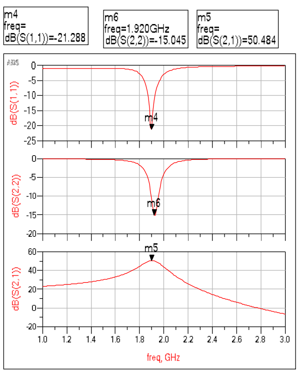
Fig.4.1 Stability plot

4.2 S-parameter

Figure 4.2 shown below are the values of S11,S22 and S21 for 1.9 GHz,2.1 GHz and 2.4 GHz .



(a) **(b)**



(c)

Fig.4.2 S-parameter for (a) 2.4 GHz (b) 2.1 GHz (c) 1.9 GHz

Gain(dB(S(2,1))) for 1.9 GHz,2.1 Ghz and 2.4 GHz is 50.484 dB,46.986 dB and 41.403 dB.

4.3 Noise Figure

The noise figure(figure 4.3) for 1.9 GHz is 1.299 dB, for 2.1 GHz is 1.308 dB and for 2.4 GHz is 1.335 dB .This values indicate that this multistandard LNA is best suited for any receiver because it has very less noise figure.

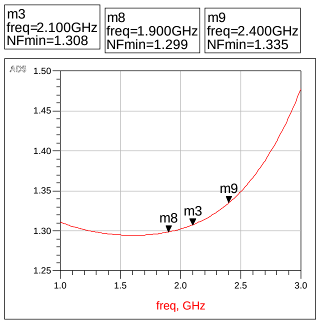
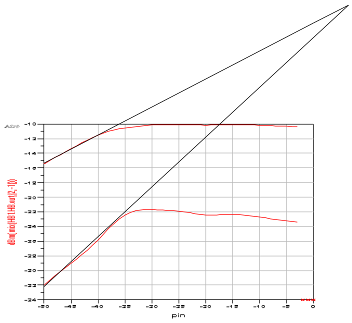


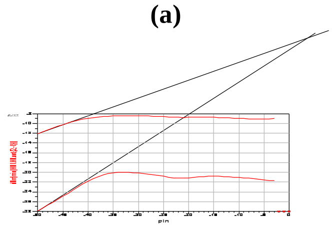
Fig.4.3 Noise figure analysis

4.4 IIP3

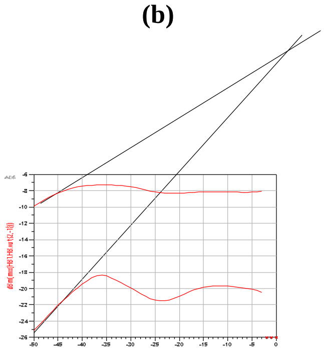
IIP3 for 2.4 GHz (figure 4.4)is 7 dBm, for 2.1 GHz (figure 5.6) is 5 dBm and for 1.9 GHz is 2 dBm.



(a)



(b)



(c)

Fig. 4.4 IIP3 for (a) 2.4 GHz (b) 2.1 GHz (c) 1.9 GHz

4.5 COMPARATIVE ANAYLSIS

Table 4.1
Comparison of LNA.

Ref.	Standard	Freq. (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	S11/S22(dB)	Supply(V)	PDC(mW)
[21]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	21 22 23.5	2.45 2.45 2.7	-3 -0.273 1.45	-	1.8	10.9
[38]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	19 20 21	2.290 2.3 2.4	-	-12.4/-12.41 -15.1/-15.21 -11.1/-11.1	1.8	32.8
[31]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	10 11 13	7 6 7	-1	-15/-15 -23/-24 -12/-23	1.5	10.5
[25]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	12 10.26 11	1.8 1.85 3	-12 -11 -10	-14.5/-24 -11.6/-37.9 -10/-40	1.2	7.4
[27]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	20 19 17.734	0.009 0.011 0.011	-	-10/- -2/- -1/,-	1.8	-
[39]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	20 -35 19.150	0.019 0.038 0.020	-	-10.064/- -10.765/- -10.5/-	1.8	-
[22]	WLAN802.11b	2.4	9.86	5.11	-7.5	-18/-15	0.5	0.3
[3]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	31 32 33	2.2 2.2 2.2	-17 -18 -18	-22/-27 -21/-17 -13/-24	1.2	7.5
[28]	GSM UMTS WLAN802.11b	1.9 2.1 2.4	31.5 35 38.4	3.78 3.79 3.86	-30.075 -30.413 -30.267	-1.3/- -1.3/- -1.3/-	1	6.2
This work	**GSM UMTS WLAN802.11b**	**1.9 2.1 2.4**	**50.484 46.986 41.403**	**1.299 1.308 1.335**	**2 5 7**	**-21.29/-15.04 -22.73/-20.35 -28.33/-33.90**	**1**	**18**

V. CONCLUSION

Multistandard LNA is designed for GSM,UMTS and WLAN802.11b. The capacitive switching is used to select various band as well as inductor at gate is added at the bottom transistor. Middle inductor is also added to achive better noise figure and stability. Body bias technique is used to reduce power consumption by connecting Vb of 1 V at body of cascode transistors. Whole circuit is designed and simulated in ADS software using 32 nm technology.

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