A Discontinuous PWM Method For Balancing The Neutral Point Voltage In Three-Level Inverter-Fed Variable Frequency Drives

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Abstract- *The paper describes a new discontinuous carrier based pulse width modulation (PWM) method for use in variable frequency drives (VFD) driven by three-level inverters. The method introduces three different switching patterns for the full range of operating speeds. Depending on the actual operating speed, the proposed algorithm is developed to select the most suitable PWM switching pattern that improves the VFD performance. This results in low imbalance in the dc-link capacitor voltage, and low current distortions without increasing switching losses. Theory, simulation, and experimental results are presented.*

Keywords- Discontinuous pulse width modulation, energy saving, neutral point clamped(NPC), neutral point (NP) voltage, pulse width modulation (PWM), three-level inverter, variable frequency drives (VFD).

I. INTRODUCTION

Due to the growing worldwide awareness of environmental problems, better electric power efficiency is sought. The industry relies heavily on variable frequency drives (VFD) that need power conversion for their operation. The energy conversion for VFDs is critical particularly for high-power applications where minimization of energy losses is important. The overall VFDs losses represent losses in the motor in addition to losses in the power converter. The latter are mainly due to the switching losses of the semiconductor devices. In large capacity applications, the switching losses represent a significant amount of wasted energy. Hence, need for reducing these switching losses.

Three-level inverters, also called neutral point clamped (NPC) inverters, have been widely used for large capacity VFDs due to their high input voltage and to the small harmonic components of their output current [1]–[3]. Various pulse width modulation (PWM) methods for three-level inverter control have been described [4]. It is well known that NPC inverters as their name implies, are based on clamping the output to neutral point (NP). Their operation principle is based on the assumption that the NP voltage, Vo,is held at zero permanently. However, in practice, this NP voltage varies especially at low-frequency operation.

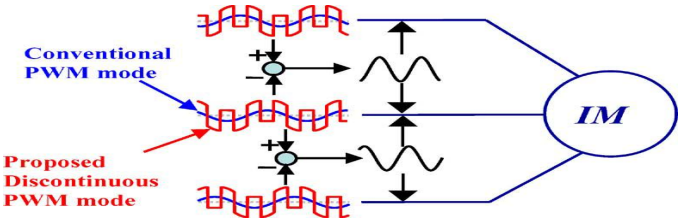


Fig. 1. Principle of discontinuous PWM method.

This may lead to instability of the PWM inverter even with balanced load. Most of these techniques resolve the NP voltage balancing problem, but increase the switching losses. A new PWM is presented to guarantee dc-link voltage balancing and describes a PWM technique to reduce the common mode or NP voltage in three-level inverter. A modified sinusoidal pulse width modulation (SPWM) method of injecting an NP voltage to the reference signals in order to control the dc-link voltage was reported in.

In this paper, a new method based on a discontinuous PWM method is proposed for three-level inverters in order to reduce the NP voltage fluctuations without increasing the switching losses. The proposed method has been applied in for compensation of MOSFET minimum ON–OFF pulse width limitation. However, in this paper, the method is adapted and customized for balancing the NP voltage for three level inverters employing any switching devices. The method is based on the principle of keeping the output line-to-line voltages unchanged while changing the phase voltages input to the motor.

II. NEUTRAL POINT BALANCING ANALYSIS

For high power/high voltage applications, the three-level inverter, shown as a functional block diagram in Fig. 2, has advantages such that the blocking voltage of each switch

is clamped to the half of the dc-link voltage, *Vd* , and the output voltage and current waveforms contain low harmonics when compared to the conventional two-level inverter operating with the same switching frequency.

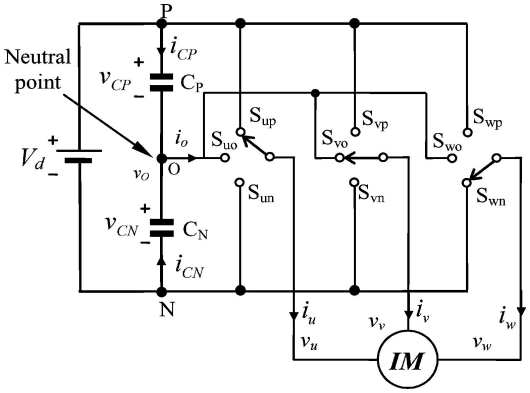


Fig. 2. Functional block diagram of three level inverter driving an induction motor.

A. Neutral Point Balancing Analysis

Two capacitors, *CP* and *CN* , are connected in series to obtain the midpoint that provides the zero voltage at the output or the NP of the three-level inverter. The NP voltage will deviate from its implicit zero level if a current flows from the inverter bridge into the capacitor midpoint. Maintaining the voltage balance between the capacitors is important and influences the control strategy. The midpoint of dc bus capacitors can be connected to the inverter bridge (in practice, it is connected to the inverter bridge circuit through clamp diodes as will be shown later). The flow of current through this NP causes voltage imbalance between the upper and lower capacitors, *CP* and *CN* .

There are several switching cases in the three-level inverter. Some of these switching states can cause voltage imbalance between capacitors. When one or two motor terminals are connected to the dc midpoint and the remaining is (are) connected to either the positive or negative rail, the dc balancing problem may occur. At this switching state [i.e., Fig. 3(a) and (c)], the capacitor *CP* is discharged while *CN* is charged. In this case, the midpoint current does flow causing capacitor voltage imbalance. This can be controlled by choosing an appropriate switching combination from those that produce the same motor voltage but cause the capacitor current to flow in the opposite direction [i.e., Fig. 3(b) and (d)]. Other cases (such as when one or two motor terminals are connected to *P*, and the remaining is (are) connected to *N*)

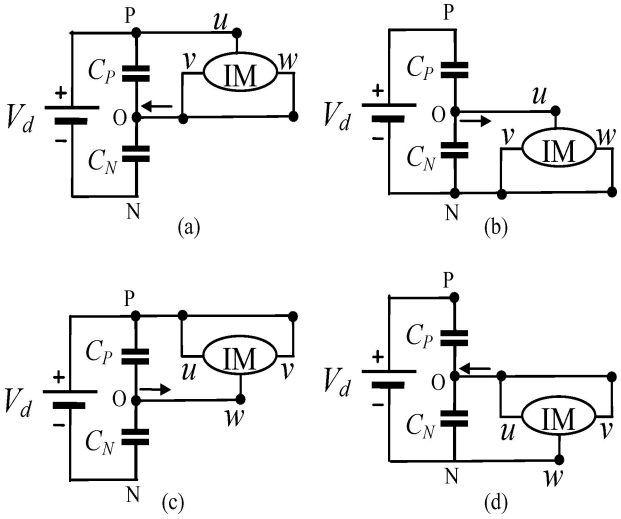


Fig 3 Neutral point current polarity.

Connections (a) and (b) of Fig. 3 provide the motor withthe same line-to-line voltage and current under a given operating condition. The midpoint currents however have opposite directions to each other. Therefore, the capacitor voltage balancing can be realized by choosing appropriately from (a) or (b). Connections of (c) and (d) have similar relations to (a) and (b) with regard to the midpoint voltage and motor current.

Under normal operation, the mean current drawn from the NP over a modulation cycle is zero and the average NP potential remains constant. At certain operating conditions, this balancing of the dc-link voltage degrades at very low operating frequencies and may lead to instability of the drive system. In these cases of low frequencies, the imbalance between the upper and lower dc-link voltages may be serious for ac drives. The output voltage of the inverter, in the presence of this unbalance, is seriously distorted as compared to the balanced one and harmonics of second order may appear that cause serious problems in ac drives such as current harmonics, torque ripples, and power losses .

B. PWM Control of NPC Inverter

The practical three-level inverter is shown in Fig. 5, and the principle of its control is shown in Table I. For the leg of the phase *u*, the main switches are *Su*1 and *Su*4 ,while *Su*2 and *Su*3 are auxiliary switches and along with *Du*2 and *Du*3 are used to clamp the output terminal potential, *vu* , to the NP potential. The auxiliary switches *Su*2 and *Su*3 are driven complementary to the main switches *Su*4 and *Su*1 , respectively. As a result, three levels of output potentials are possible. This paper will focus on carrier-based PWM techniques, this is because carrier-based PWM offers various advantages: it is easily implemented in analog or digital

circuitry, or numerically (using software techniques); it is easily extendable to all multilevel converter topologies; it shows good performance at moderate switching frequencies; it has good dynamic performance; and it is suitable for closed-loop control. Also, the understanding of the application of carrier-based modulation to multilevel converters leads easily to an understanding of the requirements for and problems of multilevel modulation using other techniques.

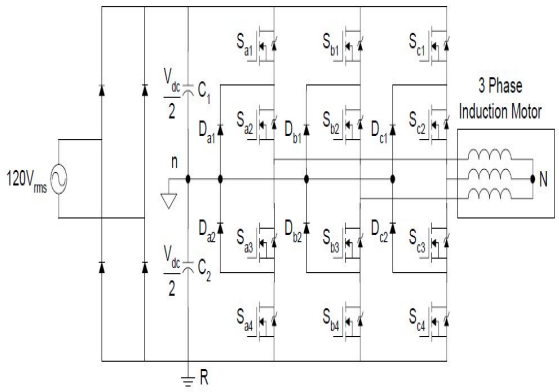


Fig. 4 Three level inverter with MOSFET as switch

C. Neutral Point Compensation Techniques

Several authors have proposed techniques to control the unbalance of the dc-link voltage of the multilevel converters. These techniques can be summarized into three categories as shown

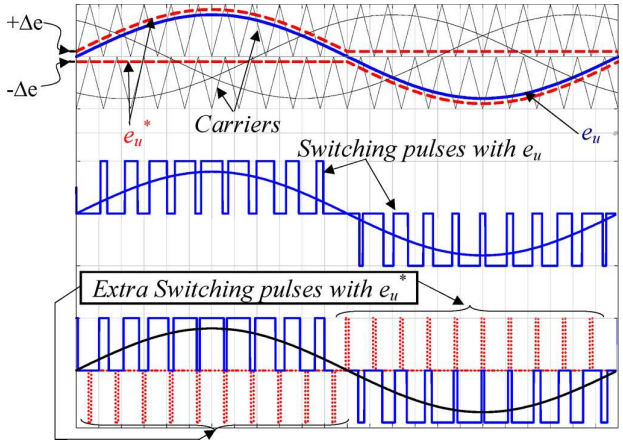


Fig. 5. Conventional method of minimum ON-pulse compensation.

Fig. 5. The principle behind the closed-loop version of these control techniques is that if a variation in the NP voltage is detected by measuring a difference between the two capacitor voltages, the controller acts in response to reduce this difference.

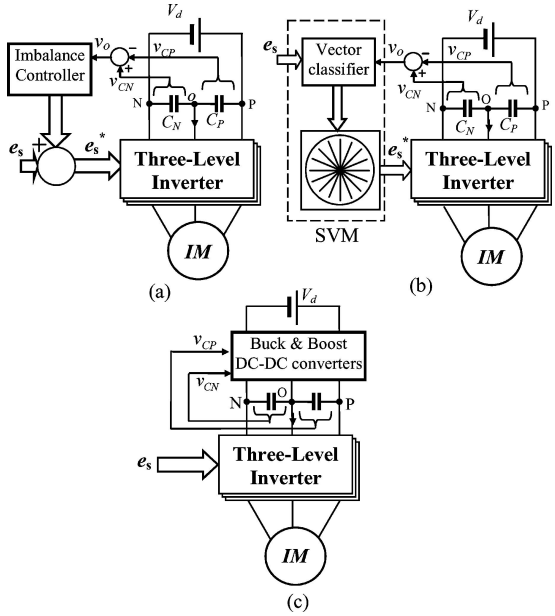


Fig. 6. Conventional methods for NP voltage compensation.

In Fig. 6, the controller reacts to the voltage unbalance by:

1) Introducing a dc offset to the reference values in carrier
   based PWM, Fig. 8(a);
2) Modifying the duration of voltage vector in space vector method, Fig. 8(b); and
3) Controlling two dc–dc choppers to keep the positive and negative capacitor voltages balanced, Fig. 8(c).

The first two methods use no extra hardware, but may increase the switching losses [35].However, the third one needs two more dc–dc converters that increase the cost of the whole converter.

III. PRINCIPLE OF THE PROPOSED METHOD

To solve the problem of dc-link voltage unbalance, without increasing the switching losses, a switching pattern PWM method is used. Fig. 9 depicts this technique, which modifies the reference voltage by selecting a suitable pattern that guarantees both motor performance and dc capacitor voltage balance. This PWM technique control of the GTO-based three-level inverter takes into account the minimum conduction time needed to dissipate capacitive energy of the snubber circuit. So, the selected switching pattern method compensates for the minimum ONpulse effect of the switching device and reduces the NP voltage unbalance without increasing the switching losses of the PWM inverter

The method is based on the principle of keeping the output line-to-line voltages unchanged while guaranteeing control pulses larger than the minimum ON pulse. The switching pattern depends on the level of reference voltages delivered by the controller, *er* = (*eu*, *ev* , *ew*).

Let the minimum voltage be the voltage generating a pulse whose width is exactly equal to the minimum ON time of the GTO. The minimum voltage reference, Δ*e*, is calculated, using minimum ON-time Δ*T*min and triangular carrier frequency

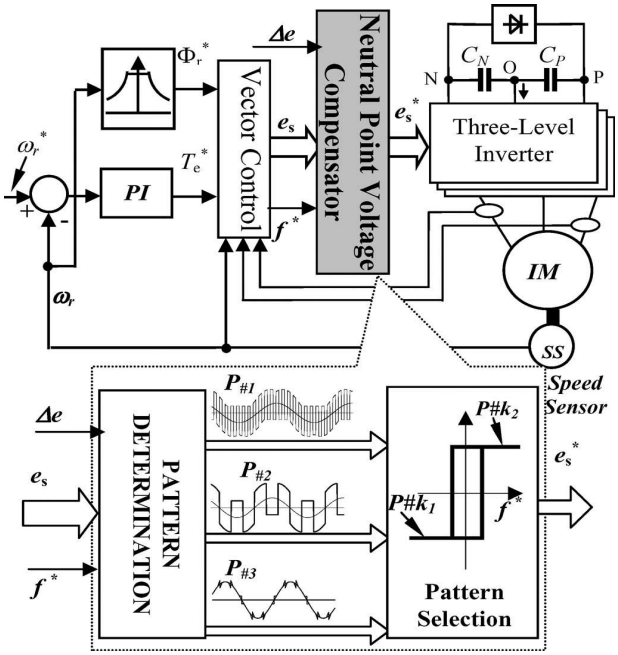
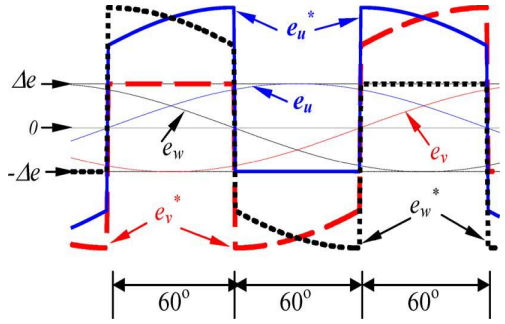


Fig. 7. Proposed method for NP voltage compensation.



$f_c = 1/T$, as follows:

$$\Delta e = E_d \times \frac{\Delta T_{\min}}{T}.$$

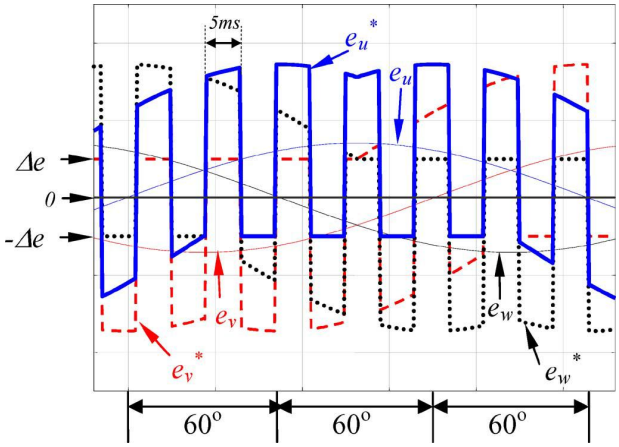


Fig. 8. Time switching mode at low operating frequency.

D. Algorithm

The general principle of the new PWM is as follows. Whenever the magnitude of one of the three phases reference voltage is less than the minimum voltage, then this phase has to be changed. It will be chosen greater or equal to the minimum voltage, and accordingly, the two other phases will be changed so that the new line-to-line voltage references are unchanged. Let the modified reference voltages have a superscript

The voltage reference, *er* , which has the largest magnitude among the three signals (i.e., *eu*, *ev* , *ew*) is set to a voltage having an opposite sign and a magnitude equal to the minimum voltageΔ*e*. Accordingly, the remaining reference voltages are adjusted so that the line-to-line voltages are kept equal to the original ones. For instance, when the voltage reference signal *eu* has the biggest magnitude ($|eu| \geq |ev| \geq |ew|$), each voltage reference signal is modified as follows: $\text{sign}(ew) \times \Delta e - (eu - ew)$.

The operational waveforms during this mode are shown inFig. 10. As illustrated in this figure, the switching patternswitches from one mode to another every 60◦.

Theoretically, the 60◦-rectangular mode may be used at any operating frequency. However, at very low speed, the period of 60◦ may become long. As a result, the imbalance may stay longer than expected, also the switching device, such as the GTO, will overheat as it is conducting for a very long period. The efficiency of the inverter will improve if we switch from one pattern to another at a faster rate than the 60◦ period.

Fig. 8.This algorithm reduces the NP voltage imbalance, and avoids the minimum ON-time pulses without increasing the switching losses of the switching devices. At

low-frequency operation, even if the magnitudes of the three-phase voltage references are all above the critical value Δ*e*, the time switching pattern shown in Fig. 11 is used. This results in a significant reduction of the fluctuations of the NP voltage *vo*.

IV. RESULTS AND DISCUSSIONS

Simulation Results

Simulation was carried out with and without the switchingpattern. Fig. 9 shows the simulation results, where the proposed method results in a significant reduction of the fluctuations of the NP voltage *vo* . Note that although the results shown have been generated using a switching frequency of 500 Hz, the proposed PWM scheme works irrespective of this frequency. Evidently, since the method can be implemented with devices other than MOSFETs, higher switching frequency can be used, the value of this must be compatible with the employed devices discussions

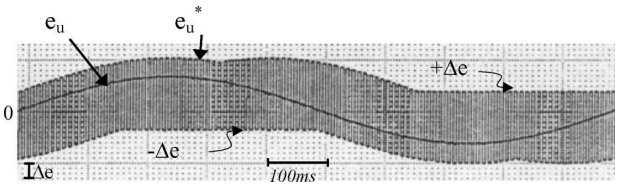


Fig. 9. Switching pattern applied at low speed (at 1 Hz operating frequency).

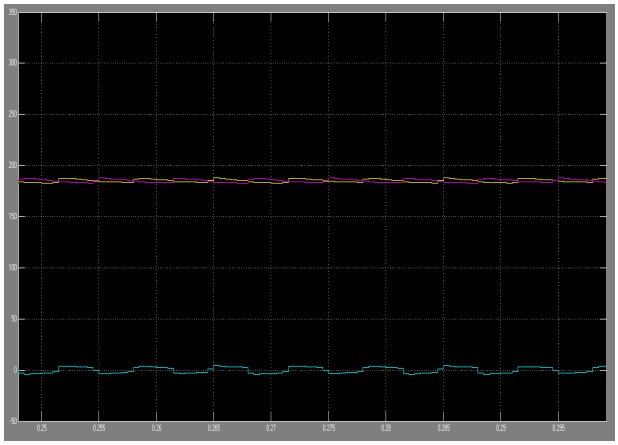
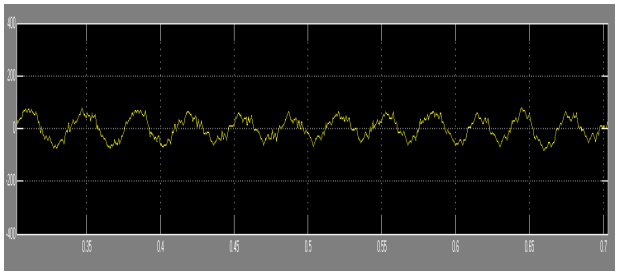


Fig. 10. NP voltage: with the proposed PWM .



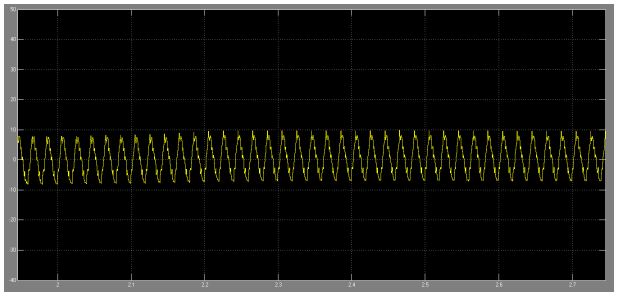


Fig. 16. Experimental results: current waveforms (upper: without minimum pulse compensation, lower: with compensation).

Table 1. DC link voltage comparison

Simulation time in seconds	DC Link Voltage (volts)			
	Conventional method		Proposed DPWM method	
	V_{CP}	V_{CN}	V_{CP}	V_{CN}
0.94	180.1	100.2	190.1	188.0
0.96	200.8	100.7	190.0	188.1
0.98	150.6	50.0	190.3	188.3
1	200.0	90.2	190.1	188.4

Table 2. THD comparison with conventional and proposed method

Simulation time in Seconds	% TOTAL HARMONIC DISTORTION	
	Conventional Method	Proposed DPWM Method
0.0	55.61	11.20
0.01	59.51	11.16
0.03	182.61	12.42
0.1	83.61	18.57

V. CONCLUSION

A new method, suitable for reducing the imbalanced voltage of the NP voltage, has been described. This method improves the characteristics of a MOSFET-based three-level inverter. The proposed switching-pattern-based PWM method approach has reduced the fluctuations of the NP voltage of the inverter, without increasing the switching losses. The

simulations and the experiments were carried out to verify the feasibility of the method. The proposed method is suitable for high performance energy saving drive system that can operate down to zero speed.

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