# BIST Method For Testing of Memory

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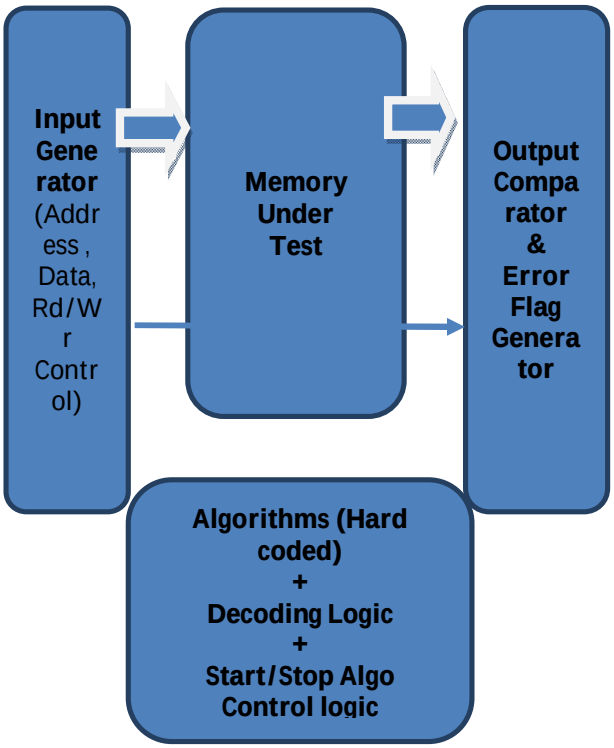
***Abstract***-*This paper gives information regarding to MBIST. This Built-in Self-Test (BIST) technique helpful from economically but also it gives test logic for the test pattern also concluded basic test problems and some reliable methods of solution. The basic concept of BIST is that it provides a path by which system could test itself. The saving from BIST include reduced test generation effort at all levels, reduced test effort at chip through system levels, improved system level maintenance and repair.*

***Keywords***-Xilinx, Memory Built-In Self Test (MBIST), Verilog, BIST

## I. INTRODUCTION

Built-in self-test (BIST) techniques constitute a group of techniques that provide the capability of performing high fault coverage with speed testing, whereas simultaneously they relax the reliance on expensive external testing tools. Hence, they constitute an attractive solution to the crisis of testing VLSI devices. BIST techniques are typically classified into online and offline. Offline architectures operate in either test mode or normal mode (during which the BIST circuitry is idle). During test mode, the inputs generated by a test generator unit are applied to the inputs of the circuit under test (CUT) and the results are captured into a response verifier (RV). Consequently, to perform the test, the normal operation of the circuit under test is stalled and, therefore, the performance of the system in which the circuit is included, is degraded. The functionality of gadgets and electronics equipment's has achieved a phenomenal growth over the last two decades while their physical sizes have come down significantly. The main reason is, due to the rapid advances in IC technologies, which enables fabrication of several millions of transistors in a single chip or integrated circuit (IC). According to Moore's law, number of transistors in a chip doubles in every 1.5 years. With the recent research in the technology, device shrinks to nanometer scale, but complexity and density of the chips keep on increasing. This may result in device failure and many manufacturing faults. Reduction in the feature sizes results in growing the fault detection and manufacturing faults becomes very difficult. VLSI testing is becoming more and more important and challenging to verify a device functions are properly or not. Conventional automatic test equipment (ATE) based testing technique is no longer able to handle the rising test challenges. The built-in self-test (BIST) is widely used in the online testing while chip in normal operation. In case of offline BIST chip is not in normal operation. The requirement of efficient and economical testing method such as the Built-In Self-Test (BIST) increases with the increase in complexity of Very Large Scale Integration (VLSI) devices or System-on-Chip (SoC). The logic behind BIST is to design an IC that is capable of verifying itself as being either fault-free or faulty and then continue its operation when the testing is not being carried out. Memory BIST has been proven to be one of the most cost- effective and widely used solutions for memory testing for the following reasons: no external test equipment, Reduced development efforts, tests can run at circuit speed to yield a more realistic test time, on-chip test pattern generation to provide higher controllability and observability, On-chip response analysis, test can be on-line or offline, adaptability to engineering changes

## II. IMPLEMENTATION AND DESIGN OF MEMORY BIST

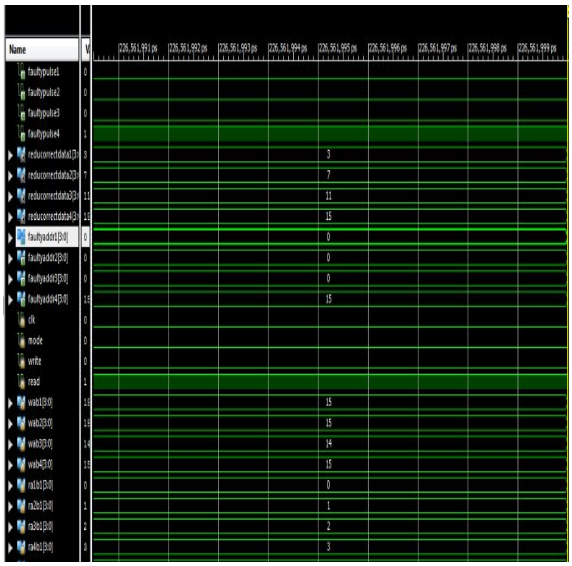



BIST Places the job of device testing inside the device itself and generates its own stimulus and analyzes its

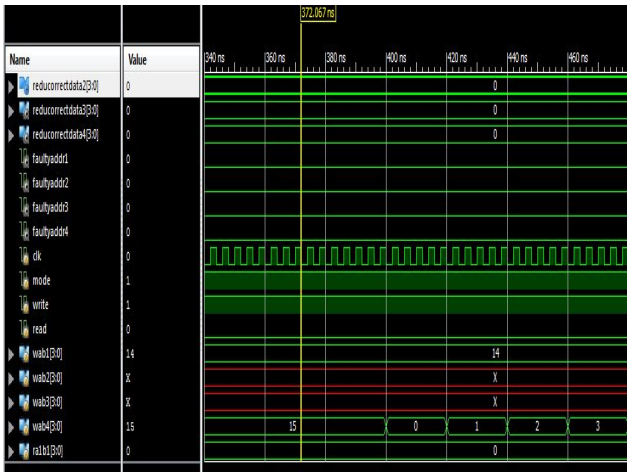
own response. The trend to include more test logic on an ASIC has already been mentioned. Built-in self-test (BIST) is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. In each case the principle is to generate test vectors, apply them to the device under test (DUT) or circuit under test (CUT), and then verify the response. The architecture of BIST technique is shown above which having three main components are CUT, TPG, and ORA. An automatic test pattern generation (ATPG) and fault simulation technique is used to generate the test patterns. A good test pattern set is stored in a ROM on the chip. When BIST is activated, test patterns are applied to the CUT and the responses are compared with the corresponding stored patterns. Although stored-pattern BIST can provide excellent fault coverage, it has limited applicability due to its high area overhead. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit. Controller generates control signals to the test pattern Generate control signals to the test pattern generator & the memory under test. Test Pattern Generator generates the required test patterns and Read/Write signals. Comparator evaluates the response. BIST structures generate patterns and compare output responses for a dedicated piece of circuitry. BIST can be implemented on entire designs, design blocks or structures within design blocks. Pattern generation as well as output-comparison circuitry can vary depending on the design.

## III. PERFORMANCE ANALYSIS

For mode = 0, the memory will perform in a regular manner. It will read/write the data and will give the output



For Mode = 1, BIST will be implemented on the memory. If there is any fault in the read/write data, then it will be tested and repaired and will then data will be sent to output



## IV. CONCLUSION

The BIST technology is economic and also gives logic test pattern. Typically the BIST controllers that are going to be generated will have test algorithms built into itself. The faults are checked in itself. We don't need an external hardware. So that the complexity is reduced and the cost reduction is also possible. By using the separate on-chip test logic, the memory test can be performed to reduce the test time and of being able to detect the faults at system operation speed is the advantage of BIST logic embedded memory. Different BIST architecture enables efficient tests of the high-performance embedded memories that are required essentially for the computer system, and it reduces the test cost.

## REFERENCES

[1] Xilinx. 7 Series FPGAs Configurable Logic Block User Guide, accessed on May 30, 2016. [Online].Available:http://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf

[2] Xilinx. Zynq-7000 All Programmable SoC Overview, accessed on May 30, 2016. [Online]. Available: http://www.xilinx.com/ support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf

[3] J.-L. Lin and B.-C. C. Lai, "BRAM efficient multi-ported memory onFPGA," in Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT),Apr. 2015, pp. 1–4.

[4] G. A. Malazgirt, H. E. Yantir, A. Yurdakul, and S. Niar, "Application specific multi-port memory customization in FPGAs," in Proc. IEEE Int.Conf. Field Program. Logic Appl. (FPL), Sep. 2014, pp. 1–4.

[5] C. E. Laforest, Z. Li, T. O'Rourke, M. G. Liu, and J. G. Steffan, "Composing multi-ported memories on FPGAs," ACM Trans. Reconfigurable Technol. Syst., vol. 7, no. 3, Aug. 2014, Art. no. 16.

[6] H. E. Yantir and A. Yurdakul, "An efficient heterogeneous register file implementation for FPGAs," in Proc. IEEE Int. Parallel Distrib. Process.Symp. Workshops (IPDPSW), May 2014, pp. 293–298.

[7] H. E. Yantir, S. Bayar, and A. Yurdakul, "Efficient implementations of multi-pumped multi-port register files in FPGAs," in Proc. Euromicro Conf. Digit. Syst. Design (DSD), Sep. 2013, pp. 185–192.

[8] C. E. LaForest, M. G. Liu, E. Rapati, and J. G. Steffan, "Multi-ported memories for FPGAs via XOR," in Proc. 20th Annu. ACM/SIGDA Int.Symp.Field Program. Gate Arrays (FPGA), 2012, pp. 209–218

[9] C. E. LaForest and J. G. Steffan, "Efficient multi-ported memories for FPGAs," in Proc. 18th Annu. ACM/SIGDA Int. Symp.FieldProgram.Gate Arrays, 2010, pp. 41–50.