Aging-Aware Reliable Multiplier Design with Adaptive Hold Logic

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Abstract-*High speed and low power consumption is one of the most important design objectives in integrated circuits. Digital multipliers are most critical functional units. The overall performance of this system depends on the throughput of multiplier design. Aging problem of transistors has a significant effect on performance of these systems and in long term, the system may fail due to timing violations. Aging effect can be reduced by using over-design approaches, but these leads to area, power inefficiency. Hence to reduce the maximum power consumption and delay, variable latency multiplier with adaptive hold logic is used. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. The proposed architecture can be applied to image multiplication. Based on the idea of razor flip flop and adaptive hold logic the timing violations are reduced. In the fixed latency usage of clock cycles is increased. The re-execution of clock cycles is reduced by using variable latency.*

Keywords-Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

I. INTRODUCTION

A multiplier is essential and abundant in DSP applications. Typical DSP applications where a multiplier plays an important role include image processing, wavelet transforms; telecommunication etc. The basic idea is to eliminate unnecessary computation of power saving via signal bypassing. **S**CALING OF MOS device geometries poses hard limitations on the development of new generations of integrated circuits. In particular, reliability has been indicated as one of the most serious concerns [1], [2]. Adverse on-chip operating conditions, characterized by extremely high substrate temperature, accelerate the degradation of the electromechanical properties of both active (i.e., transistors) and passive (i.e., interconnects) devices. Electro migration, hot-carrier injection, and time-dependent dielectric breakdown have been indicated as the main responsible of reliability decrease [3]. If we restrict our attention to the aging sources, negative bias temperature instability (NBTI) has emerged as the dominant factor in determining the lifetime of digital devices [4]. In CMOS circuits, NBTI effects occur in p-type transistors when a logic "0" is applied to the gate terminal (gate-to-source voltage Vgs = $-Vdd$, i.e., negative bias). Under this condition, called the stress state, the magnitude of the threshold voltage (Vth) increases over time, resulting in a degradation of the drive current.

In contrast, when a logic "1" is applied to the gate terminal (Vgs = 0), NBTI stress is actually removed. The latter condition, called the recovery state, induces a progressive yet partial recovery of the Vth. A traditional method to mitigate the aging effect is overdesign [5], including such things as guard-banding and gate over sizing; however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI-aware methodologies have been proposed. An NBTI-aware technology mapping technique was proposed in [7] to guarantee the performance of the circuit during its lifetime. In an NBTI-aware sleep transistor was designed to reduce the aging effects on pMOS sleep-transistors, and the lifetime stability of the power-gated circuits under consideration was improved. Wu and Marculescu [9] proposed a joint logic restructuring and pin reordering method, which is basedon detecting functional symmetries and transistor stacking effects. They also proposed an NBTI optimization method that considered path sensitization [12]. In [10] and [11], dynamic voltage scaling and body-basing techniques were proposed to reduce power or extend circuit life. These techniques, however, require circuit modification or do not provide optimization of specific circuits.

II. LITERATURE SURVEY

In many designs, the worst-case delay [1] of a critical path may be activated infrequently. Traditional optimization approaches assume the worst-case conditions, which could lead to an inefficient resource usage. It is possible to improve the throughput of such designs by introducing variable latency. One existing realization of the variable-latency design style is based on telescopic units. The design of the hold logic in telescopic units influences the circuit's throughput. In this paper, we show that the traditionally designed hold logic may

be inaccurate. They use the short path activation conditions to obtain more accurate hold logic and improve the efficiency of telescopic units. Threshold voltage (Vt) of a field effect transistor (FET) is[2] observed to shift with stressing time and this stress induced V t shift is an important transistor reliability issue. Vt shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping. In this paper, we present a comparative study of NBTI and PBTI for a variety of FETs with different dielectric stacks and gate materials. The study has two parts. In part I, NBTI and PBTI measurements are performed for FUSI NiSi gated FETs with SiO2 SiO2/HfO2 and SiO2/HfSiO as gate dielectric stacks and the results are compared with those for conventional Si ON/poly-Si FETs.For a low-power row-bypassing multiplier the addition [3]operations in the j-th row can be disabled to reduce the power dissipation if the bit bj in the multiplier is 0. In the multiplier design, each modified FA in the CSA array is attached by three tri-state buffers and two 2-to-1 multiplexers. Because the addition operations of the rightmost FAs in the CSA rows are able to be bypassed, the extra correcting circuits must be added to correct the multiplication result. a combination of circuit and architectural techniques[4] for low cost in-situ error detection and correction of delay failures. At the circuit level, each delay-critical flip flop is augmented with a so-called shadow latch which is controlled using a delayed clock. The operating voltage is constrained such that the worst-case delay is guaranteed to meet the shadow latch setup time, even though the main flip flop could fail. By comparing the values latched by the flip flop and the shadow latch, a delay error in the main flip-flop is detected. Negative bias temperature instability (NBTI) has[5] become a dominant reliability concern for nanoscale PMOS transistors. In this paper, we propose variable-latency adder (VL-adder) technique for NBTI tolerance. By detecting the circuit failure on-the-fly, the proposed VL-adder can automatically shift data capturing clock edge to tolerate NBTI-induced delay degradation on critical timing paths. VL-adder operates with a fixed supply voltage and clock period, avoiding the high design and manufacturing costs incurred by existing NBTI-tolerant techniques.

III. METHODOLOGY

This section details the proposed aging-aware reliable multiplier design. It presents the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs. Fig.1 shows our proposed aging-aware multiplier architecture, which consists of two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops [10], and an AHL circuit. The inputs of the row-bypassing multiplier are the symbols in the parentheses. In the proposed architecture, the column- and row-bypassing multipliers can be examined by the number of zeros in either the multiplicand or multiplication to predict whether the operation requires one cycle or two cycles to complete. At the point When input patterns are irregular, the number of zeros and ones in the multiplication and multiplicand follows a normal distribution.

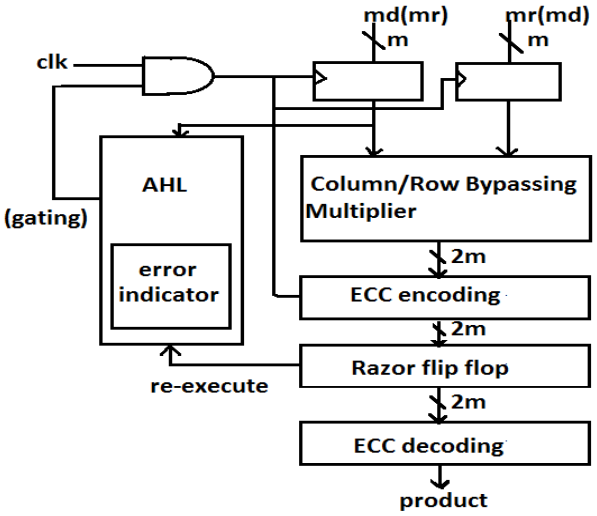

Fig.1: Proposed architecture

Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the column or row-bypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing multiplier is the multiplicand, whereas that of the row-bypassing multiplier is the multiplication. Razor flip-flops can be used to detect whether timing violations happens before the next input pattern arrives.

Fig.2 shows the details of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to execute the operation and notify the AHL circuit that an error has occurred. We use Razor flip-flops to detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is executed with

two cycles. Although the reexecution may seem costly, the overall cost is low because the reexecution frequency is low. More details for the Razor flip-flop can be found in [10].

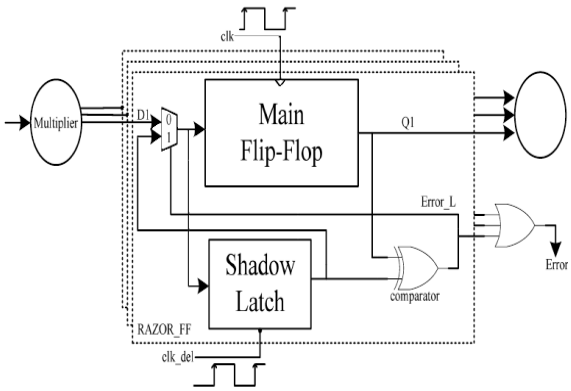

Fig.1: Razor Flip-Flop

The aging indicator indicates whether the circuit has suffered significant execution degradation due to the aging effect. The aging indicator is implemented in a basic counter that counts the number of errors over a certain amount of operations and is reset to zero at the end of those operations. If the cycle period is too short, the column- or row-bypassing multiplier is not able to complete these operations successfully, causing timing violations. These timing violations will be caught by the Razor flip-flops, which generate error signals. If errors happen frequently and exceed a predefined threshold, it means the circuit has suffered significant timing degradation due to the aging effect, and the aging indicator will output signal 1; otherwise, it will output 0 to demonstrate the aging effect is still not significant, and no actions are required.

The overall flow of our proposed architecture is as per the following: when input patterns arrive, the column- or row-bypassing multiplier, and the AHL circuit execute simultaneously. According to the number of zeros in the multiplicand (multiplication), the AHL circuit chooses if the input patterns require one or two cycles. If the input pattern needs two cycles to complete, the AHL will output 0 to disable the clock signal of the flip-flops. Something else, the AHL will output 1 for normal operations. When the column- or row-bypassing multiplier finishes the operation, the result will be passed to the Razor flip-flops. The Razor flip-flops check whether there is the path delay timing violation. If timing violations occur, it means the cycle period is not long enough for the current operation to complete and that the execution result of the multiplier is incorrect. Thus, the Razor flip-flops will output an error to inform the system that the current operation needs to be reexecuted using two cycles to ensure the operation is correct. In this situation, the extra reexecution cycles caused by timing violation incurs a penalty to overall average latency. However, our proposed AHL circuit can precisely predict whether the input patterns require one or two cycles in most cases.

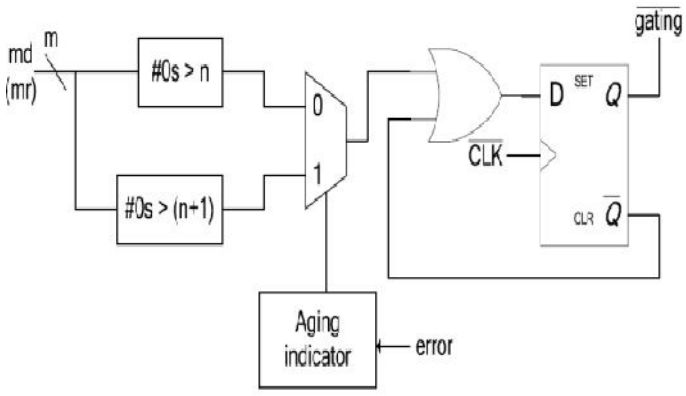

Fig 3. AHL Circuit

A. FPGA Spartan 6

The Spartan®-6 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to 5,000,000 system gates, The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from the Virtex®-II platform technology. These Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry. Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection and digital television equipment.

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  - 622+ Mb/s data transfer rate per I/O
  - Dedicated 18 x 18 multipliers
- Selec RAM™ hierarchical memory
  - Up to 1,872 Kbits of total block RAM
  - Up to 520 Kbits of total distributed RAM

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B. Hamming Codes - Error Detection and Error Correction

The way to the Hamming Code is the utilization of additional parity bits to permits the identification of a single error. Make the code word as follows:

Mark all bit positions that are powers of two as parity bits. (positions 1, 2, 4, 8, 16, 32, 64, etc.)

All other bit positions are for the data to be encoded. (positions 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, 17, etc.)

Each parity bit calculates the parity for some of the bits in the code word. The position of the parity bit determines the sequence of bits that it alternately checks and skips.

Position 1: check 1 bit, skip 1 bit, check 1 bit, skip 1 bit, etc. (1,3,5,7,9,11,13,15,...)

Position 2: check 2 bits, skip 2 bits, check 2 bits, skip 2 bits, etc. (2,3,6,7,10,11,14,15,...)

Position 4: check 4 bits, skip 4 bits, check 4 bits, skip 4 bits, etc. (4,5,6,7,12,13,14,15,20,21,22,23,...)

Position 8: check 8 bits, skip 8 bits, check 8 bits, skip 8 bits, etc. (8-15, 24-31, 40-47,...)

Position 16: check 16 bits, skip 16 bits, check 16 bits, skip 16 bits, etc. (16-31,48-63,80-95,...)

Position 32: check 32 bits, skip 32 bits, check 32 bits, skip 32 bits, etc. (32-63,96-127,160-191,...)etc.

Set a parity bit to 1 if the total number of ones in the positions it checks is odd. Set a parity bit to 0 if the total number of ones in the positions it checks is even.

IV. SOFTWARE IMPLEMENTATION

Result without error

Result with error

IV.CONCLUSION

This paper is a review on aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The proposed variable latency multipliers can be used under the influence of both the BTI effect and electro migration. In addition, it has less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period. We will analyze the

behavioral simulation of this proposed multiplier by using Xilinx ISE simulator using Verilog HDL language.

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