High Speed Multiplication using Ancient Mathematics – Urdhwa Tiryagbhayam

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Abstract-*The most important fundamental cell in any processor is multiplier which forms the basis of most of the computations in the technical formulas. The multiplier based on conventional method takes long time for completing the multiplication as compared to the multipliers using vedic mathematics. Huge Arithmetic Multiplication functions are currently used in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of the processors algorithms, which makes for the great need of high speed multiplier. Multiplication is an important and factor in evaluating the processing of instructions processed per unit in all types of processors. The demand for high speed processing has been growing as a result of developing computer and signal processing applications. This leads for an efficient throughput processor that is required for getting the desired performance in most of the Digital signal processing applications. So, arithmetic operations in the processors require multiplication which makes the development of fast multiplier circuit; which has been a subject of interest over decades. Multiplier based on Vedic mathematics calculates the required multiplication in less time thereby consuming less Gates, LUTs & IOBs. Employing this technique in the computation algorithms will reduce the complexity, execution time, power etc.*

Keywords-Urdhwa Tiryagbhayam, Reversible Gate, Vedic Mathematics, 32x32 Vedic Multiplier, Xilinx

I. INTRODUCTION

ANCIENT VEDIC MATHEMATICS

The word 'Vedic' means the store-house of all knowledge derived from the word 'veda'. It was introduced by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja as Vedic Mathematics. Vedic mathematics consists of 16 Vedic Sutras.

VEDIC SUTRAS

Vedic mathematics consisting of 16 Sutras deals with various branches of mathematics like arithmetic, algebra, geometry etc. Below are the 16 Sutras definitions:-

1) (Anurupye) Shunyamanyat – The work of it is if the one is in ratio; then other is zero
2) Chalana-Kalanabyham – It means differences and similarities.
3) Ekadhikina Purvena – It means by one more than the previous one
4) Ekanyunena Purvena – It means by one less than the previous one
5) Gunakasamuchyah – It means the factors of the sum is equal to the sum of the factors
6) Gunitasamuchyah – It means the product of the sum is equal to the sum of the product
7) Nikhilam Navatashcaramam Dashatah – It means all from 9 and the last from 10
8) Paraavartya Yojayet – It means Transpose and adjust.
9) Puranapuranabyham – It means by the completion or noncompletion
10) Sankalana-vyavakalanabhyam – It means by addition and by subtraction
11) Shesanyankena Charamena – It means the remainders by the last digit
12) Shunyam Saamyasamuccaye – It means when the sum is the same that sum is zero
13) Sopaantyadvayamantyam – It means the ultimate and twice the penultimate
14) Urdhva-tiryakbyham – It means Vertically and crosswise
15) Vyashtisamanstih – It means Part and Whole
16) Yaavadunam – It means whatever the extent of its Deficiency

II. URDHVA-TIRYAKBYHAM - VERTICAL & CROSSWISE

The working of this multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a common multiplication formula which is applicable to all cases of multiplication. It's literal meaning is "Vertically and crosswise". It is based on the principle through

which the generation of all partial products can be done with the concurrent addition of these partial products. The generation of partial products and their summation is obtained using Urdhava Tiryakbhyam explained in figure. The generalized form of the algorithm can be for n x n bit number. In this the partial products and their sums are calculated in parallel. Apart from it the multiplier is independent of the clock frequency of the processor. Therefore the multiplier will require the same amount of time to calculate the product and all the partial products and hence it is independent of the clock frequency. Therefore it can be said that the advantage of vedic multiplier is that that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By using the Vedic multiplier, microprocessors the designers can easily find a way around the problems to avoid fatal device failures.

MULTIPLICATION OF 3 DIGIT NUMBER 234*316

Urdhwa-Tiryagbhayam is the general formula applicable to all cases of multiplication. It means "Vertically and Crosswise."

1) Step 1 – 4*6 = 24: [2 carried over digit placed below the 2nd digit]

2) Step 2 - (3*6)+(4*1)=18+4=22: [2 carried over digit placed below the 3rd digit]

3) Step 3 – (2*6)+(3*1)+(4*3)= 12+3+12= 27: [2 carried over digit placed below the 4th digit]

4) Step 4- (2*1)+(3*3)=2+9=11: [1 carried over digit placed below the 5th digit]

5) Step 5 - 2*3 = 6

6) Respective digits are added at the end. All the carries are added to produce the final answer: 73944

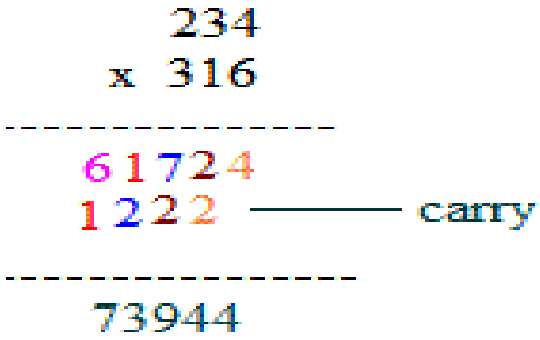

Figure 1:- Vedic Multiplication Example of 234*316

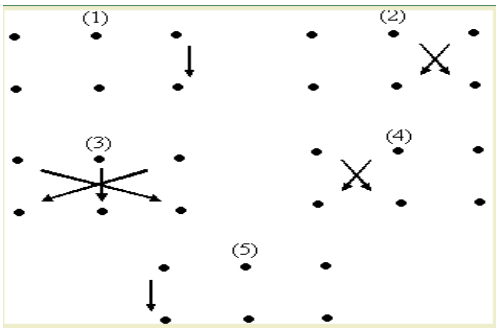

Figure 2:- General Rule for 3*3 multiplication

III. ALGORITHM FOR VEDIC MULTIPLIER

Vedic Mathematics works on the 16 algorithms or sutras developed and derived from ancient Vedic texts. This particular method for fast multipliers used in digital image and signal processing techniques is named Urdhva Tiryakbhyam is more efficient and which consume less time and improves the speed and performance. This method performs multiplication in crosswise and vertically manner it makes all the numeric computations faster by generating partial product and sum in single iteration[1][2][3][4][5]. The Vedic multiplier calculates faster than the conventional multipliers. This gives a scheme for hierarchical multiplier design. The design is faster, consumes smaller area and has less power consumption as compared to the conventional multipliers.

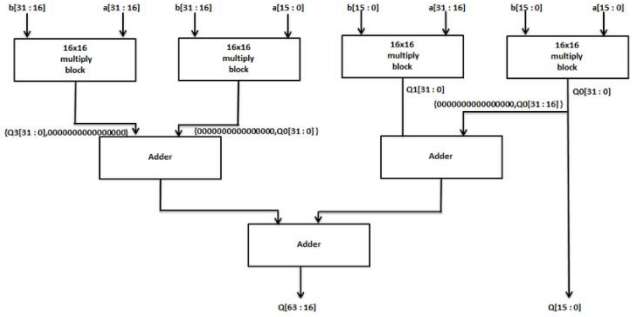

Figure 3: Block diagram of 32x32 UT Multiplier

IV. PERFORMANCE ANALYSIS

The conventional multiplier requires more gates and so the processor using simple conventional multipliers speed becomes slow. The Table 1 and Table 2 gives the summary of the maximum path delay and number of Slices, LUTs and IOBs for both conventional multiplier and Reversible Gates [vedic maths] multipliers. The tables clearly shows that reversible gates are more efficient than conventional multiplier as uses less number of LUTs, Slices, IOBs ; thereby making the processor speed fast using reversible gates [vedic math's].

Table 1: Comparison of speed using various multipliers

Technology used	**Maximum Path Delay**
4x4 conventional multiplier	13.201 ns
4x4 multiplier using reversible gates	12.972 ns
8x8 conventional multiplier	26.177 ns
8x8 multiplier using reversible gates	24.484 ns
16x16 conventional multiplier	45.183 ns
16x16multiplier using reversible gates	40.214 ns
32x32 multiplier using reversible gates	38.874 ns

Table 2: 32x32 multiplier using reversible gates[vedic maths]

Number of Slices:	2896 out of 5720 (50 % utilized)
Number of LUTs FF pairs Used:	2896 out of 2896 (100% utilized)
Number of bonded IOBs:	128out of 102 (125% utilized)

OUTPUTS OF VEDIC MULTIPLIERS

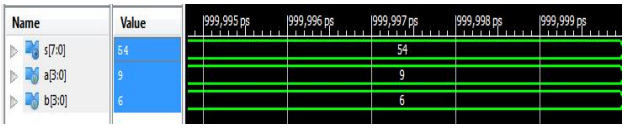

Figure 4:- Output of 4x4 Vedic Multiplier

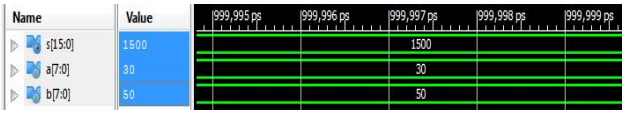

Figure 5:- Output of 8x8 Vedic Multiplier

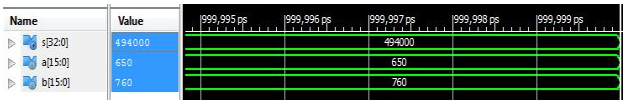

Figure 6:- Output of 16x16 Vedic Multiplier

Figure 7:- Output of 32x32 Vedic Multiplier

A high speed 4x4 vedic multiplier, 8x8 vedic multiplier, 16x16 vedic multiplier , 32x32 vedic multiplier was designed with below inputs and outputs.

V. CONCLUSION

Thus an efficient Vedic multiplier with high speed, low power and consuming little bit wide area was designed and implemented on device Spartan and simulated using ISE simulator. It was found that the multiplier based on vedic sutras had execution delay of almost half of that of binary multiplier.

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