Area Efficient Implementation of FM0/Manchester Encoding & Decoding Using Sols Techniques For DSRC Applications

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Abstract-*DSRC (Dedicated Short Range Communication) is a protocol mainly used for intelligent transportation system. The information signals transmitted by this protocol are encoded by using either FM0 or Manchester codes. The code diversity between these two codes limits the designing of a VLSI architecture that supports the both. Hence this paper put forward a new VLSI architecture design which can be fully reused by using both the codes. This design based on similarity oriented logic simplification (SOLS) technique achieves an efficient performance compared with sophisticated works. In order to decode the encoded data, a SOLS decoder can also be designed. This design flow can be attained in Verilog language by using Xilinx development board.*

Keywords-DSRC protocol, FM0 encoding, Manchester encoding, SOLS encoder, SOLS decoder.

I. INTRODUCTION

Dedicated Short Range Communication (DSRC) is a protocol used for communication for a short range of distance, say a few hundred meters through a dedicated channel. It is used to introduce intelligent transport system into our day to day life. The DSRC communication aids in both vehicle to vehicle communication as well as vehicle to roadside communication. The vehicle to vehicle communication mainly deals with the collision alarms, hard break warnings etc. At the same time the vehicle to infrastructure communication includes the Electronic Toll Collection (ETC), highway-rail intersection warning, in vehicle signing etc. However the primary motivation of the DSRC communication channel is collision detection and vehicular safety. In addition to it, it also an aid in smooth Every DSRC equipment is equipped with a reusable system that can make use of both FM0 and Manchester encoding. The normal reusable system designed has the disadvantage of consuming more memory space, having lower device utilization rate and lower efficiency. Hence a new technique called Similarity Oriented Logic Simplification (SOLS) technique is used to design the reusable system. The SOLS technique facilitates easier communication by the designing a more simplified version of the encoder and decoder systems. The SOLS system have higher device utilization rate, consumes lower device utilization rate. Also the system has higher efficiency.traffic control. In DSRC communication, normally FM0 or Manchester encodings are used. These encodings are characterized by the use of a transition in the middle of a clock pulse. Therefore the encoded data undergoes transitions even if the data is a string of identical bits. Hence they enable the system to overrule the possibility of treating a channel with a string of similar data as an idle channel.

II. LITERATURE SURVEY

Dedicated short range communication (DSRC) is a fast, short to midrange, wireless technology. It enables one way or two way communication between vehicles or between vehicles and roadside.[2] It is to used make streets safer, travel easier and minimizes the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per second.[1]

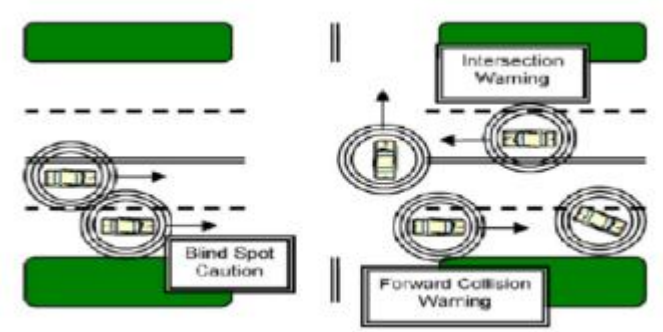

Fig.1: DSRC Communication

In DSRC communication, the most important concern is collision detection. Each DSRC equipped vehicle broadcasts its basic information including speed, trajectory, location etc to a short range of distance, say a few hundredmeters. All other DSRC equipped vehicles in the vicinity receives this message. Later on this message is decoded by the receiver vehicles and a caution or warning

may be issued to the driver. This can be issued audibly, visually or haptic ally. The DSRC Communication can be illustrated using fig 1. [2] The DSRC communication is based on direct communication between vehicles. Therefore it does not need a networking capability. The safety communication is mainly through broadcasting and it does not have a coordinator to facilitate the communication. Each DSRC equipped vehicle can communicate with its neighbor and each neighbor can communicate with its own neighbors. Finally the communication can extend to an unbounded level. Hence DSRC communication can be described as a single hop, uncoordinated broadcast messaging in an unbounded system consisting of all neighboring vehicles in a dedicated channel.[4] The safety communication involvestwo types of messages:

1) Routine safety messages— These are status messages including change of speed, location, etc that are regularly sent by the vehicle.

2) Event safety messages— These are messages that signify an event like a hard brake.[4]

In case of routine safety messages, there is a chance of receiving the same message twice by the same vehicle. This is avoided by using the Echo protocol. In Echo protocol, every message is attached with an unique message Id. Whenever a message is received, the receiver cross check the message with the message id of the previous messages. If both the IDs match, then the message is assumed to receive before and it is rejected. However, in the case of event safety messages, the whole operation is controlled bythe receiver. The sender echo's the message. When a similar echo is detected, it sends an unique sender ID along with the message.[5]

III. METHODOLOGY

A. FM0 Encoding-Decoding

FM0 encoding also known as biphase space encoding, is a type of Non-Return to Zero code. It is also used to represent the binary signals in a digital system. In FM0 encoding, even though the data stream does not encounter transition, the encoded signal experiences a transition for every clock cycle. The FM0 encoding can be specified by using the three basic rules [1]. They are as follows:

1) There should be transition for every logic zero input within a clock cycle.
2) There should be no transition for logic one input.
3) There should be a transition after every clock cycle irrespective of the input data. These rules can be better be explained by using the diagram (Fig 2).

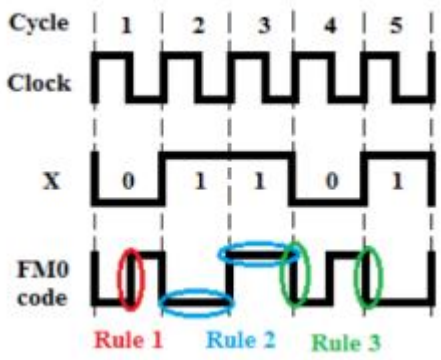

Fig.2:FM0 Encoding

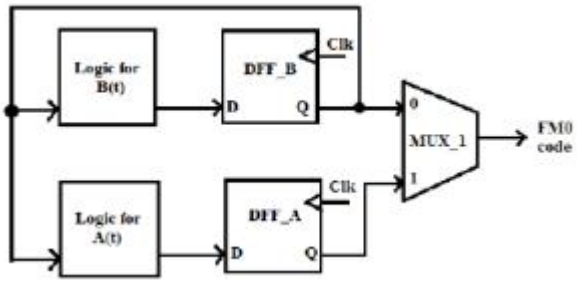

Fig.3: FM0 Encoder

FM0 encoding can be realized by using two flip-flops and also multiplexers. The FM0 encoding can be implemented by using the block diagram as shown in fig 3. In the following block diagram, A(t) and B(t) signifies the two states. FM0 decoding involves the conversion of a data that encounters transition during the clock pulse. Such a system operates by checking whether the two bits of the encoded data are equal. When both of them are equal, then the output is a logic '1'. but whenever the both bits are unequal, the system produces a logic '0' output. It can be implemented by using an XNOR gate and D flipflops.

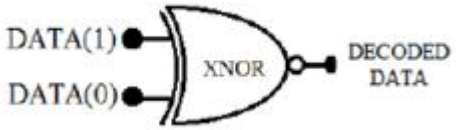

Fig.4: FM0 Decoder

B. Manchester Encoding - Decoding

One of the most common data coding methods used today is Manchester encoding. Manchester coding gives a way of adding the data rate clock to the message to be used at the receiving end. To represent the binary values 1 and 0 in digital system, the Manchester codes are used. Manchester code

represents binary values by a transition rather than a level. An example of a Manchester encoding is shown below in Fig 5.

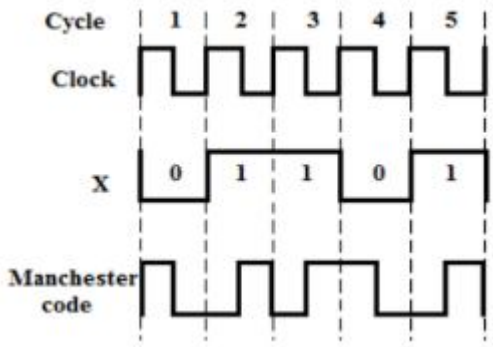

Fig.5: Manchester Encoding

Manchester coding states that there will always be a transition of the message signal at the mid-point of the data bit frame. What occurs at the bit edges depends on the state of the previous bit frame and does not always produce a transition. A logical 1 is defined as a mid-point transition from low to high and a 0 is a mid-point transition from high to low. The Manchester encoding can be implemented using an XOR gate where the clock signal and the data signal are XORed together to obtain the encoded data as shown in the diagram below (Fig 6.)

Fig. 6. Manchester Encoder

Manchester decoding involves the conversion of a data that encounters transition during the clock pulse. Such a system can be designed by XNORing the first data bit with the positive clock pulse. Such a system is shown in figure 7.

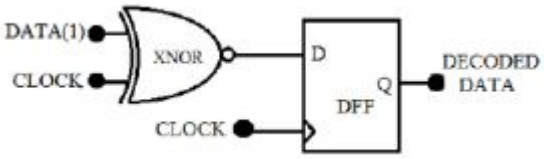

Fig.7: Manchester Decoder

C. SOLS Technique for Encoder Section

Normally DSRC encoders make use of both the FM0 and the Manchester encoding. Hence both the encoders can be combined together to form a reusable encoder. Such a reusable encoder can be illustrated as shown in the figure 8. This block diagram can be further simplified using the SOLS technique. The SOLS encoder consists of mainly two methods:

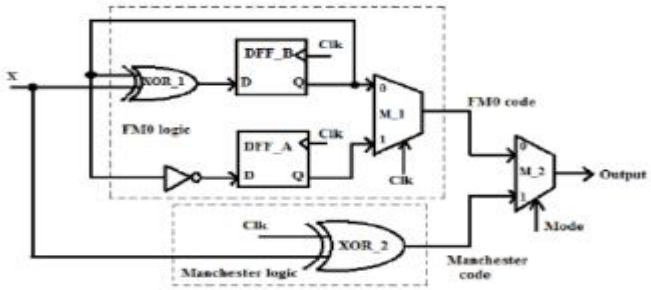

Fig 8:Reusable Encoder

1) **Area Compact Retiming:** This method is mainly usedin simplifying the FM0 encoder. For FM0 encoder, the state code of each state A(t) and B(t) is stored into separate flip flops. Since the transition of state code only depends on B(t), the encoder needs only a single bit flip flop. Hence the block diagram is rearranged as shown in the diagram 9.

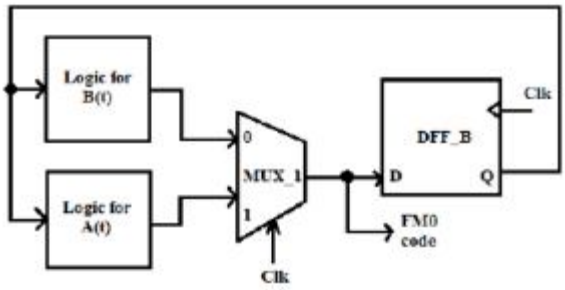

Fig. 9. Simplified FM0 Encoder

2) **Balance Logic Simplification:** This technique dealswith the Manchester encoder. Usually Manchester encoding can be treated as the XORing between the input signal and the clock. But it can also be treated as a Multiplexer where the clock is given as the select input and the data and its complement is given as the data input. This is better explained by the diagram 10.

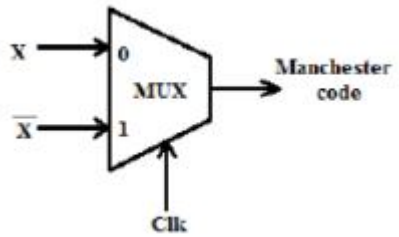

Fig. 10. Simplified Manchester Encoder

The above specified simplified encoders are combined together to form the SOLS encoder. This is shown

in the diagram 11. The disadvantage of this SOLS encoder is that there is an unbalance in the computation time which results in glitch. In order to avoid that, the NOT gate is moved to the output part of the first Mux and the XOR gate is replaced by the XNOR gate as shown in the diagram 12.

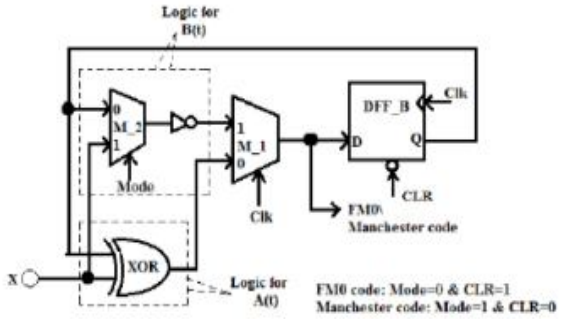

Fig.11.SOLS Encoder

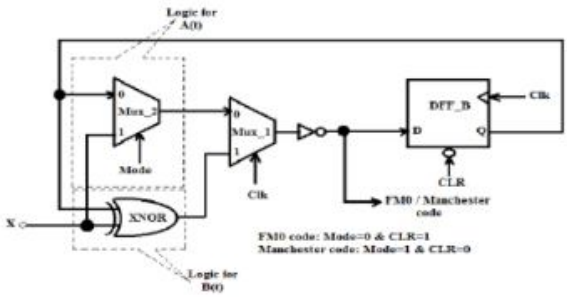

Fig. 12. Retimed SOLS Encoder

D. SOLS Technique for Decoder Section

FM0 decoder can be simplified by using area compact retiming. In this method, the decoder is simplified into a system containing only two edge triggered flipflops and an XNOR gate, as shown in the figure 13. In Manchester decoding, according to the transition the decoded data can be either a logic '1' or a logic '0'. Such a system can be implemented by using a simple NOT gate as shown in the figure 14.

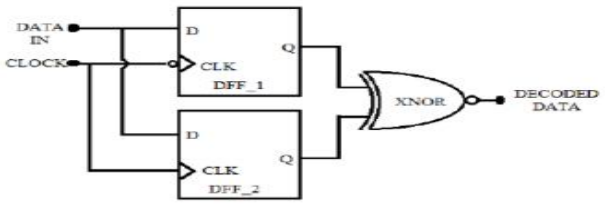

Fig.13.Simplified FM0 Decoder

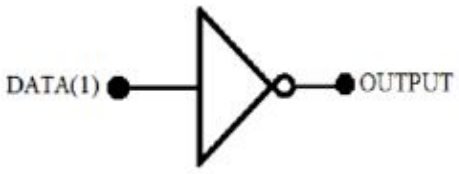

Fig.14. Simplified Manchester Decoder

A normal reusable decoder can be designed by combining both the FM0 and Manchester decoders. Using SOLS technique, the normal reusable decoder can be simplified and retimed into SOLS decoder which is shown in the figure 15.

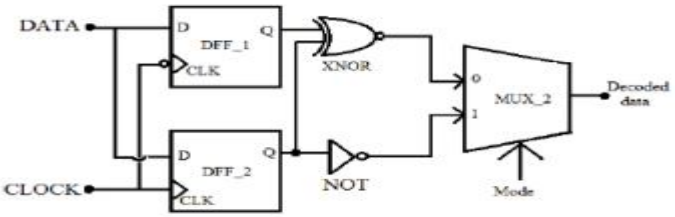

Fig.15. Reusable SOLS Decoder Section

E. RESULTS

a) Encoder RTL Schematic:

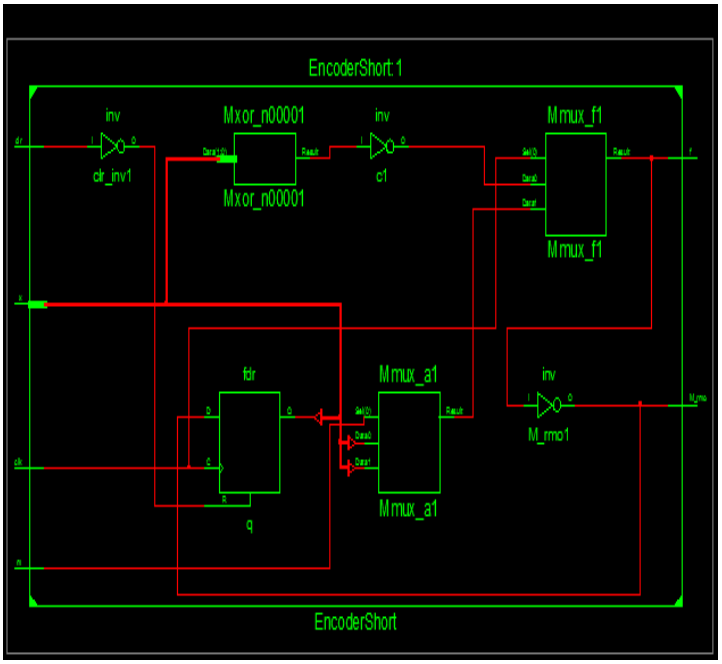

Figure16: Encoder RTL Schematic

Xilinx ISE 14.7 Simulations:

The SOLS design is realized with Spartan 6 xc6slx45-3csg484 FPGA as a targeted device by using Xilinx ISE14.7 design suite with Verilog HDL language.

1] Encoder Simulation:

Xilinx ISE Simulation for Manchester encoding:

At the positive edge of clock when mode is at logic '1'and CLR at logic 0, Manchester encoding is adopted. When

input X is at logic 0, it shows 1 to 0 transition of falling edge as shown in figure

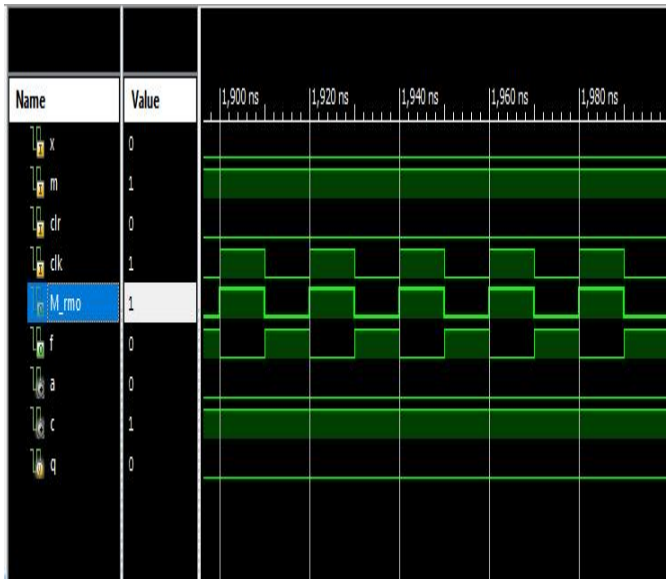

Figure 17: Simulation waveforms of Manchester encoding when X is at logic '0'.

When x is at logic 1, it shows 0 to 1 transition of rising edge between one clock cycles as shown in figure

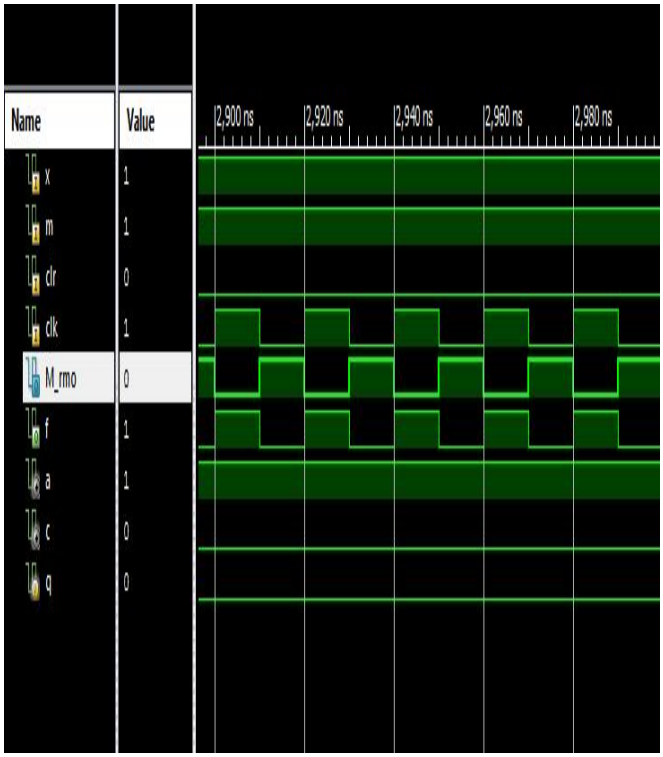

Figure 18: Simulation waveforms of Manchester encoding when X is at logic '1'.

Xilinx ISE simulation for FM0 encoding:

At the positive edge of clock, when mode is '0' and CLR are at logic 1, FM0 encoding is adopted. When X is at logic 0, it shows 0 to 1 transition in one cycle of clock as shown in figure

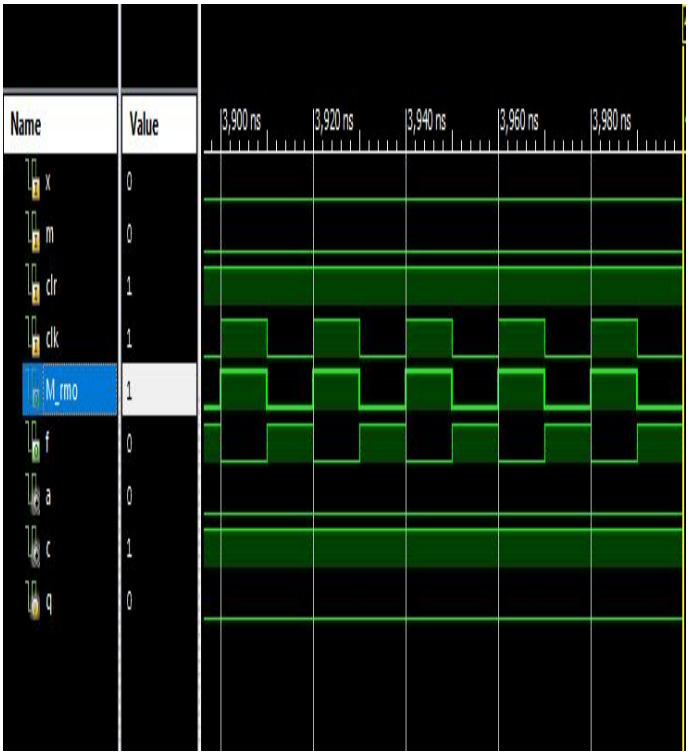

Figure 19: Simulation waveforms of FM0 encoding when X is at logic '0'.

When X is logic 1 then no transition between the clock cycles as shown in Figure below. The FM0 transition allocated amongst each FM0code after every clock cycle which validate all the three rules for FM0 encoding principles.

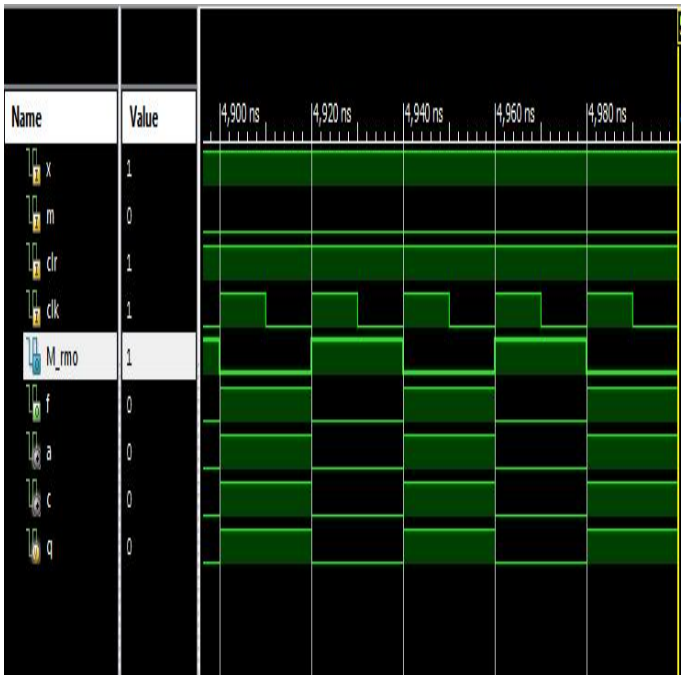

Figure 20: Simulation waveforms of FM0 encoding when X is at logic '1'.

Decoder RTL Schematic:

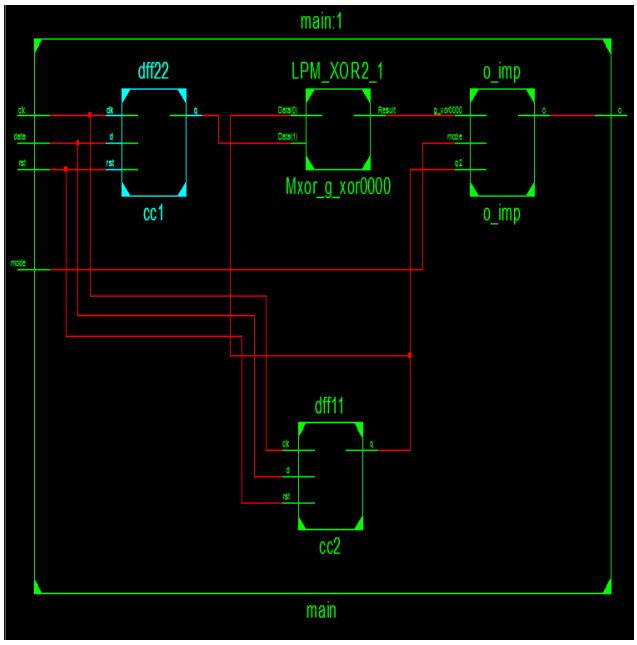

Figure 21: Decoder RTL Schematic

4.9.1. Decoder Simulation Waveforms:

Xilinx ISE simulation for Manchester Decoding
Mode=0

The simulated output of a Manchester Decoder is shown in figure 19. Here clock pulse encounters a transition in the data bits. When the transition is from logic low to logic high, then the output is logic ’1’. Similarly when the transition is from logic high to logic low, then the output is logic ’0’

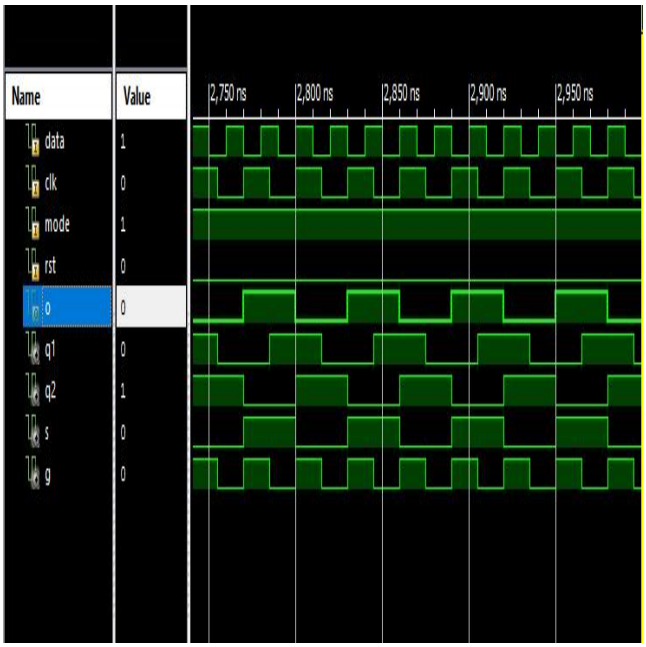

Figure 22. Simulation waveforms of Manchester decoding

Xilinx ISE simulation for FM0 Decoding:

Mode=0

The simulated output of the FM0 Decoder after simplification is shown in fig. Here whenever the input data bit experience a transition during the clock pulse, the output data is considered as a logic ’0’. Similarly whenever the data bits remain constant for a clock pulse without any transition, then the output is logic ’1’.

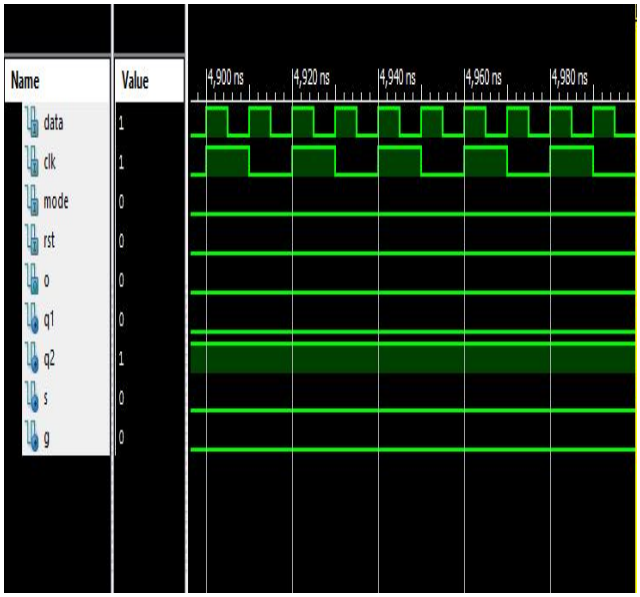

Figure 23:Simulation waveforms of FM0 decoding when input data have transition in clock pulse.

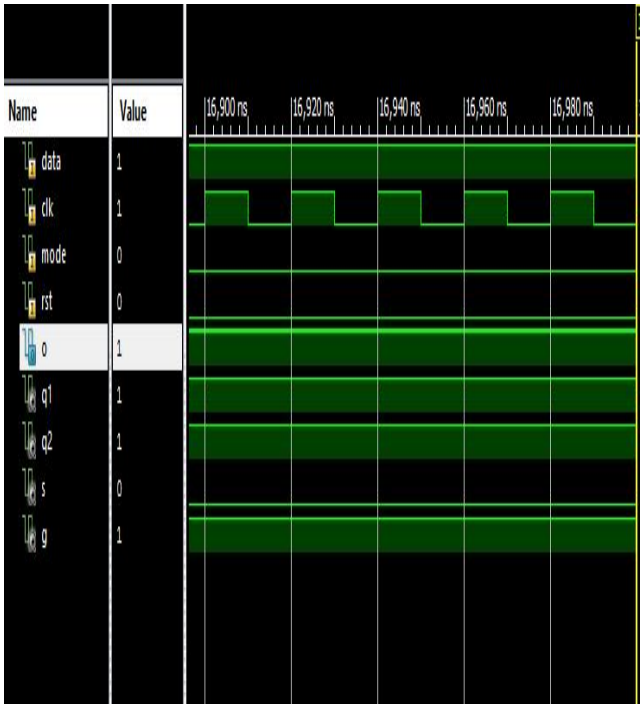

Figure 24: Simulation waveforms of FM0 decoding when input data have no transition in clock pulse

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