Solar Micro Inverter Efficiency can be Improved By Operating in Different Modes of Operation

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Abstract- *This paper discusses a control method that achieves high weighted efficiency in solar micro-inverters. A challenge in micro-inverters is to achieve high efficiency over a range of output powers. To address this challenge, the proposed controller presents two primary benefits that enable such an efficiency profile, a switching frequency that scales with power, and a low peak current that enables efficient magnetic design of the inductor. At high powers, the switching frequency increases to minimize the RMS current, and at low powers, the switching frequency decreases to minimize the switching loss. Since the peak inductor current is low, the inductor may be designed with fewer turns of wire, or with lower flux density, and is thus highly efficient. The proposed constant peak current switching scheme is implemented by a chaotic frequency modulation technique which reduce EMI and reduce the cost and improves overall efficiency.*

Keywords- Discrete event simulation, queuing system, size delay function

I. INTRODUCTION

Micro-inverters are small single-phase power modules that connects directly to a photovoltaic (PV) panel and to the AC line [1]-[3]. Several advantages of these devices include individual maximum power point tracking of each PV panel, modular connection, and high reliability, because a system of micro-inverters has no single point of failure. Due to the varying nature of solar energy, micro-inverters are rated according to their weighted efficiency. One example of a weighted efficiency standard is that published by the California Energy Commission [4], generally known as the CEC weighted efficiency. This standard uses a formula involving the inverter efficiencies at operating points ranging from 10% to 100% of the inverter rated power, where the 100% power point is assigned a small weighting factor of 5%, while intermediate power points are weighted more strongly. achieving a peak efficiency of 95.1 %. Works [9] and [11] demonstrate a modified buck topology that utilize 6 switches, and achieves a typical weighted efficiency of 96.5 % and a peak efficiency of 97.4 %. Works [12] and [13] propose a BCM scheme that is zero voltage switching and achieves peak efficiencies of 98.4 % and 98.7 %. Another study in [14] uses BCM and CCM waveforms that has high current ripples to achieve a fully zero-voltage switching topology, a topology that enables peak efficiency of 97.5%.

Despite these recent advancements, the main barrier for higher efficiencies remains the switching loss. While the DCM and BCM control methods are soft switching, the frequency dependent losses are still dominant in these approaches. One example is the loss due to the output capacitances of the switching devices, a loss mechanism that is voltage driven, does not scale with the output power, and hence substantially degrades the inverter weighted efficiency. The popular BCM control scheme actually increases the switching frequency when the inverter output current is reduced, with corresponding penalty in the efficiency. Thus, to improve the weighted efficiency, it is desirable to lower the switching frequency at low output powers.

In the competitive business of solar grid-tied solar micro-inverters, cost and efficiency are critical. In a moderately-shaded rooftop environment, distributed maximum power point tracking (MPPT) can increase the annual energy capture by 5-10% [15], and therefore an increase in micro-inverter efficiency of even 1% or less can significantly impact the value proposition of grid-tied micro-inverter systems. We propose a new approach to micro-inverter design and control that can lead to significant improvements in efficiency and cost. This approach is based on a variable-frequency DCM approach that can reduce the inverter power stage average loss by a factor of two. The size and cost of the inverter inductors is also significantly reduced, and the cost and complexity of current sensing is also reduced.

We address this challenge by introducing a novel control scheme and an optimized magnetic design. the proposed research provides not only an improved peak efficiency, but more importantly a substantially improvement in weighted CEC efficiency, which provides a competitive advantage and enables improved overall energy capture under varying irradiance conditions. The proposed design achieves this desired efficiency profile by small and low cost

components and a simple controller, and therefore enables a substantial increase in average energy capture per invested capital, and is highly competitive under the figure of merit of [Watts-hour / $]. The controller operates in DCM with a constant peak current and scales the switching frequency as a function of the output power. At high powers the inverter switches in BCM with low RMS current. At low powers, however, the switching frequency decreases and reduces the frequency dependent losses. In addition, the constant peak current enables efficient design of the inductor. We also introduce a fast and stable cycle-by-cycle controller that does not require sensing of the average output current, and thus avoids an expensive current sensor. Overall, the proposed method enables a low-cost design that operates with a small inductor and achieves a peak efficiency of 99.5 % and a weighted efficiency of 99.15 %.

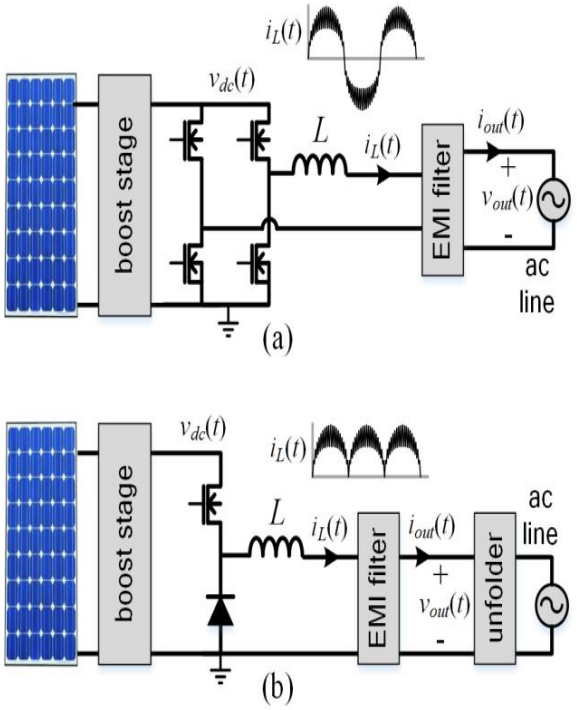

Figure 1. Common micro-inverter power stages. (a) Full bridge. (b) Buck stage with an unfolder stage.

II. VARIABLE FREQUENCY PEAK CURRENT CONTROLLER

In this section we present the constant peak current switching scheme. This new scheme is derived through an analysis of weighted losses in BCM, an analysis that demonstrates that the dominant loss for BCM is switching loss. To improve the weighted efficiency, we explore which peak current is optimal at each output power, and show that in DCM the optimal peak current is constant.

A common topology for micro-inverters is the two-stage topology [24], [25], which includes a boost stage and an inverter stage, as shown in Fig. 1. Typically the boost stage tracks the maximum power point of the PV source, and boosts the low PV input voltage to a higher voltage. The inverter stage generates the AC current that is injected to the AC line. Despite various new topologies that have been demonstrated in recent literature [5], the typical low-cost micro-inverter is still designed either as a full-bridge stage, or as a buck stage with an unfolder stage. The unfolder stage, if present, switches at the zero-crossings of the line voltage to convert the rectified sinusoid at the buck output to a full sinusoid on the AC line.

An illustration of the Boundary Conduction Mode (BCM) waveform is shown in Fig. 2. Although it is soft-switching, and operates with low RMS current, a disadvantage of BCM is its high average switching frequency, which causes high switching losses. As demonstrated by equation (1), the BCM waveform has the highest switching frequency among all DCM waveforms. This is because the peak current of BCM is equal to ipk(t)=2iout(t), which is the lowest possible peak current in DCM, and as a result the switching frequency in BCM is maximal. Equation (1) also predicts that the switching frequency of BCM increases at low output powers, creating a switching frequency profile that causes disproportional switching losses at low powers. This is demonstrated by the last expression in equation (1) for which the power-factor is unity and the switching frequency is proportional to Rout. A lower output voltage vout(t) results in a higher switching frequency, so the switching frequency and switching losses in BCM substantially increase at low voltages and low powers.The switching frequencies in DCM and BCM are given by:

$$\text{DCM:} \quad f_s(t) = \frac{v_{out}(t)}{2L \cdot i_{out}(t)} \left(1 - \frac{v_{out}(t)}{v_{dc}(t)}\right) \left(\frac{2i_{out}(t)}{i_{pk}(t)}\right)^2$$

$$\text{BCM:} \quad f_s(t) = \frac{v_{out}(t)}{2L \cdot i_{out}(t)} \left(1 - \frac{v_{out}(t)}{v_{dc}(t)}\right)$$

BCM with unity power factor :

$$f_s(t) = \frac{R_{out}}{2L} \left(1 - \frac{v_{out}(t)}{v_{dc}(t)}\right) \quad \text{, where } R_{out} = \frac{v_{out}(t)}{i_{out}(t)}$$

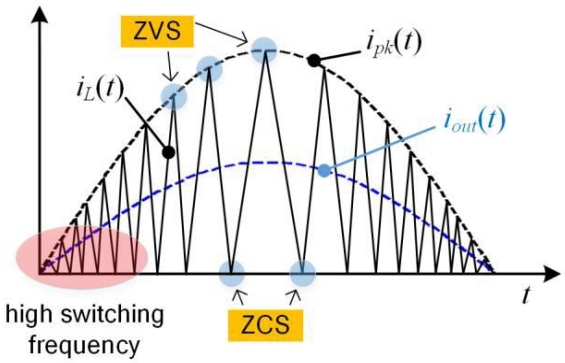

Figure 2. Illustration of the inductor current in BCM, showing soft switching transitions (ZVS, ZCS) and the variations in switching frequency over the line cycle.

The losses in this figure are averaged over a line cycle, and are shown in percent relative to the cycle averaged output power. The total loss is composed of four types of loss: conduction losses, switching losses, proximity loss in the inductor, and core loss in the inductor. The losses are computed according to the calibrated loss model presented in Section IV. The conditions for the test are AC voltage of 220 Vrms @ 60 Hz, average AC power of 300 W, bus voltage of 425 V, and an inductor of 300 µH built on a PQ 26/20 core. The results demonstrate that the dominant loss mechanism in BCM at low powers is switching loss.

This data in Fig. 3 suggests that the weighted efficiency of BCM may be substantially improved if the low power switching losses are reduced. According to equation (1), this may be achieved by increasing the peak current. To demonstrate this idea, Fig. 4 compares a BCM waveform and a DCM waveform with a higher peak current. Although both waveforms provide the same average current (iout), the DCM waveform delivers more energy to the output at every cycle, and as a result operates with a lower switching frequency that enables lower switching losses.

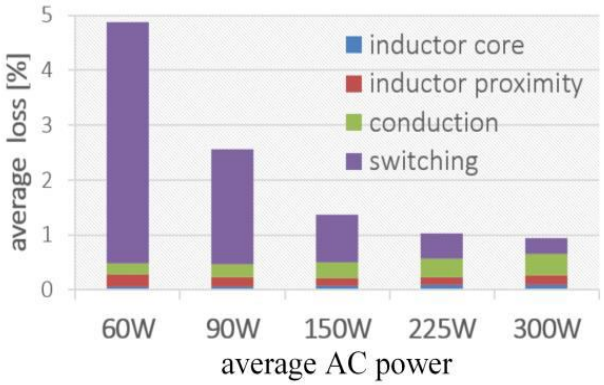

Figure 3. Distribution of losses in BCM. The vertical bars represent average losses over an AC line cycle. The losses are shown in percent relative to the average AC output power. Switching losses dominate at low powers.

Thus, to achieve a certain average current, the controller can vary either the peak current or the switching frequency of the inductor current waveform. A higher peak current reduces the switching frequency, but also raises the RMS current and causes more conduction losses. At each operating point, there is an optimal peak current that minimizes the sum of these losses. To discover which peak current is optimal, Fig. 5 shows a plot of efficiency as a function of peak current (ipk) at various DC operating points. Each curve in this figure corresponds to one DC operating point, with fixed average current and voltage (iout and vout). The minimal ipk at every curve is 2iout, which corresponds to a BCM waveform. The DC operating points are selected with constant ratio of voltage and current vout/iout = Rout, and thus reside on the same output sinusoid. The efficiency is computed according to the calibrated loss model presented in section IV, with conditions as follows: Rout = 215.1 Ω, average AC power of 225 W, bus voltage of vbus = 425 V, and an inductor of 300µH built on a PQ 26/20 core. Each curve is label by its output power pout = voutiout, which is given in percent relative to the maximal instantaneous output power of 450 W.

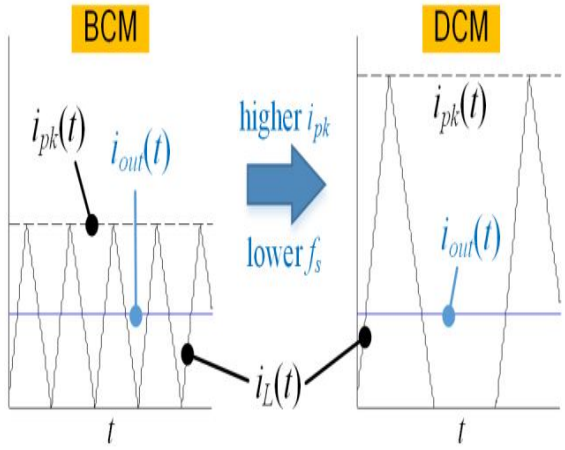

Figure 4. By increasing the peak current in DCM, the switching frequency is reduced, while the averge nductor current (iout) is unchanged.

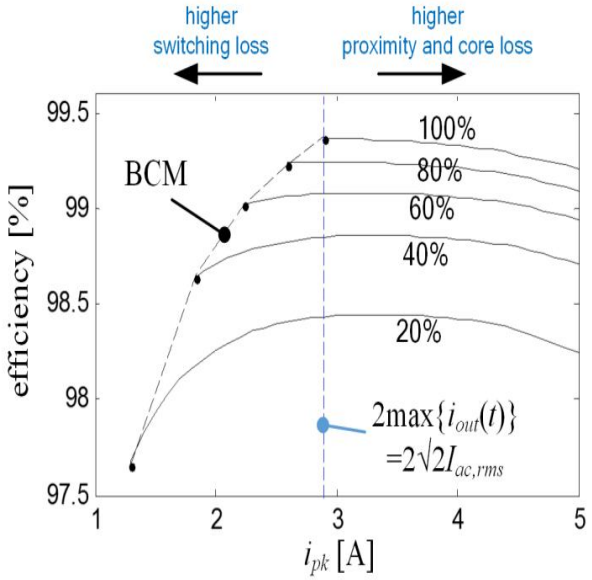

Figure 5. The optimal peak current at various powers. Each curve shows the instantaneous efficiency as a function of peak current (ipk) at a certain DC operating point. The output power of each curve is shown in percentage relative to the peak instantaneous output power.

Figure 5 reveals that the optimal peak current is nearly equal at all operating points, and that this optimal value is Ipk = 2max{iout(t)}, or Ipk = 2√2Iac,RMS, where Iac,RMS is the RMS current injected to the AC line. At peak currents that are lower than this optimal value the frequency dependent losses are dominant. However, at peak currents higher than this optimal peak value, proximity and core losses in the inductor dominate, because the inductor must support a higher peak current. This is because the minimal possible peak current of the inductor is the peak current that occurs at BCM at maximum power, which is Ipk = 2max{iout(t)}. If the peak current is increased above this minimal value, the inductor must support a higher peak current, and therefore must use more turns of wire or operate with a higher magnetic flux density, which results in increased proximity loss or core loss. Therefore, a peak current that equals to the peak current of BCM at full load, namely Ipk = 2max{iout(t)}, minimizes the sum of switching losses and the inductor related losses, and maximizes the efficiency.

A conclusion from Fig. 5 is that a controller that operates in DCM with a constant peak current of Ipk = 2√2Iac,RMS provides an optimized weighted efficiency in DCM. An illustration of the optimal inductor current over a line cycle is plotted at Fig. 6. The switching frequency of this waveform is given in equation (2), and plotted in Fig. 7. The controller scales the switching frequency according to the instantaneous output power. At low powers near the zero crossings it operates with a low switching frequency. At high powers, the switching frequency increases and the controller operates at BCM. In addition, the inductor is designed with minimal peak current, and therefore uses the minimal number of turns and magnetic flux density. Combined, all these factors result in high efficiency at both low powers and high powers.

The switching frequency of the proposed constant peak current controller is:

$$f_s(t) = \frac{2v_{out}(t)i_{out}(t)}{L \cdot I_{pk}^{\,2}}\left(1 - \frac{v_{out}(t)}{v_{dc}(t)}\right)$$

$$\text{where } I_{pk} = 2\max_t\{i_{out}(t)\} = 2\sqrt{2}I_{ac,RMS}$$

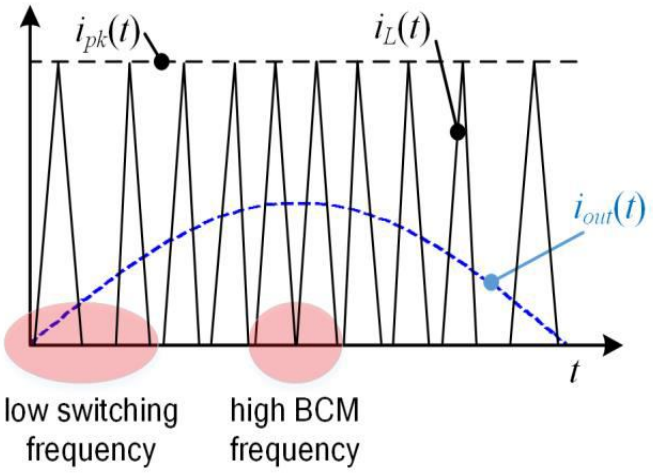

Figure 6. Inductor current waveform of the proposed peak current controller. The inductor peak current is constant, and the switching frequency is scaled in proportion to the output current.

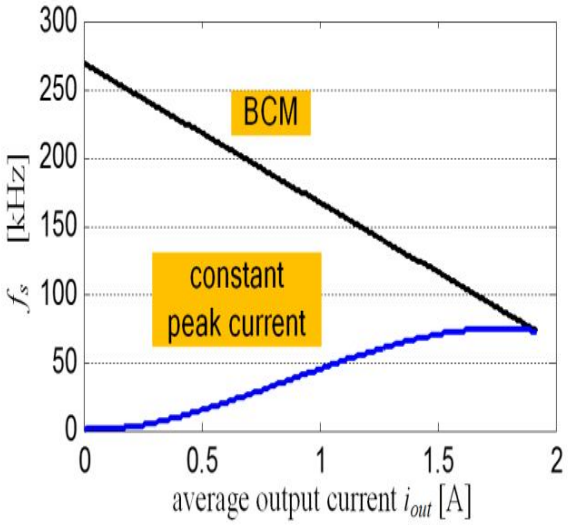

Figure 7. Switching frequency of BCM and the proposed controller. Condition: L=300 µH, vbus=425 V and Rout=161.3Ω

III. METHODOLOGY

As we know the widespread use of power converter makes substantial contribution to energy saving but simultaneously considerably increases noises and thus intensifies electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems[1]. Due to switch on and off large amount of current and voltages in power converters gives rise to EMI, also known as radio frequency interference (RFI)[6]. Within a few last decades the research is continued in this field, the many available techniques include appropriate design of converter (e.g., the use of input and output filters, correct design of printed circuit boards, grounding and shielding) having their limited size, weight, design complexity, efficiency, costs, etc and proper organization of switching process i.e soft switching technique which significantly reduce the switching dv/dt and di/dt, but today it hasn't acted on the noise source, the effect is limited[1]. Another effective techniques is to modulate the constant switching frequency fsw, by the action of low frequency additional signal (periodic, random or chaotic). having a spectrum with lower peak amplitude than the constant frequency square signal, while keeping the desired duty. This can be achieved by using a variable switching frequency, obtained by modulating a base value (carrier frequency, fc) in a way known as frequency modulation technique. Also known as spread-spectrum technique and still developed for radio communications, currently broadens its scope in the field of power converter[1]. modified and effective way of simple frequency modulation is to use chaotic frequencyspreading technique has been a new effective technology for EMI suppressing recently. It modulate the original constant frequency by chaos system poses continuous spectrum with lower amplitude hence EMI will be suppressed effectively[2-3]. This paper, based on the analysis of the relationship between PWM switch scheme and EMI spectrum, a simulation study and analysis have been made on a commercial PWM scheme and compare them with latest technique. The chaotic converter work stable and EMI is suppressed effectively research for EMI problem now continuously growing and investigating with different modulation techniques.

Simple frequency modulation techniques

Starting energy has spread by various technique of modulating in this technique.

Therefore it gives wider spectrum having lesser amplitudes.

Various modulation profile are:

1. Exponential
2. Triangular
3. Sinusoidal

From sinus-wave study we can derive the consequence of frequency modulation for each and every harmonic With lesser amplitude of wider spectrum depends upon various factor

1. Profile of modulation
2. Frequency of modulation [f_m]
3. Carrier frequency [f_c]
4. Index of modulation [m_f]
5. Rating of percentage or $\delta\%$

$$m_f = \frac{\Delta f_c}{f}$$

m_f = index of modulating

Δf_c = switching- frequency of peak deviation

f_m = modulating frequency

$$\delta = \frac{\Delta f_c}{f_c}$$

δ = rating of modulation

Technique of Chaotic-frequency modulation

The principal operational of both chaotic frequency-modulation technique and simple frequency- modulation technique is same. In this frequency of PWM is spread chaotically. Here energy get distributed with lesser amplitude, then EMI get decreases.

Switch converter of Chaotic PWM frequency-spreading scheme is explained by f(t)

f(t)= $f_s + \Delta f(3)$

f_s =original unvarying frequency of PWM

Δf =modulating frequency of PWM

While additional-frequency [Δf] will zero in that case pulse vary like original constant PWM frequency. While additional frequency [Δf] vary with periodically at that moment pulse of PWM vary with periodically. While additional-frequence[Δf] vary chaotically at that time PWM pulse vary chaotically. In technique of chaotic-frequency modulation, [Δf] vary as per chaotic-sequence and it can be generate by these following method:

1 Chaotic map [Logistic-map]
2 Simple chua's circuit

$$\xi_{i+1} = A\,\xi(1-\xi_i)$$

A = controlling parameter

$[\xi_i]$ is known as modulating signal which coming from logistic-map and as per this Δf vary chaotically or with periodically. At time of discrete, state variable has to update. Simulation of logistic-map in MATLAB has to generate in range of 0-7.9. Logistic-map simulation is shown in the fig. While controlling parameter A has progressively increased starting 0 – 8, the logistic- map show transition among chaotic and regular behaviour.

If $0 < A < 1$ then map produce fixed- point where it is constant

$1 < A < 4$ stability of fixed-point will losses and one more fixed-point will come into view into segment [0,1]

$4 < A < 5$ at this point ξ_i is unsteady

While after the value of 5 is exceeds, then next logistic occurs. Four cycle newly appears.

While a later this cycle will become unstable, giving origin to consequent constant 8 cycles. Consequent period of doubling logistic of a=7.9 is get reach. In this value the time of attractive cycle deviation and all limited cycle of time will become repulsive.

While $0 < A < 8$ logistic-map may be has a cycle of several aperiodic and periodic sequence ,it give ascend to chaotic behaviour and aperiodic is sequence and completely its chaotic.

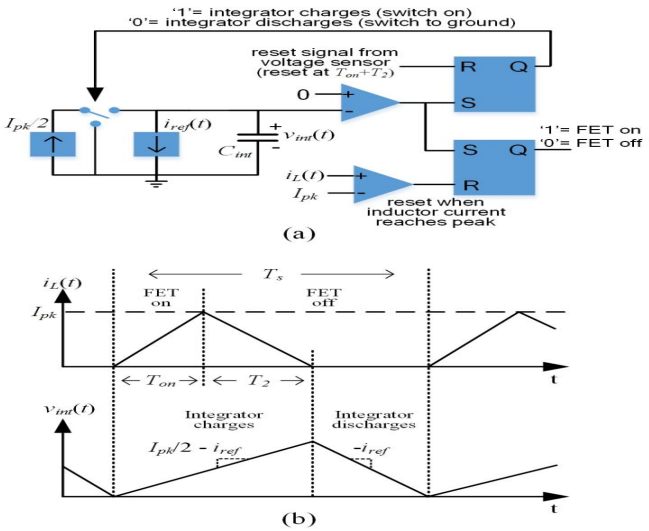

Figure 8.

IV. EXPERIMENTALLY CALIBRATED LOSS MODEL

The loss model is designed to predict the power losses in a buck power stage that operates in DCM, with a lower FET and an upper diode, similar to the experimental power stage described in section V. The power stage is shown in Fig. 11, and the switching devices, voltages and other variables are detailed in Table I. The model parameters were calibrated, using a least-squares criterion, to a large amount of power loss data that were measured at various operating points and switching frequencies. As a result, the calibrated model predicts the power loss with a standard deviation error of 0.5 W, which translates to 0.16% error in efficiency at 300 W, so the model accurately predicts the loss in the experimental power stage.

The model includes four sources of loss: conduction losses, switching losses, inductor core loss, and inductor AC and DC copper losses. Conduction losses are computed by the following equation:

$$P_{conduction} = \frac{R_{FET,on}}{T_s}\int_0^{T_s} {i_{FET}}^2(t)\,dt + \frac{1}{T_s}\int_0^{T_s} i_{DIODE}(t)\cdot v_{DIODE}(t)\,dt$$

$$R_{FET,on} = 0.38\,\Omega, \quad v_{DIODE} = 1.0466 + 0.118\cdot\ln\left(i_{diode}\right)$$

Where iFET(t) and idiode(t) are the current waveforms in the FET and diode during a cycle, Ts is the period of these waveforms, and RFET,on is the FET on resistance. The diode forward drop vdiode depends on the diode current and is fitted to the experimental curve of the selected diode. These losses are computed per switching cycle, and than averaged over a 60 Hz line cycle to predict the average loss.

The loss model also includes two loss mechanisms that are related to the inductor: core loss and proximity loss. Core losses are caused by AC variations in the magnetic flux density B(t) within the magnetic core. AC and DC copper losses are Ohmic losses in the inductor wires that are increased through the skin and proximity effects. Both effects are well known. The core loss is evaluated by the iGSE model given in [26] and the proximity loss is evaluated by the model in [27]. To evaluate these losses we used a computer program that fully modeled the inductor geometry, using parameters of the specific magnetic core, air gap, and Litz wire configuration. This program is available in [28].

Although DCM operation substantially reduces the diode reverse recovery loses, switching loss is nonetheless a dominant loss mechanism at high switching frequencies. A substantial loss mechanism is induced by semiconductor

output capacitances and the associated ringing. An example of this well-known phenomenon is shown in Fig. 9. These oscillations cause energy losses that are manifested by a decay in the oscillations amplitude over time. In addition, when the FET is turned on, its parasitic drain-to-source capacitor is shorted, and any energy stored in this capacitor is lost. The resulting loss depends on the exact amplitude of the oscillation when the FET turns on. If most of the oscillating energy is stored in the inductor during the turn-on, the parasitic capacitor voltage is low, and the energy loss is low. However, if most of the oscillating energy is stored in the parasitic drain-source capacitor, the energy loss is high.

Predicting the exact ringing loss in every DC operating point is very challenging, because this loss highly depends on the moment of switching, and thus is largely affected by small parasitic components. The main problem is that the amplitude of the oscillating voltage at the moment of switching is unknown, and so the energy stored in the drain-source capacitance is also unknown. However, over an AC line cycle, the operating point varies, and the switching occurs at many different voltages, and as a result, the average loss over a cycle is well predicted by a probabilistic model, which assumes that the oscillating voltage distributes randomly over a range. Such model is derived next.

At each time point, the voltage range in which the switching node oscillates is defined by {vlow(t), vhigh(t)}, where vlow(t) is the low bound of the oscillating voltage, and vhigh(t) is the high bound of the oscillating voltage. Time t=0 is the moment in which the inductor current reaches zero and the oscillations commence. At this initial time, the voltage oscillates between the input voltage Vdc and the voltage Vdc-2vout. After infinite time, if no switching occurs, all the energy is lost, and the switching node voltage is constant at Vdc-vout. Between these points, the range of oscillations decays exponentially, at a rate proportional to the inductance L, as described by the following equation:

$$v_{high}(0) = V_{dc}, \quad v_{low}(0) = V_{dc} - 2v_{out}$$
$$v_{high}(\infty) = V_{dc} - v_{out}, \quad v_{low}(\infty) = V_{dc} - v_{out}$$
$$\Downarrow$$
$$v_{high}(t) = V_{dc} + v_{out}\left(-1 + \exp\left(-\frac{R_d t}{2L}\right)\right)$$
$$v_{low}(t) = V_{dc} + v_{out}\left(-1 - \exp\left(-\frac{R_d t}{2L}\right)\right)$$

where Rd is a parameter that governs the rate of decay in the oscillating voltage amplitude. The value used in the calibrated model is Rd = 11 Ω.

The switching loss due to ringing is evaluated by the function Eoss(vds) which defines the energy stored in the FET drain-source capacitance as a function of drain-source voltage.

This function may be found in the FET datasheet (see Table I). The loss due to the decay in the oscillation amplitude over time is defined as Pringing-resistive, and is calculated by the difference of the initial energy in the drain-source capacitor, Eoss(Vdc) and the maximal energy in this capacitor at the time of the switch, Eoss(vhigh). The second loss component describes the loss of energy when the drain-source capacitance is shorted, and is defined as Pringing-capacitive. This loss is computed by the average energy loss over the range vlow and vhigh. The total switching loss is evaluated by the following equation

$$P_{switching} = P_{ringing-resistive} + P_{ringing-capacitive}$$
$$P_{ringing-resistive} = f_s \cdot \left(E_{oss}(V_{DC}) - E_{oss}(v_{high})\right)$$
$$P_{ringing-capacitive} = f_s \cdot \frac{1}{v_{high} - v_{low}} \int_{vlow}^{vhigh} E_{oss}(v)\,dv$$

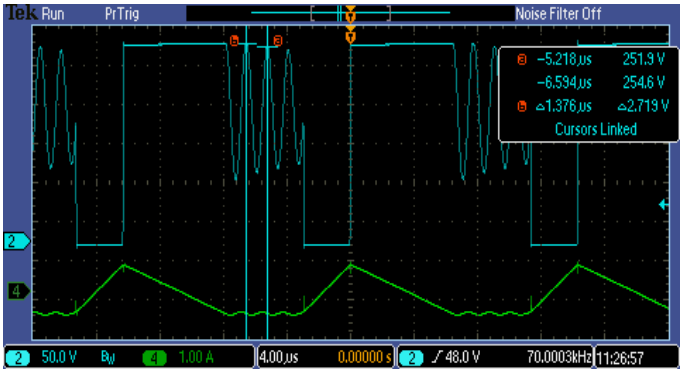

Figure 9. Oscillations in the switching node voltage when the inductor current reaches zero in DCM. Ch2 (blue) – switching node voltage. Ch4 (green) – inductor current.

V. CONCLUSION

This work presents a switching scheme and a control method that achieve high weighted efficiency in solar micro-inverters. Through a detailed analysis of the losses in DCM, we explore what is the best balance between switching frequency and peak current at various powers. The conclusion is that the sum of conduction losses and frequency dependent losses is minimized by a peak current that is constant at all output powers, and therefore a switching scheme that uses variable frequency and constant peak current optimizes the weighted efficiency. This scheme presents two main benefits, a switching frequency that scales with power, and a low peak current that enables efficient magnetic design of the inductor.

At high powers, the switching frequency matches the frequency of BCM, so the RMS current is low, and at low powers the switching frequency decreases, and the switching losses are low. Since the peak inductor current is constant and low, the inductor may be designed with fewer turns of wire, or with lower flux density, and is thus highly efficient, even when implemented on a small magnetic core. The proposed constant current switching scheme is controlled by a chaotic frequency modulation technique which reduces EMI and increases efficiency of the device.

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