A Review on Design of PVT Insensitive Low Power SRAM Cell

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Abstract- *Static Random Access memory (SRAM) is a matrix of static volatile memory cell. 6T SRAM suffers from read current disturbance, 8T SRAM has leakage in read path, 9T SRAM increases read access time. 10T differential Schmitt trigger SRAM cell suffered from read write conflict and it is vulnerable to noise. Write assist circuits, boosted supply, gated feedback write assist, cross point data aware are the few technologies used for power optimization and Challenges regarding reduction of static and dynamic power. Single ended topologies reduce the leakage and half of the active switching power and saves chip area.This paper presents the review of previous SRAM cell and proposed process, voltage and temperature variation (PVT) insensitive low power cell using single ended Schmitt trigger for high stability.*

Keywords- Leakage current, low power, SRAM, stability, static noise margin (SNM), Schmitt trigger.

I. INTRODUCTION

The Schmitt Trigger is a comparator circuit that incorporates positive feedback. Noise is being ignored by CMOS Schmitt Trigger as the hysteresis in a Schmitt Trigger circuit offers a better noise margin and noise stable operation. Reducing the power dissipation in memories can significantly improve the system power efficiency, performance, reliability and overall costs.

SRAM or Static random access memory is a form of semiconductor memory widely used in electronics, microprocessor and general computer applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion and does not need to be dynamically updated as in the case of DRAM memory. While the data in the SRAM memory does not need to be refreshed dynamically, it is still volatile meaning that when the power is removed from the memory device, the data is not held and will disappear.

SRAM memory basics

There are two key features of SRAM memory:

1. The data is held statically: This means that the data is held in semiconductor memory without the need to be refreshed as long as power is applied to the memory.
2. SRAM is a form of random access memory: A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed.

The circuit for an individual SRAM memory cell comprises typically four transistors configured as two cross coupled inverters. This circuit has two stable states and these equate to the logical “0” and “1” states. In addition to the four transistors in the basic memory cell, additional two transistors are required to control the access to the memory cell during the read and write operations. This makes a total of six transistors, making what is termed a 6T memory cell. Further transistors are used to give either 8T or 10T memory cells.

II. OVERVIEW OF CMOS INVERTER

The gate of an MOS transistor controls the flow of current between the source and drain. When the gate of an NMOS transistor is 1, the transistor is ON and there is a conducting path from source to drain. A PMOS transistor is just the opposite, being ON when the gate is low and OFF when the gate is high.The bar at the top indicates VDD and the triangle at the bottom indicates GND. The output Y is pulled up to 1 because it is connected to VDD but not to GND [2].

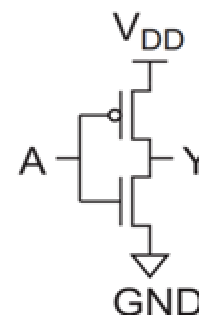

Fig.1. Basic ST inverter [1]

III. OVERVIEW OF SCHMITT TRIGGER

When the input is higher than a certain chosen threshold the output is high; when the input is below another (lower) chosen threshold the output is low and when the input is between the two the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis and implies that the Schmitt Trigger has some memory. The benefit of a Schmitt Trigger over a circuit with only a single input threshold is greater stability (noise immunity).

The standard CMOS Schmitt Trigger circuit design is shown below. Initially, IN = 0 V, the two stacked p-MOSFET (P1 and P2) will be on. Hence OUT = VDD. When IN rises to VTN, N1 is on. But N2 is still off since N3 is on and source voltage of N2 is VDD. Now N1 and N3 form an inverting NMOS amplifier. Thus, source voltage of N2 is falling with increasing IN. When source voltage of N2 drops to VTN, N2 is on. Now both N2 and N1 are on, OUT approaches to 0V rapidly and N3 becomes off. When IN approaches VDD, the two stacked n-MOSFET (N1 and N2) will be on. Hence OUT = 0.

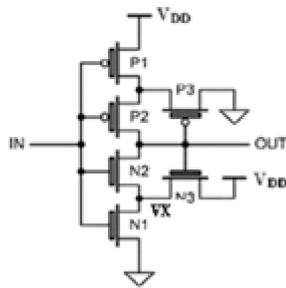

Fig.2. Schmitt trigger [3]

When IN falls to |VTP|, P1 is on. But P2 is still off since P3 is on and source voltage of P2 is 0 V. Now P1 and P3 form an inverting PMOS amplifier. Thus, source voltage of P2 is rising with decreasing IN. When source voltage of P2 rises to |VTP|, P2 is on. Now both P1 and P2 are on, OUT approaches to VDD rapidly and P3 becomes off [3].

IV. REVIEW OF SRAM CELL

1. Review of 6T SRAM cell

The standard cell comprises six transistors, as shown in fig.3.The nMOS access transistors (A1 and A2) located at the ends of circuit and a pair of cross-coupled inverters constitute memory cell. The nMOS elements (D1 and D2) of the latch are the driver transistors, while pMOS (P1 and P2) are the pull-up transistors. The access transistors operate when the word line is raised, for read or write operation, connecting the cell to the bit lines (Bit line, ~Bit line). The cell has three different operation modes. In the standby state, word line is not asserted, so access transistors are turned off. Therefore, cell cannot be accessed and two cross-coupled inverters continue to feedback each other as long as they are connected to the supply, data will hold in the latch. The read operation starts by pre-charging the bit lines high then allowing them to float. Then word line is asserted turning on all access transistors. The data stored in the nodes are driven onto bit lines. A voltage difference is developed between bit lines and a sense amplifier detects the value of the cell.

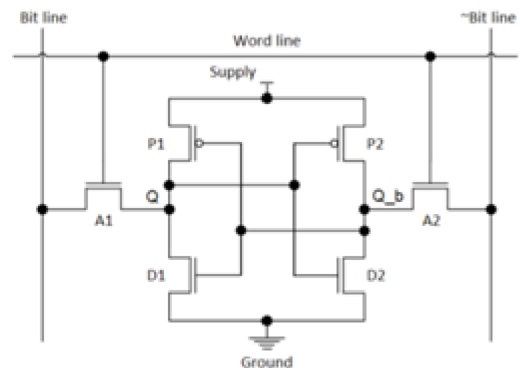

Fig.3. 6T SRAM cell

During the write operation the bit lines are driven to complementary voltage level sand then word line is raised. The data to be written into the cell are driven onto the bit lines and one of the storage nodes is discharged through the access transistor [2]. 6T SRAM cell suffers from read-current disturbance-induced SNM degradation with Vdd scaling. Also, the read stability and the write stability of 6T SRAM cell degrade to unacceptable level at low supply voltages due to process variations [1].

2. Review of 7T SRAM Cell

7T SRAM cell uses a novel write mechanism which depends only on one of the 2-bit lines to perform a write operation which reduces the activity factor of discharging the bit-line pair. Both, the read delay and the static noise margins are maintained after carefully sizing the cell transistors [5]. It is read disturb free bitcell in which an extra transistor is added in the pull down path of one of the coupled inverters [1].

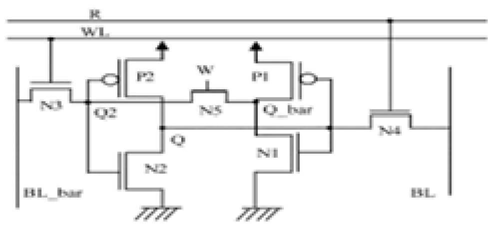

Fig.4. 7T SRAM Cell Novel Write Mechanism [5]

3. Review of 8T SRAM Cell

8T-SRAM cell has 30% more area than a conventional 6T-SRAM cell but the 30% area overhead is composed of not only the two added transistors but also of the contact area of the word-line for write operations. Also it suffers from leakage in read path, write delay and degraded read zero. While WL contact area is conventionally assigned to the boundary line between two SRAM cells in this SRAM cell the WWL contact area is assigned to within a cell as shown in below[5].

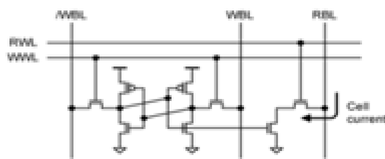

Fig.5. 8T SRAM cell

4. Review of 9T SRAM cell

The upper sub-circuit of the 9T memory cell is essentially a conventional 6T SRAM cell. The write operation is identical with the conventional 6T SRAM cell but 9T SRAM has increased read access time. The lower sub-circuit of the 9T memory cell is a differential read port. Prior to a read operation both bitlines are precharged to start a read operation, the read signal transitions from 0 to 1. One of the bitlines is discharged depending on the data that is stored in the cell [6]

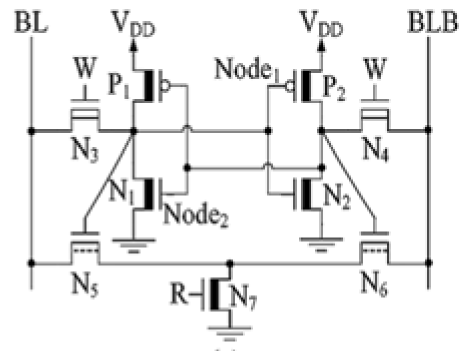

Fig.6. 9T SRAM cell

5.Review of 10-T SRAM Bitcell

Transistors PL-NL1-NL2-NFL form one ST inverterwhilePR-NR1-NR2-NFR formanotherST inverter. AXL and AXR are the access transistors. The positive feedback from NFL/NFR adaptively changes the switching threshold of the inverter depending on the direction of input transition. During a read operation due to voltage divider action between the access transistor and the pull-down NMOS, the voltage of node rises. If this voltage is higher than the switching threshold (trip point) of the other inverter, the contents of the cell can be flipped, resulting in a read failure event. In order to avoid a read failure, the feedback mechanism should increase the switching threshold of the inverter PR-NR1-NR2. Transistors NFR and NR2 raise the voltage at node and increase the switching threshold of the inverter storing “1”. Thus, Schmitt trigger action is used to preserve the logic “1” state of the memory cell. [7]. 10T SRAM is read disturb free differential 10Tbitcell. It has two series connected transistors in its write path, which degrade write ability of the bitcell. It is also vulnerable to noise [1].

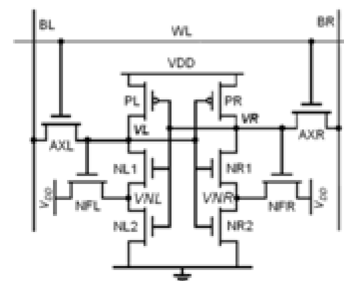

Fig.7.10T SRAM cell

V. SOURCES OF VARIATION

Variation is the deviation from intended values for structure or a parameter of concern. The electrical performance of modern IC is subject to different sources of variations that affect both the device (transistor) and

interconnect. For the purposes of circuit design the process variation can broadly be categorized into three classes:

1. Process Variation

1) Die-to-Die (D2D): Also called global or inter-die variations affect all devices on the same chip in the same way (e.g., they may cause all the transistors gate lengths to be larger than a nominal value).
2) With-in Die (WID):Also called local or intra-die variations correspond to variability within a single chip and may affect different devices differently on the same chip (e.g., devices in close proximity may have different Vth than the rest of the devices
3) Random variations: As the name implies they are the sources that show random behaviour and can be characterized using their statistical distribution.
4) 4)Systematic variations: Show certain variational trends across a chip and are caused by physical phenomena during manufacturing such as distortions in lenses and other elements of lithographic systems. Due to difficulties in modeling this type of variation they are usually modeled as random variations.[14]

2. Supply Voltage Variation

Variations in switching activity and diversity in the type of logic result in uneven power dissipation across the die. This variation results in uneven supply voltage distribution and temperature hot spots, causing transistor sub-threshold leakage variation. The supply voltage (Vcc) will continue to scale modestly by 15% not by the historic 30% per generation, due to

1) Difficulties in scaling threshold voltage (Vth)
2) To meet the transistor performance goals. Maximum Vcc is specified as a process reliability limit and minimum Vcc is required for the target performance [13]

2. Temperature Variation

Within-die temperature fluctuations have existed as a major performance and packaging challenge for many years. Both the device and interconnect performance have temperature dependence, with higher temperature causing performance degradation. Additionally, temperature variation across communicating blocks on the same chip may cause performance mismatches, which may lead to logic or functional failures. The delay and the power suffer from an increase in the circuit temperature mainly due to the adverse impact of temperature on the drain current and interconnect resistance. Temperature also affects certain variables such as the mobility and Threshold voltage which determine Id drain current, Idsat drain current insaturation and Req equivalent resistance of the transistors[13].

VI. CHALLENGES

At high negative bias and elevated temperature, the PMOS VT gradually drifts to become more negative, thus reducing PMOS current drive and affecting cell stability, margin and Vmin (minimum operating voltage) of SRAM.

The need for low power in digital devices is responsible for the scaling of the supply voltage.

In addition to the standby power consumption, access time and the cell stability are important parameters of consideration during the design of low power SRAM cell.

The cell stability represented by the noise margin is another important criterion during the design of the cell.

Higher noise margin ensures that the data is secure and probability of accidental changes is kept to minimum [8].

VII. PROPOSED 11T SRAM CELL

In the proposed cell hard coding technique is used. Word bit line and virtual ground control signals are used significantly.

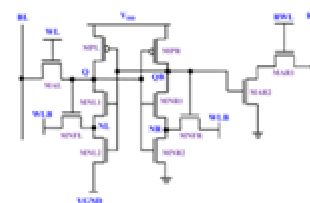

Fig.8. 11T SRAM cell

The write-access transistor MAL is controlled by row-based WL, and the read-access transistor MAR1 is controlled by row-based read WL (RWL). MAR1 is controlled by row-based read WL (RWL). The feedback transistors of ST, MNFL and MNFR are controlled by internal storage nodes Q and QB. The virtual ground (VGND) is row-based, and WLB and BLs (BL and RBL) are column-based. When RWL=1 path for RBL is connected through MAR1 and MAR2, when WL=0 data storage Q and QB are decoupled. So, RSNM is nearly equal to HSNM.

As HSNM is very high read stability is remarkably improved. In read and hold mode WLB=VDD. For writing, WL=1 and RWL=0 VGND =floating. Writing speed is

increased as there is no feedback from feedback transistor MNFL and MNFR as NL and NR<1. System has read buffers to decouple storage nodes (Q&QB) to eliminate read disturb problem. Decrease in the size of pulldown transistors reduces leakage current along with cell area at expense of speed. So, to keep balance minimum width transistor are used for cell core and increase widths of MAL, MAR1 and MAR2 to reduce the access delay[1].

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