A Wide Range, Low Power, Better Phase Noise VCO Using 45nm Technology

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Abstract- *VCO is the important part of many receivers' likes WLAN, GPS and much other application. Many researchers have done many researches to obtain better VCO for these applications. Ring and LC VCO are the types of VCO of which LC VCO is catching wide attention because of better phase noise, lower power consumption and large tuning range.One of the important parameter of VCO is phase noise. As the value of phase noise is more negative, better VCO will be able to filter the noise and provide better output. Since it's a very difficult task to obtain, various architecture have been adopted to improve this parameter. Out of this architecture's, cross coupled topology has found to be the best architecture.*

So this thesis based on this same architecture with little modifications. First is a PMOS and a NMOS is added on each side, secondly inductor is placed in series with capacitor and NMOS in parallel at the source end NMOS block. All this modifications contribute to obtain better phase noise and tuning range. L in series with NMOS and C in parallel at the end of NMOS block is used for filtering purpose.

In this thesis, 20 GHz LC VCO is shown with the help of which better phase noise and FOM is obtained. Whole circuit is implemented on 45nm technology. A 15.36 GHz tuning range is obtained with tuning voltage of 0-1.4V. The power consume by the whole circuit is 1.78mW-2.75 mW which is better than the other listed papers shown in the references. The supply voltage is 1V.

I. INTRODUCTION

Voltage Controlled Oscillator is tunable oscillator whose output frequency is linear function of control voltage.

1. Characteristics of VCO

a) Phase Noise

Noise in phase is referred as phase noise which is basically a random deviation in frequency or random variation in zero crossing point of time dependent oscillator waveform.

David B. Lesson in 1966 given a phase noise model commonly known Lesson's model for oscillator the phase noise predicated by this model is can be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{2FK_T}{P_s}\left[1+\left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f}}{|\Delta\omega|}\right)\right]$$

By choosing carefully power supplies, power supply noise and tuning voltage supply noise can be minimized. Due to this reason phase noise of the VCO is mainly determined by the overall quality factor Q of the circuit.

b) Tuning Range:

Frequency of oscillation for LC tank is given below by manipulating equation

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Tuning of capacitor is achieved by use of voltage dependent capacitor which is varactor. By varying the voltage of these varactor maximum and minimum capacitance can be obtained which help to calculate minimum and maximum oscillation frequency .

c) Power Dissipation:

Today many wireless devices are required long life of battery which means that have low power consumption. But for VCO designer it's difficult to obtain low power consumption and low phase noise simultaneously. This because of tank voltage amplitude is proportional to current flowing. It means that there is trade-off exist between phase noise and power consumption.

$$V_{tank} \approx I_{total}.R_{eq}$$

II. LITERATURE SURVEY

Mahmoud Moghavvemi and AliyarAttaran[5] demonstrated comparative study of various cross coupled topologies with different configuration for different CMOS processes. In their note they give detail discussion on phase noise reduction for CMOS LC VCO and effect of tail current

source on resonator performance. In last they analyze on 1/f flicker noise contributed by active devices.

Fad et.al [9] demonstrated a comparative study of CMOS LC VCO Topologies in standard 0.35um CMOS technology for Wide-Band Multi-Standard Transceivers. In their study, they simulate both cross coupled differential and CMOS cross coupled differential topology and obtain result.The comparison shows that both circuits are applicable for multistandard transceivers. The complementary VCO shows 50% lower power dissipation with lower phase noise levels. Asa disadvantage, the circuit is suffering from larger parasitics and shows 500 MHz lower maximum operating frequency when compared to the NMOS structure. Although the NMOS topology consumes more current but by reducing the supply voltage the power dissipation significantly reduces due to this reason this topology more attractive for realization in digital technologies with lower supply voltages.

Ali Hajimiri and Thomas H. Lee [15] proposed new physical phase noise model which help to make quantative prediction of phase noise and jitter for different type of oscillators.

Li Zhu[1] proposed current-reuse cross-connected pair is utilized as a negative conductance generator to compensate the energy loss of the resonator. The supply current is reduced by half compared to that of the conventional LC-VCO. An improved inversion-mode MOSFET (IMOS) varactor is introduced to extend the capacitance tuning range from 32.8% to 66%.

Guang Zhu[2] conclude that through optimization, power challenge for high frequency systems can be overcame to some extent.

Qiyang Wu[3] designed An ultra wideband LC voltage-controlled oscillator (LC-VCO) operating in the Ka-band with equally spaced sub-band coarse tuning characteristics. A tunable negative capacitance (TNC) circuit technique is used to cancel the fixed capacitance in the LC-tank to extend the tuning range (TR).

C.-M. Hung[4] demonstrated VCO using 0.1-pm NMOS transistors in a partially scaled CMOS process. The phase noise at a 3-MHz offset is -106 dBc/Hz when the VCO core consumes 24 mW from a 1.5-V supply.

KaChun Kwok[21] publish their work in which Tuning is accomplished by exploiting the 90 phase shift across a transconductor. The frequency is continuously tunable with differential and common-mode ranges of 23.6% and 3.3%.

III. DESIGN

The CMOS LC VCO circuit(Figure.1) is designed by using S-edit from Tanner EDA. The design CMOS LC VCO is simulated using in 65nm CMOS process. This section briefly discusses the simulated transient response and amplitude, tuning range and power consumption of the cross coupled differential LC-VCO designs. The focus is targeted on the measurement of parameters for CMOS LC VCO design.

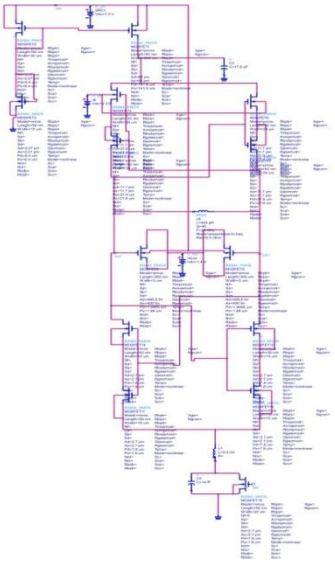

Figure 21. Schematic of LC VCO

1. Measurement of frequency

The frequency of CMOS LC VCO design can be calculated by transient response as show in Fig.2. For frequency calculation, time period (dx) is directly read by oscillation as show in Fig.2 which is equal to 51 ps at 0.65V and Vb=0.3 V. The relation between frequency and time is given below

$$F = \frac{1}{T}$$

In the above expression T is time period of oscillation. The time period of oscillation T is equal to dx. Substituting the value of time in above equation frequency comes out to be,

$$F = \frac{1}{51\ ps}$$

$$F = 20\ GHz$$

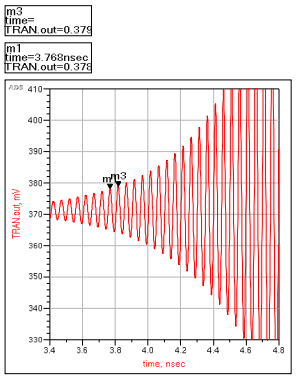

Figure 2. Transient Response of LC VCO.

2. Measurement of tuning range

The fractional tuning range of LC VCO design can be calculated by plotting graph between control voltages and frequencies as show in Fig. 3 by transient analysis.

$$Fractional\ Tuning\ Range = \frac{f_{max} - f_{min}}{f_0} \times 100$$

By the graph is clear that fmaxand fmin is 32.15GHz and 16.79 GHz where f0 is 20 GHz

Power Consumption

The power consumption of VCO can be calculated by formula given below

$$max\ d.c.power\ dissipation = V_{supply} I_{bias}$$

It gives total power consumed by the integrated parts in the circuit. The power consumed by this VCO is 1.78 mW-2.75 mW.

IV. DESIGN

1. Tabulation of Parameters extracted

CMOS LC VCO design has very low power consumption. The low value of power is obtained due to implementation of cross coupled pair of PMOS transistor in design of LC VCO. This design of CMOS LC VCO has very optimized tuning range. The two PMOS are connected back to back and biased in inversion mode in design. In last area is computed using L-edit of tanner EDA. The results are summarized in Table 1.

Table 1. Results of CMOS LC VCO.

S.No.	Parameter	Simulation result	
1.	Technology	45nm	
2.	Power Consumption(mW)	1.78-2.75	
3.	Frequency(GHz)	16.79-32.15	
4.	Tuning Voltage(V)	0.0-1.4	
5.	Tuning Range (%)	68.9	
6.	Phase Noise(dBc/Hz)	-99.23@1MHz	25.85 GHz
		-102@1MHz	30.71 GHz
7.	FOM(dBc/Hz)	-189@1MHz, -193@10MHz at 30.71 GHz	

2. Phase Noise & FOM

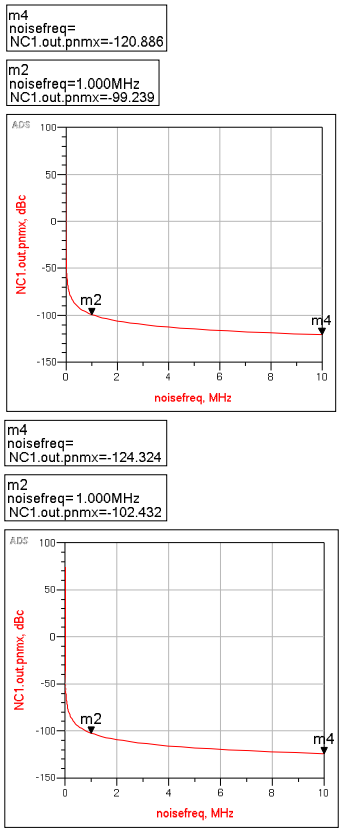

Figure 3. (a) Phase Noise at 25.85 GHz when Vtune=0.0 V and Vb=0.3 V (b) Phase noise at 30.71 GHz when Vtune=1.4 V and Vb=0.3 V.

Fig. 6.1 shows that the phase noise at an offset of 1MHz and 10 MHz is -99.23,-120 dBc/Hz at 25.85 GHz and -102.43, -124 dBc/Hz at 30.71 GHz. FOM of the proposed VCO is -189 dBc/Hz at 30.71 GHz at 1MHz offset,-193 dBc/Hz at 30.71 at 10MHz offset.

3. Comparative study of results

Table 2.

S. No.	Parameter	Ref. [21]	Ref. [3]	Ref. [4]	Ref. [1]	**This work**
1.	Technology (nm)	130	130	100	90	**45**
2.	Supply Voltage (V)	1.2	1.2	1.5	1.5	**1.0**
3.	Power Consumption (mW)	43	11	24	3.1	**1.78-2.75**
4.	Frequency (GHz)	23-29	30.5-39.6	25.3-25.9	27-32.5	**16.79-32.15**
5.	Tuning Voltage(V)	0-1.5	0.4-0.9	0.7-1.5	0-1.6	**0.0-1.4**
6.	Tuning Range(GHz)	6	9.1	0.6	5.5	**15.36**
7.	Phase Noise(dBc/Hz)	-92.6 @1MHz	-100@1MHz	-106@3MHz	-101@1MHz	**-109.4@3MHz at 25.85 GHz -102.43@1MHz at 30.71 GHz**
8.	FOM(dBc/Hz)	-181	-189	-	-185	**-189@1MHz,-193@10MHz at 30.71 GHz**

V. CONCLUSION

A CMOS LC VCO is designed in 45nm CMOS process for high frequency application. This design is simulated on ADS software. In this design, stack mosfet concept with PMOS body bias is used. A inductor is connected in series with Capacitor and a nmos in parallel at the source of nmos to increase phase noise and also used for noise filtering. This VCO works between 16.79 GHz-32.15 GHz frequency with control voltage from 0.0 to 1.4V and bias voltage of 0.3-1.0 V which helps in reducing power consumption. This design has power consumption of 1.78 mW-2.75 mW.

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